PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Book IC06N 1985
New series

High-speed CMOS

PC54/74HC/HCT/HCU

Logic family

NEW HANDBOOK SERIES

HIGH-SPEED CMOS PC54/74HC/HCT/HCU LOGIC FAMILY

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DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover. Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons, travelling-wave tubes, microwave diodes**

ET3 **Special Quality tubes, miscellaneous devices** (will not be reprinted)

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Muller tubes**

T7 **Gas-filled tubes**
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories

T8 **Picture tubes and components**
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display

T9 **Photo and electron multipliers**
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates

T10 **Camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicons and Newvicons**

T13 **Image intensifiers**

T14 **Infrared detectors**

T15 **Dry reed switches**

Data collations on these subjects are available now.
Data Handbooks will be published in 1985.

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave semiconductors** (to be published in this series in 1985)
At present available in Handbook T11

S12 **Surface acoustic wave devices**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES		Superseded by:
IC1	**Bipolar ICs for radio and audio equipment**	
IC2	**Bipolar ICs for video equipment**	IC02N
IC3	**ICs for digital systems in radio, audio and equipment**	
IC4	**Digital integrated circuits** CMOS HE4000B family	
IC5	**Digital integrated circuits – ECL** ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs	IC08N
IC6	**Professional analogue integrated circuits**	
IC7	**Signetics bipolar memories**	
IC8	**Signetics analogue circuits**	IC11N
IC9	**Signetics TTL logic**	IC09N and IC15N
IC10	**Signetics Integrated Fuse Logic (IFL)**	IC13N
IC11	**Microprocessors, microcomputers and peripheral circuitry**	

NEW SERIES

IC01N	**Radio, audio and associated systems** Bipolar, MOS	
IC02N	**Video and associated systems** Bipolar, MOS	(published 1985)
IC03N	**Integrated circuits for telephony** Bipolar, MOS	(published 1985)
IC04N	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family uncased integrated circuits** CMOS	(published 1984)
IC06N	**High-speed CMOS; PC54/74HC/HCT/HCU** Logic family	(published 1985)
IC07N	**PC54/74HC/HCU/HCT uncased integrated circuits** HCMOS	
IC08N	**10K and 100K logic family** ECL	(published 1984)
IC09N	**Logic series** TTL	(published 1984)
IC10N	**Memories** MOS, TTL, ECL	
IC11N	**Linear LSI**	(published 1985)
IC12N	**Semi-custom gate arrays & cell libraries** ISL, ECL, CMOS	
IC13N	**Semi-custom** Integrated Fuse Logic	(published 1985)
IC14N	**Microprocessors, microcontrollers & peripherals** Bipolar, MOS	
IC15N	**Logic series** FAST TTL	(published 1984)

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1 **Programmable controller modules**
PLC modules, PC20 modules

C2 **Television tuners, video modulators, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Synchronous motors and gearboxes**

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements

C10 **Connectors**

C11 **Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 **Potentiometers, encoders and switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Ceramic capacitors**

C16 **Permanent magnet materials**

C17 **Stepping motors and associated electronics**

C18 **D.C. motors**

C19 **Piezoelectric ceramics**

C20 **Wire-wound components for TVs and monitors**

C21 **Assemblies for industrial use**
HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices

C22 **Film capacitors**

INTRODUCTION

PC54/74 HIGH-SPEED CMOS INTEGRATED CIRCUIT FAMILY

The PC54/74 family of integrated circuits are manufactured in a self-aligning, 3 μm polycrystalline silicon-gate CMOS process combined with local oxidation of silicon (LOCMOS). These devices have the low power consumption, high immunity to input noise and wide operating temperature range of earlier silicon-gate CMOS together with the high speed and drive capability of bipolar, low-power Schottky TTL (LSTTL). They are an ideal replacement for LSTTL circuits, reducing power consumption without reducing speed, and will also interface between CMOS and TTL circuits.

All circuits are fully buffered and have typical operating frequencies up to 60 MHz with gate delays in the order of 9 ns. Two types of circuit are available:

HC CMOS input switching levels (1/2 V_{CC}), power supply = 2 to 6 V;

HCT TTL input switching levels, power supply = 5 V (typ).

Features

- Very low power dissipation
- D.C. noise margin of HC types twice that of TTL devices
- Fanout capability of 10 LSTTL loads (4 mA); this is increased to 15 LSTTL loads (6 mA) in devices having bus-driver outputs
- Wide operating voltage range
- Latch-up free operation
- Improved protection against electrostatic discharge
- Functions and pinning identical to our popular LSTTL and CMOS HE4000B families of integrated circuits
- Symmetrical output sourcing and sinking currents and equal output rise and fall times
- Available in plastic and ceramic DIL packages and plastic mini-packs (SO) for surface mounting
- Wide operating temperature range:
  -40 to +85 °C for PC74 series
  -55 to +125 °C for PC54 series

SELECTION GUIDE

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Cross-reference guide

TTL to HCMOS 15

CMOS to HCMOS 24

HCMOS PC54/74 FAMILY

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; D = ceramic (cerdip) DIL; T = plastic SO mini-pack

type no.	description	pins	classification	page
NAND/NOR gates/EXCLUSIVE-NOR gates				
HC/HCT00	quad 2-input NAND gate	14	SSI	121
HC/HCT02	quad 2-input NOR gate	14	SSI	129
HC/HCT03	quad 2-input NAND gate	14	SSI	136
HC/HCT10	triple 3-input NAND gate	14	SSI	150
HC/HCT27	triple 3-input NOR gate	14	SSI	161
HC/HCT30	8-input NAND gate	14	SSI	168
HC7266	quad 2-input EXCLUSIVE-NOR gate	14	SSI	505
HC/HCT4002	dual 4-input NOR gate	14	SSI	671
AND/OR/EXCLUSIVE-OR gates				
HC/HCT08	quad 2-input AND gate	14	SSI	149
HC/HCT11	triple 3-input AND gate	14	SSI	151
HC/HCT21	dual 4-input AND gate	14	SSI	160
HC/HCT32	quad 2-input OR gate	14	SSI	169
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	14	SSI	215
HC/HCT4075	triple 3-input OR gate	14	SSI	731
Inverters/buffers/line drivers/level shifters				
HC/HCT04	hex inverter	14	SSI	137
HCU04	hex inverter (unbuffered)	14	SSI	145
HC/HCT125	quad buffer/line driver; 3-state	14	MSI	253
HC/HCT126	quad buffer/line driver; 3-state	14	MSI	254
HC/HCT240*	octal buffer/line driver; 3-state; inverting	20	MSI	421
HC/HCT241*	octal buffer/line driver; 3-state	20	MSI	429
HC/HCT244*	octal buffer/line driver; 3-state	20	MSI	453
HC/HCT365*	hex buffer/line driver with common enable; 3-state	16	MSI	545
HC/HCT366*	hex buffer/line driver with common enable; 3-state; inverting	16	MSI	546
HC/HCT367*	hex buffer/line driver; 3-state	16	MSI	547
HC/HCT368*	hex buffer/line driver; 3-state; inverting	16	MSI	548
HC/HCT540*	octal buffer/line driver; 3-state; inverting	20	MSI	617
HC/HCT541*	octal buffer/line driver; 3-state	20	MSI	618
HC4049	hex inverting HIGH-to-LOW level shifter	16	SSI	698
HC4050	hex HIGH-to-LOW level shifter	16	SSI	699
Flip-flops/latches/registers				
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger	14	FF	177
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger	14	FF	187
HC/HCT75	quad bistable transparent latch	16	FF	197
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger	14	FF	223
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	16	FF	233
HC/HCT112	dual JK flip-flop with set and reset; negative-edge trigger	16	FF	242
HC/HCT173*	quad D-type flip-flop; positive-edge trigger; 3-state	16	MSI	365
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger	16	MSI	367
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger	16	MSI	369
HC/HCT259	8-bit addressable latch	16	MSI	495

* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; D = ceramic (cerdip) DIL; T = plastic SO mini-pack

type no.	description	pins	classification	page
Flip-flops/latches/registers (continued)				
HC/HCT273	octal D-type flip-flop with reset; positive-edge trigger	20	MSI	507
HC/HCT373*	octal D-type transparent latch; 3-state	20	MSI	549
HC/HCT374*	octal D-type flip-flop; positive-edge trigger; 3-state	20	MSI	559
HC/HCT377	octal D-type flip-flop with data enable; positive-edge trigger	20	MSI	569
HC/HCT533*	octal D-type transparent latch; 3-state; inverting	20	MSI	597
HC/HCT534*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	20	MSI	607
HC/HCT563*	octal D-type transparent latch; 3-state; inverting	20	MSI	619
HC/HCT564*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	20	MSI	628
HC/HCT573*	octal D-type transparent latch; 3-state	20	MSI	629
HC/HCT574*	octal D-type flip-flop; positive-edge trigger; 3-state	20	MSI	638
HC/HCT670	4 x 4 register file; 3-state	16	MSI	661
HC/HCT40105	4-bit x 16-word FIFO register	16	MSI	783
Shift registers				
HC/HCT164	8-bit serial-in/parallel-out shift register	14	MSI	335
HC/HCT165	8-bit parallel-in/serial-out shift register	16	MSI	345
HC/HCT166	8-bit parallel-in/serial-out shift register	16	MSI	355
HC/HCT194	4-bit bidirectional universal shift register	16	MSI	391
HC/HCT195	4-bit parallel access shift register	16	MSI	401
HC/HCT299*	8-bit universal shift register; 3-state	20	MSI	527
HC/HCT597	8-bit shift register with input latches	16	MSI	640
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register	16	MSI	678
HC/HCT4094	8-stage shift-and-store bus register	16	MSI	738
HC/HCT40104*	4-bit bidirectional universal shift register; 3-state	16	MSI	773
Arithmetic circuits				
HC/HCT85	4-bit magnitude comparator	16	MSI	207
HC/HCT181	4-bit arithmetic logic unit	24	MSI	379
HC/HCT182	look-ahead carry generator	16	MSI	381
HC/HCT280	9-bit odd/even parity generator/checker	14	MSI	517
HC/HCT283	4-bit full adder with fast carry	16	MSI	524
HC/HCT583	4-bit full adder with fast carry	16	MSI	639
HC/HCT688	8-bit magnitude comparator	20	MSI	663
Counters				
HC/HCT93	4-bit binary ripple counter	14	MSI	222
HC/HCT160	presettable synchronous BCD decade counter; asynchronous reset	16	MSI	328
HC/HCT161	presettable synchronous 4-bit binary counter; asynchronous reset	16	MSI	329
HC/HCT162	presettable synchronous BCD decade counter; synchronous reset	16	MSI	330
HC/HCT163	presettable synchronous 4-bit binary counter; synchronous reset	16	MSI	332
HC/HCT190	presettable synchronous BCD decade up/down counter	16	MSI	383
HC/HCT191	presettable synchronous 4-bit binary up/down counter	16	MSI	385
HC/HCT192	presettable synchronous BCD decade up/down counter	16	MSI	387
HC/HCT193	presettable synchronous 4-bit binary up/down counter	16	MSI	389
HC/HCT390	dual decade ripple counter	16	MSI	577
HC/HCT393	dual 4-bit binary ripple counter	14	MSI	579
HC/HCT4017	Johnson decade counter with 10 decoded outputs	16	MSI	688
HC/HCT4020	14-stage binary ripple counter	16	MSI	689
HC/HCT4024	7-stage binary ripple counter	14	MSI	690
HC/HCT4040	12-stage binary ripple counter	16	MSI	691

* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:
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type no.	description	pins	classification	page
Counters (continued)				
HC/HCT4059	programmable divide-by-n counter	24	MSI	712
HC/HCT4060	14-stage binary ripple counter with oscillator	16	MSI	715
HC/HCT4510	BCD up/down counter	16	MSI	746
HC/HCT4516	binary up/down counter	16	MSI	753
HC/HCT4518	dual synchronous BCD counter	16	MSI	754
HC/HCT4520	dual 4-bit synchronous binary counter	16	MSI	755
HC/HCT40102	8-bit synchronous BCD down counter	16	MSI	769
HC/HCT40103	8-bit binary down counter	16	MSI	771
Multiplexers				
HC/HCT151	8-input multiplexer	16	MSI	289
HC/HCT153	dual 4-input multiplexer	16	MSI	297
HC/HCT157	quad 2-input multiplexer	16	MSI	313
HC/HCT158	quad 2-input multiplexer; inverting	16	MSI	321
HC/HCT251	8-input multiplexer; 3-state	16	MSI	469
HC/HCT253*	dual 4-input multiplexer; 3-state	16	MSI	479
HC/HCT257*	quad 2-input multiplexer; 3-state	16	MSI	487
HC/HCT258	quad 2-input multiplexer; 3-state	16	MSI	494
HC/HCT354*	8-input multiplexer/register with transparent data latch; 3-state	20	MSI	541
HC/HCT356*	8-input multiplexer/register; 3-state	20	MSI	543
Decoders/demultiplexers				
HC/HCT42	BCD to decimal decoder (1-of-10)	16	MSI	176
HC/HCT137	1-to-8 line decoder/demultiplexer with address latches	16	MSI	263
HC/HCT138	3-to-8 line decoder/demultiplexer; inverting	16	MSI	265
HC/HCT139	dual 2-to-4 line decoder/demultiplexer	16	MSI	273
HC/HCT147	10-to-4 line priority encoder	16	MSI	281
HC/HCT154	4-to-16 line decoder/demultiplexer	24	MSI	305
HC/HCT237	1-to-8 line decoder/demultiplexer with address latches	16	MSI	412
HC/HCT238	3-to-8 line decoder/demultiplexer	16	MSI	413
HC/HCT4511	BCD to 7-segment latch/decoder/driver	16	MSI	747
HC/HCT4514	4-to-16 line decoder/demultiplexer with input latches	24	MSI	749
HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches	24	MSI	751
HC/HCT4543	BCD to 7-segment latch/decoder/driver for LCDs	16	MSI	757
Switches/multiplexers/demultiplexers				
HC/HCT4016	quad bilateral switches	14	SSI	679
HC/HCT4051	8-channel analog multiplexer/demultiplexer	16	MSI	701
HC/HCT4052	dual 4-channel analog multiplexer/demultiplexer	16	MSI	710
HC/HCT4053	triple 2-channel analog multiplexer/demultiplexer	16	MSI	711
HC/HCT4066	quad bilateral switches	14	SSI	727
HC/HCT4067	16-channel analog multiplexer/demultiplexer	24	SSI	729
HC/HCT4316	quad bilateral switches	16	MSI	739
HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch	18**	MSI	740
HC/HCT4352	dual 4-channel analog multiplexer/demultiplexer with latch	18**	MSI	742
HC/HCT4353	triple 2-channel analog multiplexer/demultiplexer with latch	18**	MSI	744

* Types with a bus-driver output stage.
** Also in SO-20 plastic mini-pack.

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; D = ceramic (cerdip) DIL; T = plastic SO mini-pack

type no.	description	pins	classification	page
Bus transceivers				
HC/HCT242*	quad bus transceiver; 3-state; inverting	14	MSI	437
HC/HCT243*	quad bus transceiver; 3-state	14	MSI	445
HC/HCT245*	octal bus transceiver; 3-state	20	MSI	461
HC/HCT640*	octal bus transceiver; 3-state; inverting	20	MSI	641
HC/HCT643*	octal bus transceiver; 3-state; true/inverting	20	MSI	649
HC/HCT646*	octal bus transceiver/register; 3-state	24	MSI	657
HC/HCT648*	octal bus transceiver/register; 3-state; inverting	24	MSI	659
Schmitt triggers				
HC/HCT14	hex inverting Schmitt trigger	14	SSI	158
HC/HCT132	quad 2-input NAND Schmitt trigger	14	SSI	255
One-shot multivibrators				
HC/HCT123	dual retriggerable monostable multivibrator with reset	16	MSI	243
HC/HCT221	dual retriggerable monostable multivibrator with reset	16	MSI	410
HC/HCT423	dual retriggerable monostable multivibrator with reset	16	MSI	587
HC/HCT4538	dual retriggerable precision monostable multivibrator	14	MSI	756
Miscellaneous				
HC/HCT297	digital phase-locked-loop filter	16	MSI	525
HC/HCT4046	phase-locked-loop with VCO	16	MSI	692
HC/HCT4046-1	phase-locked-loop with lock detector	16	MSI	695

* Types with a bus-driver output stage.

HCMOS PC54/74 FAMILY

type no.	description	page
HC/HCT00	quad 2-input NAND gate	121
HC/HCT02	quad 2-input NOR gate	129
HC/HCT03	quad 2-input NAND gate	136
HC/HCT04	hex inverter	137
HCU04	hex inverter (unbuffered)	145
HC/HCT08	quad 2-input AND gate	149
HC/HCT10	triple 3-input NAND gate	150
HC/HCT11	triple 3-input AND gate	151
HC/HCT14	hex inverting Schmitt trigger	158
HC/HCT20	dual 4-input NAND gate	159
HC/HCT21	dual 4-input AND gate	160
HC/HCT27	triple 3-input NOR gate	161
HC/HCT30	8-input NAND gate	168
HC/HCT32	quad 2-input OR gate	169
HC/HCT42	BCD to decimal decoder (1-of-10)	176
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger	177
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger	187
HC/HCT75	quad bistable transparent latch	197
HC/HCT85	4-bit magnitude comparator	207
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	215
HC/HCT93	4-bit binary ripple counter	222
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger	223
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	233
HC/HCT112	dual JK flip-flop with set and reset; negative-edge trigger	242
HC/HCT123	dual retriggerable monostable multivibrator with reset	243
HC/HCT125	quad buffer/line driver; 3-state	253
HC/HCT126	quad buffer/line driver; 3-state	254
HC/HCT132	quad 2-input NAND Schmitt trigger	255
HC/HCT137	1-to-8 line decoder/demultiplexer with address latches	263
HC/HCT138	3-to-8 line decoder/demultiplexer; inverting	265
HC/HCT139	dual 2-to-4 line decoder/demultiplexer	273
HC/HCT147	10-to-4 line priority encoder	281
HC/HCT151	8-input multiplexer	289
HC/HCT153	dual 4-input multiplexer	297
HC/HCT154	4-to-16 line decoder/demultiplexer	305
HC/HCT157	quad 2-input multiplexer	313
HC/HCT158	quad 2-input multiplexer; inverting	321
HC/HCT160	presettable synchronous BCD decade counter; asynchronous reset	328
HC/HCT161	presettable synchronous 4-bit binary counter; asynchronous reset	329
HC/HCT162	presettable synchronous BCD decade counter; synchronous reset	330

* Types with a bus driver output stage.

type no.	description	page
HC/HCT163	presettable synchronous 4-bit binary counter; synchronous reset	332
HC/HCT164	8-bit serial-in/parallel-out shift register	335
HC/HCT165	8-bit parallel-in/serial-out shift register	345
HC/HCT166	8-bit parallel-in/serial-out shift register	355
HC/HCT173*	quad D-type flip-flop; positive-edge trigger; 3-state	365
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger	367
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger	369
HC/HCT181	4-bit arithmetic logic unit	379
HC/HCT182	look-ahead carry generator	381
HC/HCT190	presettable synchronous BCD decade up/down counter	383
HC/HCT191	presettable synchronous 4-bit binary up/down counter	385
HC/HCT192	presettable synchronous BCD decade up/down counter	387
HC/HCT193	presettable synchronous 4-bit binary up/down counter	389
HC/HCT194	4-bit bidirectional universal shift register	391
HC/HCT195	4-bit parallel access shift register	401
HC/HCT221	dual retriggerable monostable multivibrator with reset	410
HC/HCT237	1-to-8 line decoder/demultiplexer with address latches	412
HC/HCT238	3-to-8 line decoder/demultiplexer	413
HC/HCT240*	octal buffer/line driver; 3-state; inverting	421
HC/HCT241*	octal buffer/line driver; 3-state	429
HC/HCT242*	quad bus transceiver; 3-state; inverting	437
HC/HCT243*	quad bus transceiver; 3-state	445
HC/HCT244*	octal buffer/line driver; 3-state	453
HC/HCT245*	octal bus transceiver; 3-state	461
HC/HCT251	8-input multiplexer; 3-state	469
HC/HCT253*	dual 4-input multiplexer; 3-state	479
HC/HCT257*	quad 2-input multiplexer; 3-state	487
HC/HCT258	quad 2-input multiplexer; 3-state	494
HC/HCT259	8-bit addressable latch	495
HC7266	quad 2-input EXCLUSIVE-NOR gate	505
HC/HCT273	octal D-type flip-flop with reset; positive-edge trigger	507
HC/HCT280	9-bit odd/even parity generator/checker	517
HC/HCT283	4-bit full adder with fast carry	524
HC/HCT297	digital phase-locked-loop filter	525
HC/HCT299*	8-bit universal shift register; 3-state	527
HC/HCT354*	8-input multiplexer/register with transparent data latch; 3-state	541
HC/HCT356*	8-input multiplexer/register; 3-state	543
HC/HCT365*	hex buffer/line driver with common enable; 3-state	545
HC/HCT366*	hex buffer/line driver with common enable; 3-state; inverting	546
HC/HCT367*	hex buffer/line driver; 3-state	547

* Types with a bus driver output stage.

type no.	description	page
HC/HCT368*	hex buffer/line driver; 3-state; inverting	548
HC/HCT373*	octal D-type transparent latch; 3-state	549
HC/HCT374*	octal D-type flip-flop; positive-edge trigger; 3-state	559
HC/HCT377	octal D-type flip-flop with data enable; positive-edge trigger	569
HC/HCT390	dual decade ripple counter	577
HC/HCT393	dual 4-bit binary ripple counter	579
HC/HCT423	dual retriggerable monostable multivibrator with reset	587
HC/HCT533*	octal D-type transparent latch; 3-state; inverting	597
HC/HCT534*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	607
HC/HCT540*	octal buffer/line driver; 3-state; inverting	617
HC/HCT541*	octal buffer/line driver; 3-state	618
HC/HCT563*	octal D-type transparent latch; 3-state; inverting	619
HC/HCT564*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	628
HC/HCT573*	octal D-type transparent latch; 3-state	629
HC/HCT574*	octal D-type flip-flop; positive-edge trigger; 3-state	638
HC/HCT583	4-bit full adder with fast carry	639
HC/HCD597	8-bit shift register with input latches	640
HC/HCT640*	octal bus transceiver; 3-state; inverting	641
HC/HCT643*	octal bus transceiver; 3-state; true/inverting	649
HC/HCT646*	octal bus transceiver/register; 3-state	657
HC/HCT648*	octal bus transceiver/register; 3-state; inverting	659
HC/HCT670	4 x 4 register file; 3-state	661
HC/HCT688	8-bit magnitude comparator	663
HC/HCT4002	dual 4-input NOR gate	671
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register	678
HC/HCT4016	quad bilateral switches	679
HC/HCT4017	Johnson decade counter with 10 decoded outputs	688
HC/HCT4020	14-stage binary ripple counter	689
HC/HCT4024	7-stage binary ripple counter	690
HC/HCT4040	12-stage binary ripple counter	691
HC/HCT4046	phase-locked-loop with VCO	692
HC/HCT4046-1	phase-locked-loop with lock detector	695
HC4049	hex inverting HIGH-to-LOW level shifter	698
HC4050	hex HIGH-to-LOW level shifter	699
HC/HCT4051	8-channel analog multiplexer/demultiplexer	701
HC/HCT4052	dual 4-channel analog multiplexer/demultiplexer	710
HC/HCT4053	triple 2-channel analog multiplexer/demultiplexer	711
HC/HCT4059	programmable divide-by-n counter	712
HC/HCT4060	14-stage binary ripple counter with oscillator	715
HC/HCT4066	quad bilateral switches	727

* Types with a bus driver output stage.

type no.	description	page
HC/HCT4067	16-channel analog multiplexer/demultiplexer	729
HC/HCT4075	triple 3-input OR gate	731
HC/HCT4094	8-stage shift-and-store bus register	738
HC/HCT4316	quad bilateral switches	739
HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch	740
HC/HCT4352	dual 4-channel analog multiplexer/demultiplexer with latch	742
HC/HCT4353	triple 2-channel analog multiplexer/demultiplexer with latch	744
HC/HCT4510	BCD up/down counter	746
HC/HCT4511	BCD to 7-segment latch/decoder/driver	747
HC/HCT4514	4-to-16 line decoder/demultiplexer with input latches	749
HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches	751
HC/HCT4516	binary up/down counter	753
HC/HCT4518	dual synchronous BCD counter	754
HC/HCT4520	dual 4-bit synchronous binary counter	755
HC/HCT4538	dual retriggerable precision monostable multivibrator	756
HC/HCT4543	BCD to 7-segment latch/decoder/driver for LCDs	757
HC/HCT40102	8-bit synchronous BCD down counter	769
HC/HCT40103	8-bit binary down counter	771
HC/HCT40104*	4-bit bidirectional universal shift register; 3-state	773
HC/HCT40105	4-bit x 16-word FIFO register	783

* Types with a bus driver output stage.

CROSS-REFERENCE 54/74 SERIES TTL TO HIGH-SPEED CMOS

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	74C	HC/HCT no.	FC	PC	function
00	00	00	Y	Y	quad 2-input NAND gate
02	02	02	Y	Y	quad 2-input NOR gate
03	-	03	Y	Y	quad 2-input NAND gate
04	04	04	Y	Y	hex inverter
05	-	-			hex inverter; open collector
08	08	08	Y	Y	quad 2-input AND gate
09	-	-			quad 2-input AND gate; open collector
10	10	10	Y	Y	triple 3-input NAND gate
11	-	11	Y	Y	triple 3-input AND gate
12	-	-			triple 3-input NAND gate; open collector
13	-	-			dual 4-input Schmitt trigger
14	14	14	Y	Y	hex inverting Schmitt trigger
15	-	-			triple 3-input AND gate; open collector
17	-	-			hex buffer driver; open collector; high voltage
18	-	-			dual 4-input Schmitt trigger
19	-	14	Y	Y	hex inverting Schmitt trigger
20	20	20	Y	Y	dual 4-input NAND gate
21	-	21	Y	Y	dual 4-input AND gate
22	-	-			dual 4-input NAND gate; open collector
24	-	132	Y	Y	quad 2-input NAND Schmitt trigger
26	-	-			quad 2-input NAND buffer; open collector
27	-	27	Y	Y	triple 3-input NOR gate
28	28	-			quad 2-input NOR buffer
30	30	30	Y	Y	8-input NAND gate
31	-	-			delay element
32	32	32	Y	Y	quad 2-input OR gate
33	-	-			quad 2-input NOR buffer; open collector
37	-	-			quad 2-input NAND buffer
38	-	-			quad 2-input NAND buffer; open collector
40	-	-			dual 4-input NAND buffer
42	42	42	Y	Y	BCD to decimal decoder (1-of-10)
47	-	-			BCD to 7-segment decoder/driver
48	-	4511	N	N	BCD to 7-segment latch/decoder/driver
49	-	4511	N	N	BCD to 7-segment latch/decoder/driver
51	-	-			dual 2-wide, 2-input/3-input AND-OR-INVERT gate
54	-	-			4-wide, 2-input AND-OR-INVERT gate
55	-	-			2-wide, 4-input AND-OR-INVERT gate
56	-	-			divider
57	-	-			divider
73	73	73	Y	Y	dual JK flip-flop with reset; negative-edge trigger
74	74	74	Y	Y	dual D-type flip-flop with set and reset; positive-edge trigger
75	-	75	Y	Y	quad bistable transparent latch
76	76	112	N	N	dual JK flip-flop with set and reset; negative-edge trigger
77	-	-			quad D-type latch
78	-	112	N	N	dual JK flip-flop with set and reset; negative-edge trigger

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	basic no. 74C	HC/HCT no.	FC	PC	function
83	83	-			4-bit binary full adder; fast carry
85	85	85	Y	Y	4-bit magnitude comparator
86	86	86	Y	Y	quad 2-input EXCLUSIVE-OR gate
89	89	-			64-bit RAM
90	90	-			decade counter
91	-	-			8-bit shift register; serial-in/serial-out
92	-	-			divide-by-12 counter
93	93	93	Y	Y	4-bit binary ripple counter
95	95	195	N	N	4-bit parallel access shift register
96	-	-			5-bit shift register
104	-	-			50 MHz counter
105	-	-			50 MHz counter
107	107	107	Y	Y	dual JK flip-flop with reset; negative-edge trigger
109	-	109	Y	Y	dual JK flip-flop with set and reset; positive-edge trigger
112	-	112	Y	Y	dual JK flip-flop with set and reset; negative-edge trigger
113	-	107	N	N	dual JK flip-flop with reset; negative-edge trigger
114	-	-			dual JK flip-flop; negative-edge trigger; common clocks and clear
122	-	-			retriggerable, resettable monostable multivibrator
123	-	123	Y	Y	dual retriggerable monostable multivibrator with reset
124	-	-			dual voltage-controlled oscillator
125	-	125	Y	Y	quad buffer/line driver; 3-state
126	-	126	Y	Y	quad buffer/line driver; 3-state
132	-	132	Y	Y	quad 2-input NAND Schmitt trigger
133	-	-			13-input NAND gate
136	-	-			quad 2-input EXCLUSIVE-OR gate; open collector
137	137	137	Y	Y	1-to-8 line decoder/demultiplexer with address latches
138	138	138	Y	Y	3-to-8 line decoder/demultiplexer; inverting
139	139	139	Y	Y	dual 2-to-4 line decoder/demultiplexer
145	-	-			1-to-10 decoder/driver; open collector
147	-	147	Y	Y	10-to-4 line priority encoder
148	-	-			8-to-3 line octal priority encoder
150	150	-			16-input multiplexer
151	151	151	Y	Y	8-input multiplexer
152	-	151	Y	N	8-input multiplexer
153	-	153	Y	Y	dual 4-input multiplexer
154	154	154	Y	Y	4-to-16 line decoder/demultiplexer
155	-	139	N	N	dual 2-to-4 line decoder/demultiplexer
156	-	-			dual 1-of-4 decoder/demultiplexer; open collector
157	157	157	Y	Y	quad 2-input multiplexer
158	-	158	Y	Y	quad 2-input multiplexer; inverting

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	basic no. 74C	HC/HCT no.	FC	PC	function
160	160	160	Y	Y	presettable synchronous BCD decade counter; asynchronous reset
161	161	161	Y	Y	presettable synchronous 4-bit binary counter; asynchronous reset
162	162	162	Y	Y	presettable synchronous BCD decade counter; synchronous reset
163	163	163	Y	Y	presettable synchronous 4-bit binary counter; synchronous reset
164	164	164	Y	Y	8-bit serial-in/parallel-out shift register
165	165	165	Y	Y	8-bit parallel-in/serial-out shift register
166	-	166	Y	Y	8-bit parallel-in/serial-out shift register
168	-	190	N	N	presettable synchronous BCD decade up/down counter
169	-	191	N	N	presettable synchronous 4-bit binary up/down counter
170	-	670	N	N	4 x 4 register file; 3-state
171	-	-			quad D-type flip-flop
173	173	173	Y	Y	quad D-type flip-flop; positive-edge trigger; 3-state
174	174	174	Y	Y	hex D-type flip-flop with reset; positive-edge trigger
175	175	175	Y	Y	quad D-type flip-flop with reset; positive-edge trigger
181	-	181	Y	Y	4-bit arithmetic logic unit
182	-	182	Y	Y	look-ahead carry generator
183	-	-			dual high speed adder
189	-	-			64-bit RAM
190	-	190	Y	Y	presettable synchronous BCD decade up/down counter
191	-	191	Y	Y	presettable synchronous 4-bit binary up/down counter
192	192	192	Y	Y	presettable synchronous BCD decade up/down counter
193	193	193	Y	Y	presettable synchronous 4-bit binary up/down counter
194	-	194	Y	Y	4-bit bidirectional universal shift register
195	195	195	Y	Y	4-bit parallel access shift register
196	-	-			presettable decade counter
197	-	-			presettable binary counter
200	200	-			256 x 1 RAM
211	-	-			16 x 9 RAM
212	-	-			16 x 9 RAM
213	-	-			16 x 12 RAM
214	-	-			1024 x 1 RAM
215	-	-			1024 x 1 RAM
216	-	-			64 x 4 RAM
217	-	-			64 x 4 RAM
218	-	-			32 x 8 RAM

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	basic no. 74C	HC/HCT no.	FC	PC	function
219	-	-			16 x 4 RAM
221	221	221	Y	Y	dual retriggerable monostable multivibrator with reset
222	-	40105	N	N	4-bit x 16-word FIFO register
224	-	40105	N	N	4-bit x 16-word FIFO register
227	-	40105	N	N	4-bit x 16-word FIFO register
228	-	40105	N	N	4-bit x 16-word FIFO register
237	237	237	Y	Y	1-to-8 line decoder/demultiplexer with address latches
238	238	238	Y	Y	3-to-8 line decoder/demultiplexer
239	239	-			quad 1-of-4 decoder/demultiplexer
240	240	240	Y	Y	octal buffer/line driver; 3-state; inverting
241	241	241	Y	Y	octal buffer/line driver; 3-state
242	242	242	Y	Y	quad bus transceiver; 3-state; inverting
243	243	243	Y	Y	quad bus transceiver; 3-state
244	244	244	Y	Y	octal buffer/line driver; 3-state
245	245	245	Y	Y	octal bus transceiver; 3-state
247	-	-			BCD to 7-segment decoder/driver; open collector
248	-	-			BCD to 7-segment decoder (with 2 kΩ pull-up resistors)
249	-	-			BCD to 7-segment decoder; open collector
251	-	251	Y	Y	8-input multiplexer; 3-state
253	-	253	Y	Y	dual 4-input multiplexer; 3-state
256	-	-			dual 4-bit addressable latch
257	-	257	Y	Y	quad 2-input multiplexer; 3-state
258	-	258	Y	Y	quad 2-input multiplexer; 3-state;
259	-	259	Y	Y	8-bit addressable latch
260	-	-			dual 5-input NOR gate
261	-	-			2-bit by 4-bit parallel binary multipliers
266	-	7266	N	Y	quad 2-input EXCLUSIVE-NOR gate
273	-	273	Y	Y	octal D-type flip-flop with reset; positive-edge trigger
275	-	-			7-bit slice Wallace trees
279	-	-			quad set-reset latch
280	-	280	Y	Y	9-bit odd/even parity generator/checker
283	-	283	Y	Y	4-bit binary full adder with fast carry
289	-	-			64-bit RAM
290	-	-			BCD decade counter
292	-	-			programmable frequency divider/digital timer
293	-	-			4-bit binary counter
294	-	-			programmable frequency divider/digital timer
295	-	195	N	N	4-bit parallel access shift register
297	-	297	Y	Y	digital phase-locked-loop filter
298	-	-			quad 2-port register
299	-	299	Y	Y	8-bit universal shift register; 3-state
311	-	-			16 x 9 RAM
312	-	-			16 x 9 RAM
314	-	-			1024 x 1 RAM
315	-	-			1024 x 1 RAM

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	basic no. 74C	HC/HCT no.	FC	PC	function
316	-	-			64 x 4 RAM
317	-	-			64 x 4 RAM
318	-	-			32 x 8 RAM
319	-	-			16 x 4 RAM
320	-	-			crystal-controlled oscillator
321	-	-			crystal-controlled oscillator
322	-	299	N	N	8-bit universal shift register; 3-state
323	-	-			8-bit universal shift/store register
324	-	-			voltage-controlled oscillator
325	-	-			dual voltage-controlled oscillator
326	-	-			dual voltage-controlled oscillator
327	-	-			dual voltage-controlled oscillator
328	-	-			dual voltage-controlled oscillator
333	-	-			field programmable logic sequencer
334	-	-			field programmable logic sequencer
335	-	-			field programmable logic sequencer
336	-	-			field programmable logic sequencer
340	-	240	Y	Y	octal buffer/line driver; 3-state; inverting
341	-	241	Y	Y	octal buffer/line driver; 3-state
344	-	244	Y	Y	octal buffer/line driver; 3-state
347	-	-			BCD to 7-segment decoder/ driver
348	-	-			8-line to 3-line priority encoder
352	-	153	N	N	dual 4-input multiplexer
353	-	253	N	N	dual 4-input multiplexer; 3-state
354	-	354	Y	Y	8-input multiplexer/register with transparent data latch; 3-state
355	-	354	N	N	8-input multiplexer/register with transparent data latch; 3-state
356	-	356	Y	Y	8-input multiplexer/register; 3-state
357	-	356	N	N	8-input multiplexer/register; 3-state
363	-	373	Y	Y	octal D-type transparent latch; 3-state
364	-	374	Y	Y	octal D-type flip flop; positive-edge trigger; 3-state
365	-	365	Y	Y	hex buffer/line driver with common enable; 3-state
366	-	366	Y	Y	hex buffer/line driver with common enable; 3-state; inverting
367	-	367	Y	Y	hex buffer/line driver; 3-state
368	-	368	Y	Y	hex buffer/line driver; 3-state; inverting
373	373	373	Y	Y	octal D-type transparent latch; 3-state
374	374	374	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state
375	-	75	Y	N	quad bistable transparent latch
377	-	377	Y	Y	octal D-type flip-flop with data enable; positive-edge trigger
378	-	174	N	N	hex D-type flip-flop with reset; positive-edge trigger
379	-	175	N	N	quad D-type flip-flop with reset; positive-edge trigger

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	basic no. 74C	HC/HCT no.	FC	PC	function
381	-	-			arithmetic logic unit/function generator
382	-	-			arithmetic logic unit/function generator
384	-	-			8-bit serial/parallel two's compliment multiplier
385	-	-			quad serial adder/subtractor
386	-	86	Y	N	quad 2-input EXCLUSIVE-OR gate
388	-	-			quad D-type flip-flop
390	-	390	Y	Y	dual decade ripple counter
393	-	393	Y	Y	dual 4-bit binary ripple counter
395	-	195	N	N	4-bit parallel access shift register
396	-	-			octal storage register
398	-	-			quad 2-input multiplexer
399	-	157	N	N	quad 2-input multiplexer
422	-	-			retriggerable monostable multivibrator
423	-	423	Y	Y	dual retriggerable monostable multivibrator with reset
424	-	-			clock generator and driver
440	-	-			quad tridirectional bus transceiver; open collector
441	-	-			quad tridirectional bus transceiver; inverting; open collector
442	-	-			quad tridirectional bus transceiver; 3-state
443	-	-			quad tridirectional bus transceiver; inverting; 3-state
444	-	-			quad tridirectional bus transceiver; true/inverting; 3-state
445	-	-			BCD to decimal decoder/driver
446	-	-			quad bus transceiver
447	-	-			BCD to 7-segment decoder/driver
448	-	-			quad tridirectional bus transceiver; true/inverting; open collector
449	-	-			quad bus transceiver
462	-	-			fibre optic transmitter
463	-	-			fibre optic transmitter
465	-	541	N	N	octal buffer/line driver; 3-state
466	-	540	N	N	octal buffer/line driver; 3-state; inverting
467	-	241	Y	N	octal buffer/line driver; 3-state
468	-	240	Y	N	octal buffer/line driver; 3-state; inverting
481	-	-			4-bit slice processor element
490	-	390	N	N	dual decade ripple counter
502	-	-			8-bit successive approximation register
503	-	-			8-bit successive approximation register
504	-	-			12-bit successive approximation register
533	533	533	Y	Y	octal D-type transparent latch; 3-state; inverting
534	534	534	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state; inverting
540	540	540	Y	Y	octal buffer/line driver; 3-state; inverting
541	-	541	Y	Y	octal buffer/line driver; 3-state

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	basic no. 74C	HC/HCT no.	FC	PC	function
544	-	240	N	N	octal buffer/line driver; 3-state; inverting
563	563	563	Y	Y	octal D-type transparent latch; 3-state; inverting
564	564	564	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state; inverting
568	-	190	N	N	presettable synchronous BCD decade up/down counter
569	-	191	N	N	presettable synchronous 4-bit binary up/down counter
573	573	573	Y	Y	octal D-type transparent latch; 3-state
574	574	574	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state
590	-	-			8-bit counter with output register
591	-	-			8-bit counter with output register
592	-	-			8-bit counter with input register
593	-	-			8-bit counter with input register
595	-	4094	N	N	8-stage shift-and-store bus register
596	-	4094	N	N	8-stage shift-and-store bus register
597	-	597	Y	Y	8-bit shift register with input latches
598	-	-			8-bit shift register with input latches
600	-	-			memory refresh controller
601	-	-			memory refresh controller
602	-	-			memory refresh controller
603	-	-			memory refresh controller
605	-	-			octal 2-input multiplexed latches
606	-	-			octal 2-input multiplexed latches
607	-	-			octal 2-input multiplexed latches
608	-	-			memory cycle controller
610	-	-			memory mapper
612	-	-			memory mapper
613	-	-			memory mapper
620	-	640	N	N	octal bus transceiver; 3-state; inverting
621	-	-			octal bus transceiver; open collector
622	-	-			octal bus transceiver; inverting; open collector
623	-	245	N	N	octal bus transceiver; 3-state
624	-	-			voltage-controlled oscillator
625	-	-			voltage-controlled oscillator
626	-	-			voltage-controlled oscillator
627	-	-			voltage-controlled oscillator
628	-	-			voltage-controlled oscillator
629	-	-			voltage-controlled oscillator
630	-	-			16-bit error detection and correction circuit
631	-	-			16-bit error detection and correction circuit
638	-	-			octal bus transceiver
639	-	-			octal bus transceiver

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	74C	HC/HCT no.	FC	PC	function
640	-	640	Y	Y	octal bus transceiver; 3-state; inverting
641	-	-			octal transceiver; open collector
642	-	-			octal inverting transceiver; open collector
643	-	643	Y	Y	octal bus transceiver; 3-state; true/inverting
644	-	-			octal true/inverting transceiver; open collector
645	-	245	Y	Y	octal bus transceiver; 3-state
646	-	646	Y	Y	octal bus transceiver/register; 3-state
647	-	-			octal transceiver/register; open collector
648	-	648	Y	Y	octal bus transceiver/register; 3-state; inverting
649	-	-			octal inverting transceiver/register; open collector
651	-	-			octal transceiver
652	-	-			octal transceiver
668	-	190	N	N	presettable synchronous BCD decade up/down counter
669	-	191	N	N	presettable synchronous 4-bit binary up/down counter
670	-	670	Y	Y	4 x 4 register file; 3-state
671	-	-			4-bit universal shift register/latch; 3-state
672	-	-			4-bit universal shift register/latch; 3-state
673	-	-			16-bit serial-in/serial-out shift register; 16-bit parallel storage out
674	-	-			16-bit parallel-in serial-out shift register
681	-	-			4-bit parallel binary accumulator
682	-	688	N	N	8-bit magnitude comparator
683	-	688	N	N	8-bit magnitude comparator
684	-	688	N	N	8-bit magnitude comparator
685	-	688	N	N	8-bit magnitude comparator
686	-	688	N	N	8-bit magnitude comparator
687	-	688	N	N	8-bit magnitude comparator
688	-	688	Y	Y	8-bit magnitude comparator
689	-	688	N	N	8-bit magnitude comparator
690	-	-			synchronous decade counter; asynchronous clear
691	-	-			synchronous 4-bit binary counter; asynchronous clear

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	basic no. 74C	HC/HCT no.	FC	PC	function
692	-	-			synchronous decade counter; synchronous clear
693	-	-			synchronous 4-bit binary counter; synchronous clear
696	-	-			synchronous up/down counter with output register and multiplexed outputs; 3-state
698	-	-			synchronous up/down counter with output register and multiplexed outputs; 3-state
699	-	-			synchronous up/down counter with output register and multiplexed outputs; 3-state
-	901	4049	N	N	hex inverting HIGH-to-LOW level shifter
-	902	4050	N	N	hex HIGH-to-LOW level shifter
-	903	-			hex P-MOS inverting buffer
-	904	-			hex P-MOS buffer
-	905	-			successive approximation register
-	906	-			hex buffer; open drain; active pull-down
-	907	-			hex buffer; open drain; active pull-up
-	908	-			quad high voltage driver; source 250 mA
-	909	-			quad linear comparator
-	910	-			64 x 4 RAM
-	911	-			4-digit display driver
-	912	-			6-digit display driver
-	914	14	N	N	hex inverting Schmitt trigger
-	915	-			7-segment to BCD converter/driver
-	917	-			6-digit hex display driver
-	918	-			dual high-voltage driver
-	920	-			256 x 4 RAM
-	921	-			256 x 4 RAM
-	922	-			keyboard encoder
-	923	-			keyboard encoder
-	925	-			4-decade counter, multiplexed outputs
-	926	-			4-decade counter, multiplexed outputs; carry at 6000
-	927	-			4-decade counter, multiplexed outputs; man count = 9599
-	928	-			4-decade counter, multiplexed outputs; man count = 1999
-	929	-			1024 x 1 RAM
-	930	-			1024 x 1 RAM
-	932	-			phase comparator
-	941	-			octal HIGH to LOW converter
-	945	-			4-digit up/down counter/latch decoder/ LCD driver
-	946	-			4 1/2-digit up/down counter/latch decoder/LCD driver
-	947	-			4-digit up/down counter/latch decoder/LCD driver
-	956	-			4-digit, 17-segment alphanumeric display driver with memory, decoder and LED drivers
-	989	-			16 x 4 RAM

CROSS-REFERENCE 4000 SERIES CMOS TO HIGH-SPEED CMOS

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic 4000 no.	HC no.	FC	PC	function
4000	-	-	-	dual 3-input NOR gate and inverter
4001	02	Y	N	quad 2-input NOR gate
4002	4002	Y	Y	dual 4-input NOR gate
4006	-			18-stage static shift register
4007	-			dual complementary pair and inverter
4008	-			4-bit binary full adder
4009	-			hex buffer/converter; inverting
4010	-			hex buffer/converter
4011	00	Y	N	quad 2-input NAND gate
4012	20	Y	N	dual 4-input NAND gate
4013	74	Y	N	dual D-type flip-flop with set and reset; positive-edge trigger
4014	-			8-bit static shift register
4015	4015	Y	Y	dual 4-bit serial-in/parallel-out shift register
4016	4016/4316	Y	Y	quad bilateral switches
4017	4017	Y	Y	Johnson decade counter with 10 decoded outputs
4018	-			presettable divide-by-n counter
4019	157	N	N	quad 2-input multiplexer
4020	4020	Y	Y	14-stage binary ripple counter
4021	166	N	N	8-bit parallel-in/serial-out shift register
4022	-			4-stage divide-by-8 Johnson counter
4023	10	Y	N	triple 3-input NAND gate
4024	4024	Y	Y	7-stage binary ripple counter
4025	27	Y	N	triple 3-input NOR gate
4026	-			decoded counter/divider with 7-segment outputs
4027	109	Y	N	dual JK$^-$ flip-flop with set and reset; positive-edge trigger
4028	42	Y	N	BCD to decimal decoder (1-of-10)
4029	-			synchronous up/down - binary/decade counter
4030	86	Y	N	quad 2-input EXCLUSIVE-OR gate
4031	-			64-stage static shift register
4032	-			triple serial adder, positive logic
4033	-			decoder counter/divider with 7-segment outputs; ripple blanking
4034	-			8 stage static bidirectional parallel/serial input/output bus register
4035	-			4-bit universal shift register
4037	-			triple AND/OR bi-phase pair
4038	-			triple serial adder; negative logic
4040	4040	Y	Y	12-stage binary ripple counter
4041	-			quad true/complement buffer
4042	-			quad D-latch
4043	-			quad R/S latch; 3-state
4044	-			quad R/S latch; 3-state
4045	-			21-stage counter
4046	4046	Y	Y	phase-locked-loop with VCO
4047	-			monostable/astable multivibrator
4048	-			multi-function expandable 8-input
4049	4049	Y	Y	hex inverting HIGH-to-LOW level shifter

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic 4000 no.	HC no.	FC	PC	function
4050	4050	Y	Y	hex HIGH-to-LOW level shifter
4051	4051/4351	Y	Y	8-channel analog multiplexer/demultiplexer
4052	4052/4352	Y	Y	dual 4-channel analog multiplexer/ demultiplexer
4053	4053/4353	Y	Y	triple 2-channel analog multiplexer/ demultiplexer
4054	-			4-segment LCD driver
4055	4543	N	N	BCD to 7-segment latch/decoder/driver for LCDs
4056	-			BCD to 7-segment decoder/driver with strobed latch function; LCD driver
4057	-			4-bit arithmetic logic unit
4059	4059	Y	Y	programmable divide-by-n counter
4060	4060	Y	Y	14-stage binary ripple counter with oscillator
4062	-			200-stage dynamic shift register
4063	85	N	N	4-bit magnitude comparator
4066	4066	Y	Y	quad bilateral switches
4067	4067	Y	Y	16-channel analog multiplexer/demultiplexer
4068	-			8-input NAND gate
4069	04	Y	Y	hex inverter
4070	86	Y	N	quad 2-input EXCLUSIVE-OR gate
4071	32	Y	N	quad 2-input OR gate
4072	-			dual 4-input OR gate
4073	11	Y	N	triple 3-input AND gate
4075	4075	Y	Y	triple 3-input OR gate
4076	173	Y	Y	quad D-type flip-flop; positive-edge trigger; 3-state
4077	-			quad EXCLUSIVE-NOR gate
4078	-			8-input NOR gate
4081	08	Y	N	quad 2-input AND gate
4082	-			dual 4-input AND gate
4085	-			dual 2-wide 2-input AND-OR-INVERT gate
4086	-			4-wide 2-input AND-OR-INVERT gate
4089	-			binary rate multiplier
4093	132	Y	N	quad 2-input NAND Schmitt trigger
4094	4094	Y	Y	8-stage shift-and-store bus register
4095	-			gated JK master slave flip-flop
4096	-			gated JK master slave flip-flop; inverting and non-inverting inputs
4097	-			differential 8-channel multiplexer/ demultiplexer
4098	423	Y	N	dual retriggerable monostable multivibrator with reset
4099	259	N	N	8-bit addressable latch
4500	-			industrial control unit
4501	-			triple gate
4502	368	N	N	hex buffer/line driver; 3-state; inverting
4503	367	Y	Y	hex buffer/line driver; 3-state
4504	-			hex LOW-to-HIGH level shifter
4505	-			64-bit static read/write RAM
4506	-			dual expandable AND-OR-INVERT gate
4507	86	Y	N	quad 2-input EXCLUSIVE-OR gate
4508	-			dual 4-bit latch

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic 4000 no.	HC no.	FC	PC	function
4510	4510	Y	Y	BCD up/down counter
4511	4511	Y	Y	BCD to 7-segment latch/decoder/driver
4512	251	N	N	8-input multiplexer; 3-state
4513	-			BCD to 7-segment latch/decoder/driver; ripple blanking
4514	4514	Y	Y	4-to-16 line decoder/demultiplexer with input latches
4515	-			4-to-16 decoder/demultiplexer with input latches
4516	4516	Y	Y	binary up/down counter
4517	-			dual 64-bit static shift register
4518	4518	Y	Y	dual synchronous BCD counter
4519	157	N	N	quad 2-input multiplexer
4520	4520	Y	Y	dual 4-bit synchronous binary counter
4521	-			24-stage frequency divider
4522	-			programmable 4-bit BCD down counter
4524	-			256 x 4 ROM
4526	-			programmable 4-bit binary down counter
4527	-			BCD rate multiplier
4528	423	N	N	dual retriggerable monostable multivibrator with reset
4529	4052	N	N	dual 4-channel analog multiplexer/ demultiplexer
4530	-			dual 5-input majority logic gate
4531	-			13-input parity checker/generator
4532	-			8-input priority encoder
4534	-			real time 5-decade counter
4536	-			programmable timer
4537	-			256 x 1 static RAM
4538	4538	Y	Y	dual retriggerable precision monostable multivibrator
4539	4052	N	N	dual 4-channel analog multiplexer/ demultiplexer
4541	-			programmable timer
4543	4543	Y	Y	BCD to 7-segment latch/decoder/driver for LCDs
4544	-			BCD to 7-segment decoder/driver/latch; ripple blanking
4547	-			BCD to 7-segment decoder/driver/latch; high current
4549	-			successive approximation register
4551	-			quad 2-channel analog multiplexer
4552	-			64 x 4 static RAM
4553	-			3-digit BCD counter
4554	-			2 x 2-bit binary multiplier
4555	139	Y	Y	dual 2-to-4 line decoder/demultiplexer
4556	-			dual 1-of-4 decoder/demultiplexer; inverting
4557	-			1-to-64 bit variable length shift register
4558	-			BCD to 7-segment decoder
4559	-			successive approximation register
4560	-			NBCD adder
4561	-			9's complementer
4562	-			128-bit static shift register
4566	-			time base generator
4568	-			phase comparator, programmable counter

FC = function compatible; PC = pin compatible; Y = yes; N = no

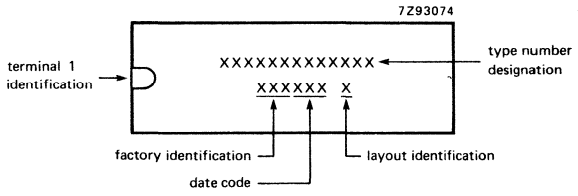
basic 4000 no.	HC no.	FC	PC	function
4569	-			dual programmable BCD/binary counter
4572	-			hex gate
4580	-			4 x 4 multiport register
4581	-			4-bit arithmetic logic unit
4582	-			look-ahead carry generator
4583	-			dual Schmitt trigger
4584	14	Y	Y	hex inverting Schmitt trigger
4585	85	Y	Y	4-bit magnitude comparator
4597	-			8-bit bus-compatible counter/latch
4598	-			8-bit bus-compatible addressable latch
4599	-			8-bit addressable latch
40097	367	Y	Y	hex buffer/line driver; 3-state
40098	368	Y	Y	hex buffer/line driver; 3-state; inverting
40100	-			32-stage left/right shift register
40101	280	N	N	9-bit odd/even parity generator/checker
40102	40102	Y	Y	8-bit synchronous BCD down counter
40103	40103	Y	Y	8-bit binary down counter
40104	40104	Y	Y	4-bit bidirectional universal shift register; 3-state
40105	40105	Y	Y	4-bit x 16-word FIFO register
40106	14	Y	Y	hex inverting Schmitt trigger
40107	-			dual 2-input NAND buffer/driver
40108	-			4 x 4 multiport register
40109	-			quad LOW-to-HIGH level shifter
40110	-			decade up/down counter/decoder/latch/driver
40115	-			8-bit universal bidirectional CMOS/TTL level converter
40116	-			8-bit universal bidirectional CMOS/TTL level converter
40147	174	Y	Y	hex D-type flip-flop with reset; positive-edge trigger
40160	160	Y	Y	presettable synchronous BCD decade counter; asynchronous reset
40161	161	Y	Y	presettable synchronous 4-bit binary counter; asynchronous reset
40162	162	Y	Y	presettable synchronous BCD decade counter; synchronous reset
40163	163	Y	Y	presettable synchronous 4-bit binary counter; synchronous reset
40174	174	Y	Y	hex D-type flip-flop with reset; positive-edge trigger
40175	175	Y	Y	quad D-type flip-flop with reset; positive-edge trigger
40181	-			4-bit arithmetic logic unit
40182	-			look-ahead carry generator
40192	192	Y	Y	presettable synchronous BCD decade up/down counter
40193	193	Y	Y	presettable synchronous 4-bit binary up/down counter
40194	194	Y	Y	4-bit bidirectional universal shift register
40208	-			4 x 4 multiport register
40240	240	Y	Y	octal buffer/line driver; 3-state; inverting
40244	244	Y	Y	octal buffer/line driver; 3-state
40245	245	Y	Y	octal bus transceiver; 3-state
40373	373	Y	Y	octal D-type transparent latch; 3-state
40374	374	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state

ORDERING INFORMATION

TYPE NUMBER DESIGNATIONS

PC XX XXX XXXXX X

- X — package code: P = plastic; D = ceramic (cerdip); T = plastic mini-pack (SO)
- XXXXX — device number (up to 5 digits)
- XXX — HC = CMOS input switching levels; supply voltage range 2 to 6 V; fully buffered
- XXX — HCT = TTL input switching levels; supply voltage range 4.5 V to 5.5 V, fully buffered
- XXX — HCU = CMOS input switching levels; supply voltage range 2 to 6 V; unbuffered (single-stage devices)
- XX — 74 = standard temperature range: -40 to +85 °C
- XX — 54 = extended temperature range: -55 to +125 °C; (cerdip only)
- PC — PC = family identification (high-speed CMOS)



ORDERING

N (a) integrated circuits PC74 (b) HC (c) 643 P (d) B (e)

Complete type number (example): PC74HC643PB

a: quantity
b: operating temperature range (74 or 54)
c: subdivision (HC, HCT, HCU)
d: package code, D = ceramic (cerdip); P = plastic; T = plastic SO mini-pack
e: screening class, burn-in (optional)

RATING SYSTEMS

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device.

An electronic tube or valve, transistor or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and similar components.

Characteristic

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those charactersistics which are directly related to the application.

Rating

A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note: Limiting conditions may be either maxima or minima.

Rating system

The set of principles upon which ratings are established and which determine their interpretation.

Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

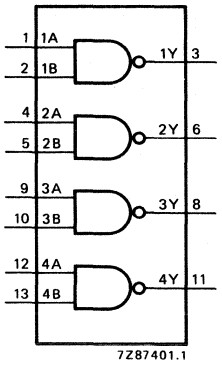
Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

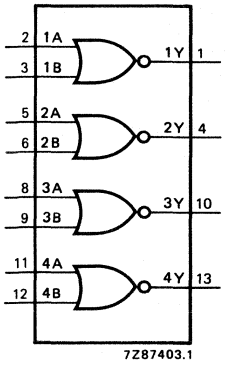
LOGIC SYMBOLS

HC/HCT00



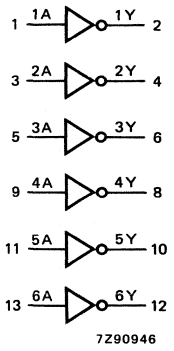
Quad 2-input NAND gate

HC/HCT02



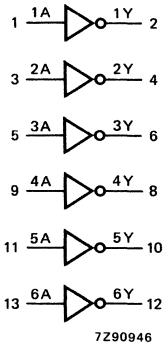
Quad 2-input NOR gate

HC/HCT04



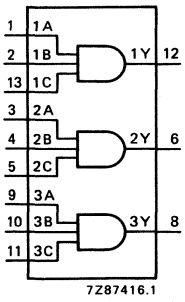
Hex inverter

HCU04



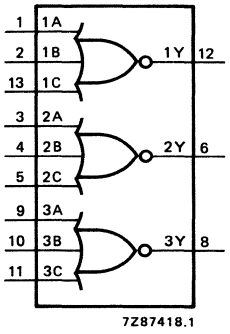
Hex inverter (unbuffered)

HC/HCT11



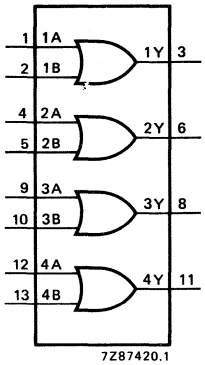
Triple 3-input AND gate

HC/HCT27



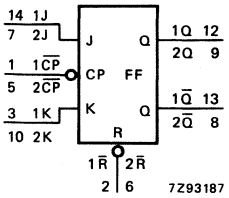
Triple 3-input NOR gate

HC/HCT32



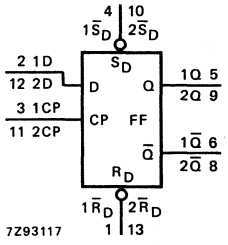
Quad 2-input OR gate

HC/HCT73



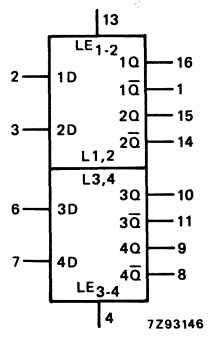
Dual JK flip-flop with reset; negative-edge trigger

HC/HCT74



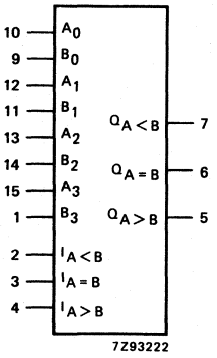
Dual D-type flip-flop with set and reset; positive-edge trigger

HC/HCT75



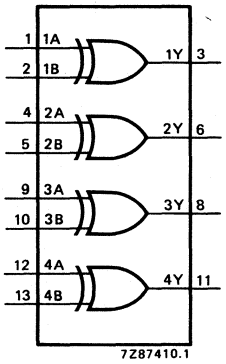
Quad bistable transparent latch

HC/HCT85



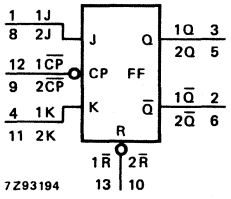
4-bit magnitude comparator

HC/HCT86



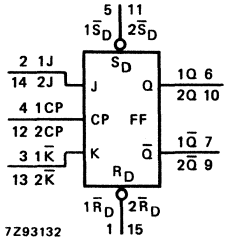
Quad 2-input EXCLUSIVE –OR gate

HC/HCT107



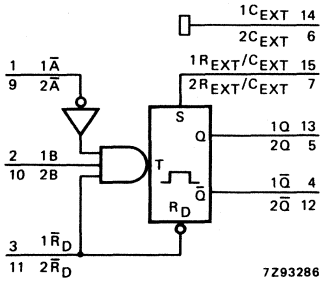
Dual JK flip-flop with reset; negative-edge trigger

HC/HCT109



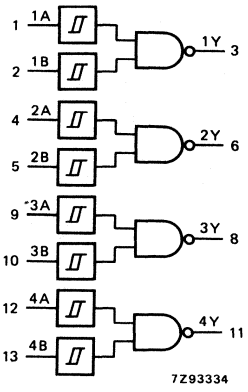
Dual $J\bar{K}$ flip-flop with set and reset; positive-edge trigger

HC/HCT123



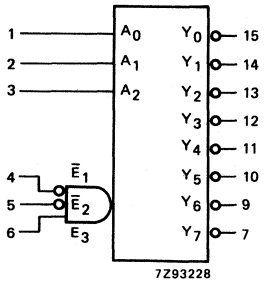
Dual retriggerable monostable multivibrator with reset

HC/HCT132



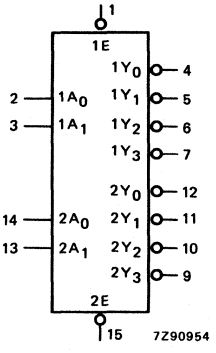
Quad 2-input NAND Schmitt trigger

HC/HCT138



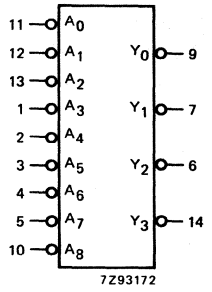
3-to-8 line decoder/demultiplexer; inverting

HC/HCT139



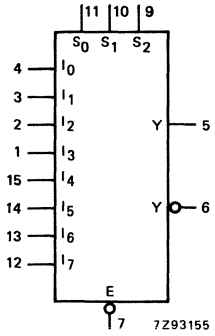
Dual 2-to-4 line decoder/ demultiplexer

HC/HCT147



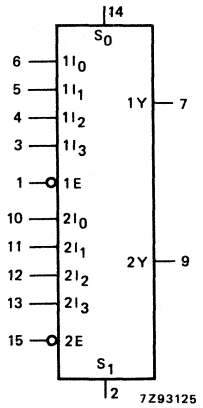
10-to-4 line priority encoder

HC/HCT151



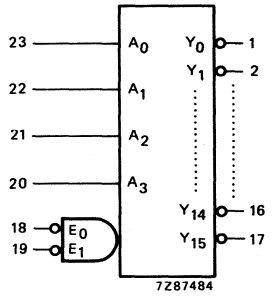
8-input multiplexer

HC/HCT153



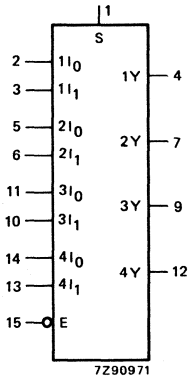
Dual 4-input multiplexer

HC/HCT154



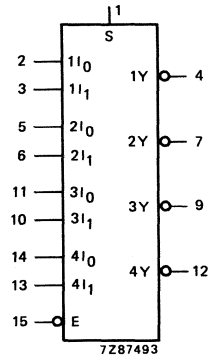
4-to-16 line decoder/
demultiplexer

HC/HCT157



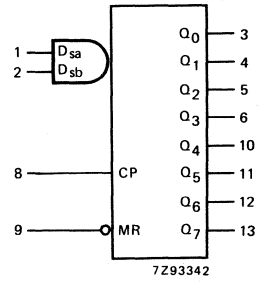
Quad 2-input multiplexer

HC/HCT158



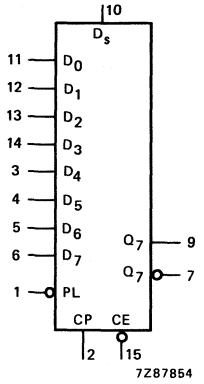
Quad 2-input multiplexer;
inverting

HC/HCT164



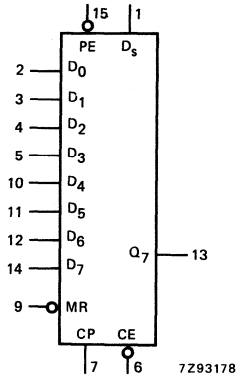
8-bit serial-in/parallel-out shift
register

HC/HCT165



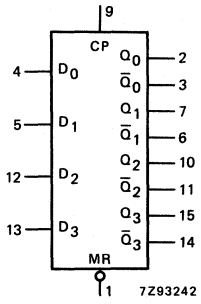
8-bit parallel-in/serial-out shift
register

HC/HCT166



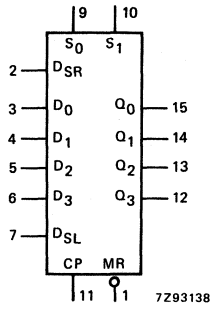
8-bit parallel-in/serial-out shift
register

HC/HCT175



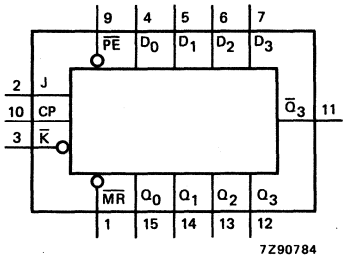
Quad D-type flip-flop with reset; positive-edge trigger

HC/HCT194



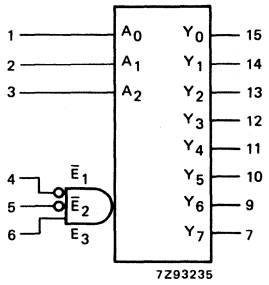
4-bit bidirectional universal shift register

HC/HCT195



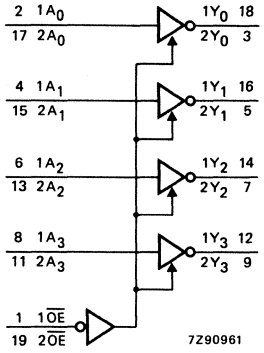
4-bit parallel access shift register

HC/HCT238



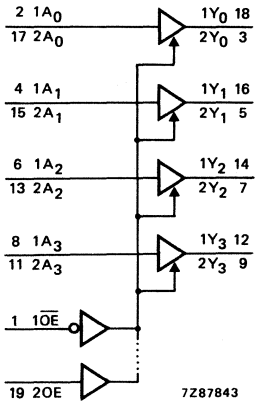
3-to-8 line decoder/demultiplexer

HC/HCT240



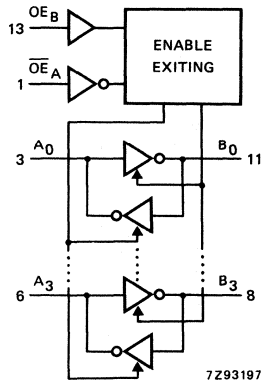
Octal buffer/line driver; 3-state; inverting

HC/HCT241



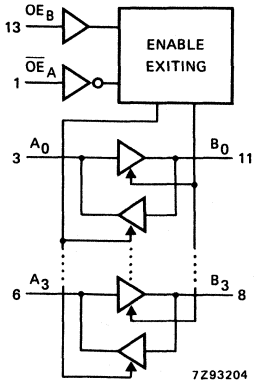
Octal buffer/line driver; 3-state

HC/HCT242



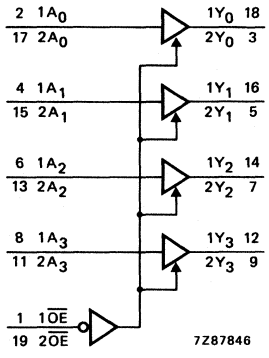
Quad bus transceiver; 3-state; inverting

HC/HCT243



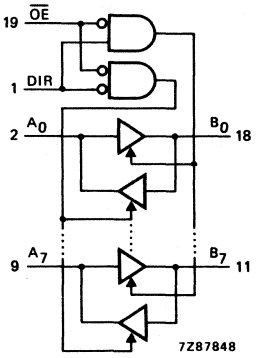
Quad bus transceiver; 3-state

HC/HCT244



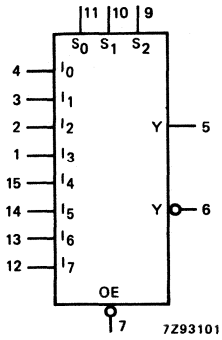
Octal buffer/line driver; 3-state

HC/HCT245



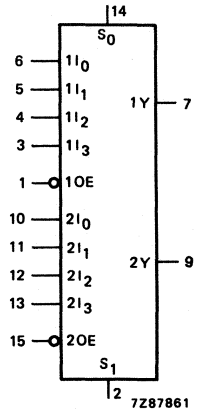
Octal bus transceiver; 3-state

HC/HCT251



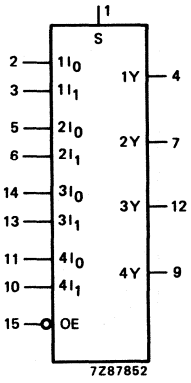
8-input multiplexer; 3-state

HC/HCT253



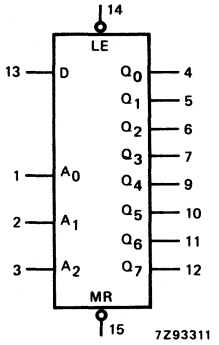
Dual 4-input multiplexer; 3-state

HC/HCT257



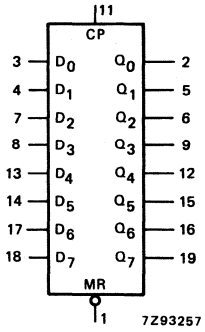
Quad 2-input multiplexer; 3-state

HC/HCT259



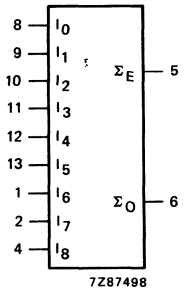
8-bit addressable latch

HC/HCT273



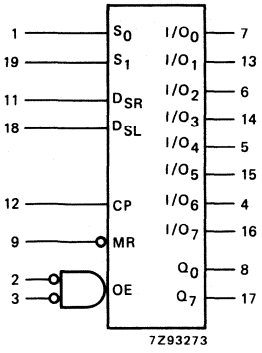
Octal D-type flip-flop with reset; positive-edge trigger

HC/HCT280



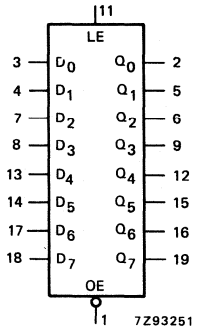
9-bit odd/even parity generator/checker

HC/HCT299



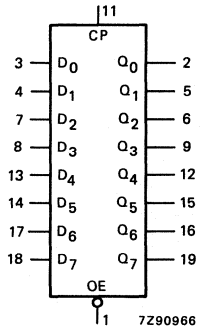
8-bit universal shift register; 3-state

HC/HCT373



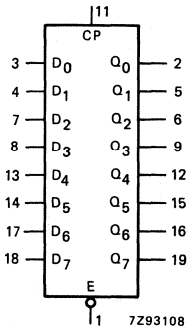
Octal D-type transparent latch; 3-state

HC/HCT374



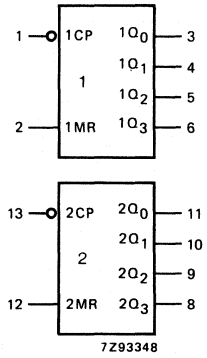
Octal D-type flip-flop; positive-edge trigger; 3-state

HC/HCT377



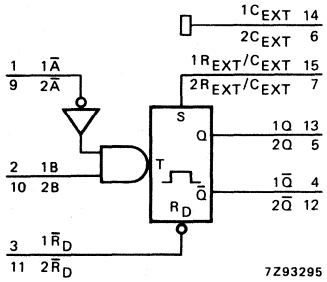
Octal D-type flip-flop with data enable; positive-edge trigger

HC/HCT393



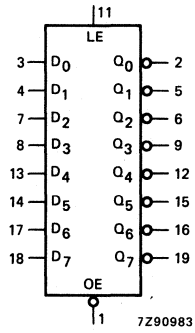
Dual 4-bit binary ripple counter

HC/HCT423



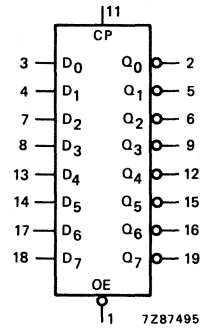
Dual retriggerable monostable multivibrator with reset

HC/HCT533



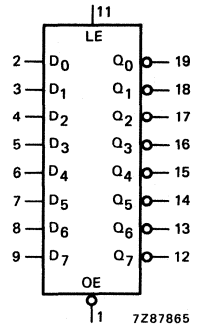
Octal D-type transparent latch; 3-state; inverting

HC/HCT534



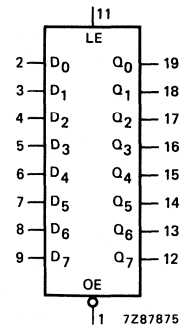
Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

HC/HCT563



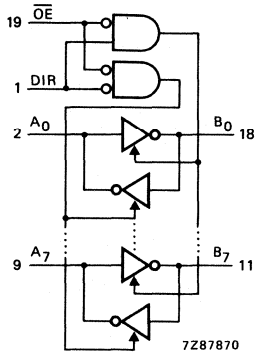
Octal D-type transparent latch; 3-state; inverting

HC/HCT573



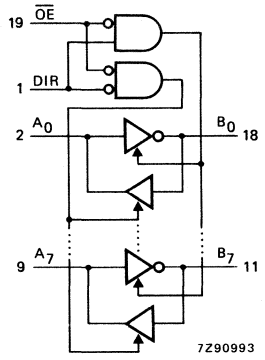
Octal D-type transparent latch; 3-state

HC/HCT640



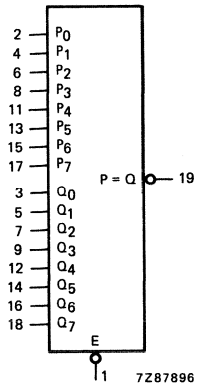
Octal bus transceiver; 3-state; inverting

HC/HCT643



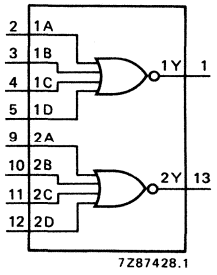
Octal bus transceiver; 3-state; true/inverting

HC/HCT688



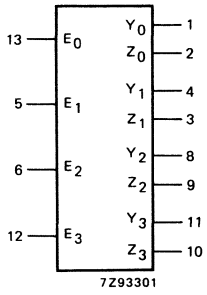
8-bit magnitude comparator

HC/HCT4002



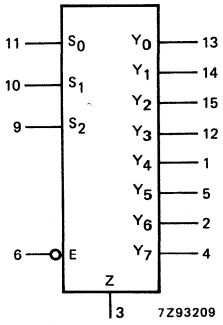
Dual 4-input NOR gate

HC/HCT4016



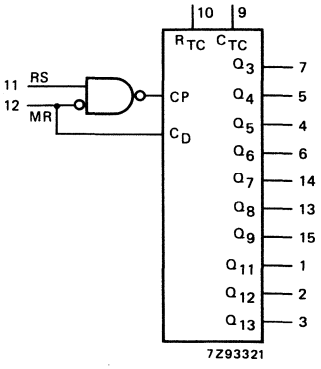
Quad bilateral switches

HC/HCT4051



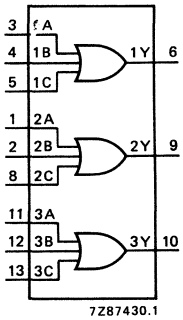
8-channel analog multiplexer/ demultiplexer

HC/HCT4060



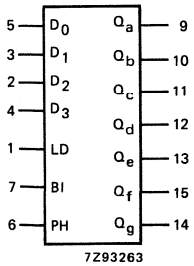
14-stage binary ripple counter with oscillator

HC/HCT4075



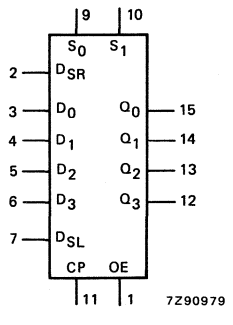
Triple 3-input OR gate

HC/HCT4543



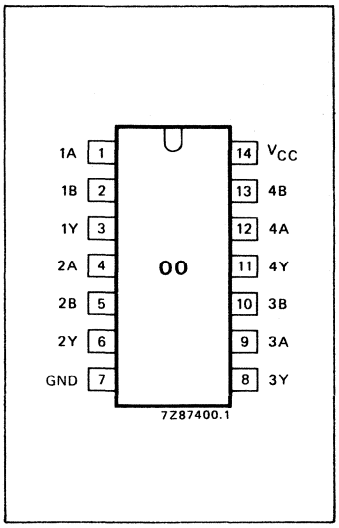
BCD to 7-segment latch/decoder/ driver for LCDs

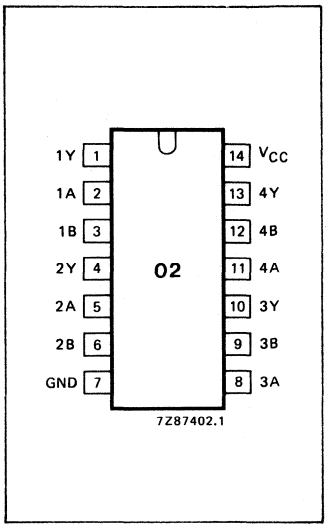
HC/HCT40104

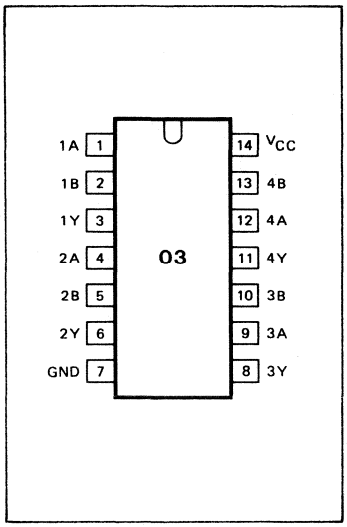


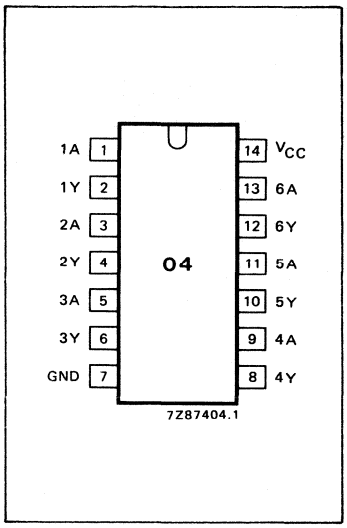
4-bit bidirectional universal shift register; 3-state

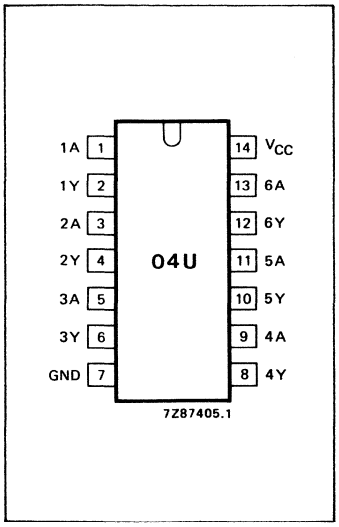
PIN CONFIGURATIONS

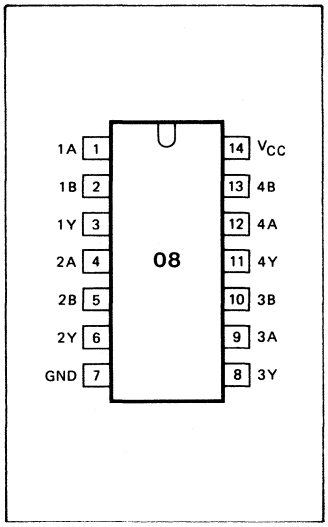

00
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z87400.1

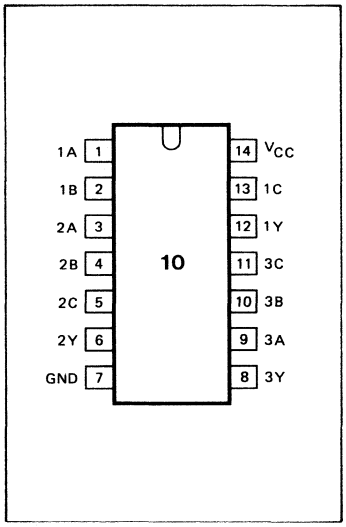

02
1Y 1
1A 2
1B 3
2Y 4
2A 5
2B 6
GND 7
14 VCC
13 4Y
12 4B
11 4A
10 3Y
9 3B
8 3A
7Z87402.1

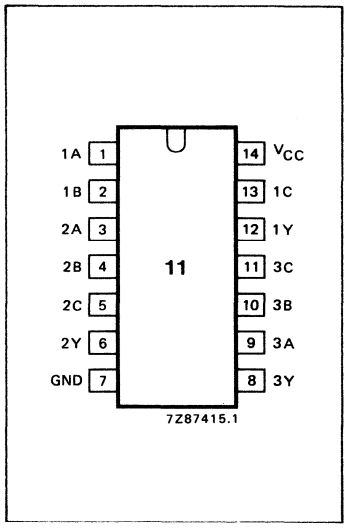

03
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y

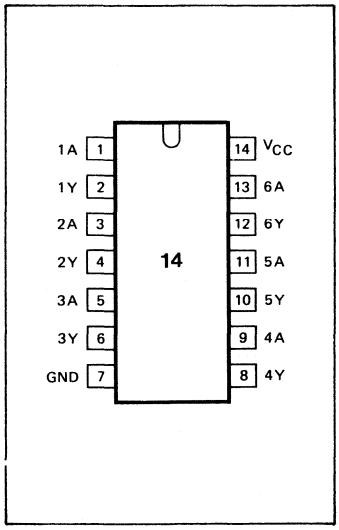

04
1A 1
1Y 2
2A 3
2Y 4
3A 5
3Y 6
GND 7
14 VCC
13 6A
12 6Y
11 5A
10 5Y
9 4A
8 4Y
7Z87404.1

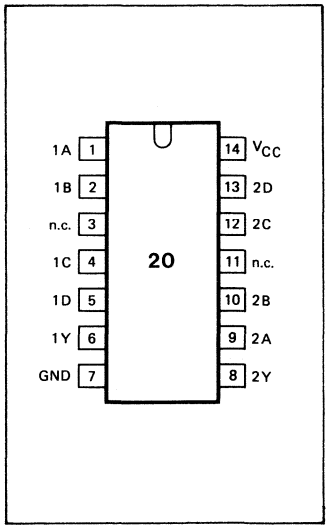

04U
1A 1
1Y 2
2A 3
2Y 4
3A 5
3Y 6
GND 7
14 VCC
13 6A
12 6Y
11 5A
10 5Y
9 4A
8 4Y
7Z87405.1

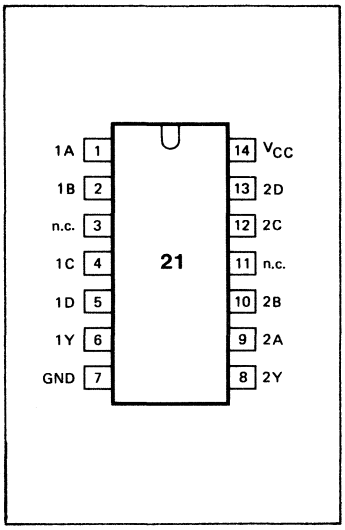

08
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y

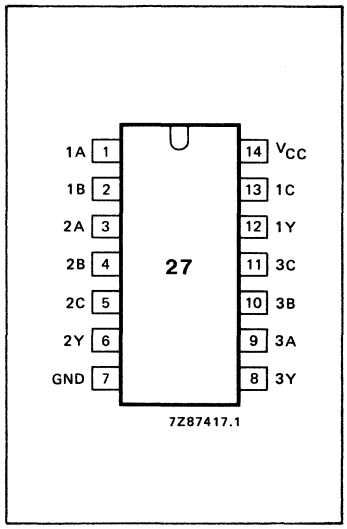

10
1A 1
1B 2
2A 3
2B 4
2C 5
2Y 6
GND 7
14 VCC
13 1C
12 1Y
11 3C
10 3B
9 3A
8 3Y

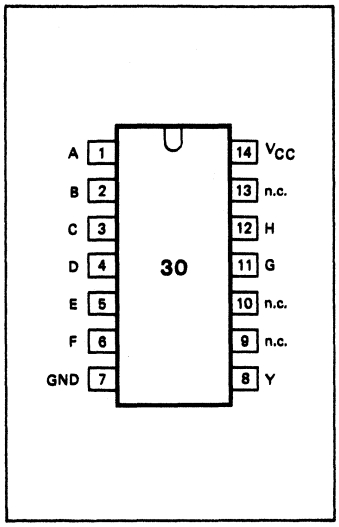

11
1A 1
1B 2
2A 3
2B 4
2C 5
2Y 6
GND 7
14 VCC
13 1C
12 1Y
11 3C
10 3B
9 3A
8 3Y
7Z87415.1

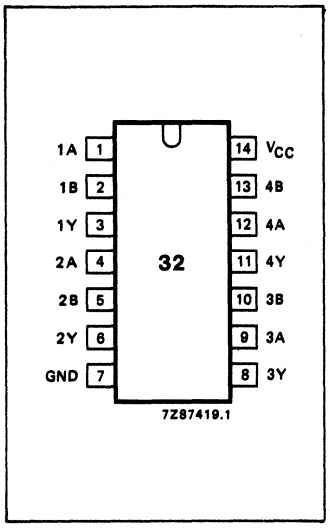

14
1A 1
1Y 2
2A 3
2Y 4
3A 5
3Y 6
GND 7
14 VCC
13 6A
12 6Y
11 5A
10 5Y
9 4A
8 4Y

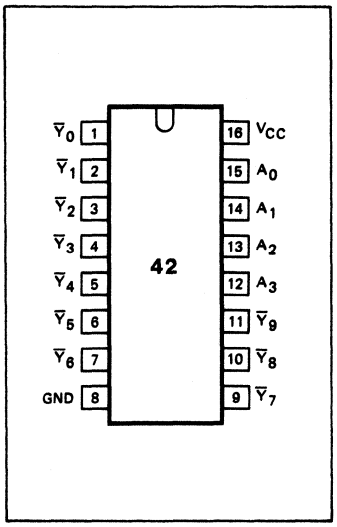

20
1A 1
1B 2
n.c. 3
1C 4
1D 5
1Y 6
GND 7
14 VCC
13 2D
12 2C
11 n.c.
10 2B
9 2A
8 2Y

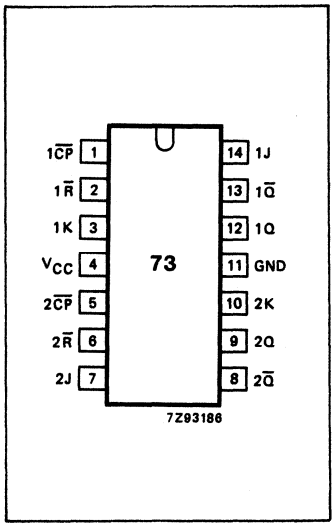

21
1A 1
1B 2
n.c. 3
1C 4
1D 5
1Y 6
GND 7
14 VCC
13 2D
12 2C
11 n.c.
10 2B
9 2A
8 2Y

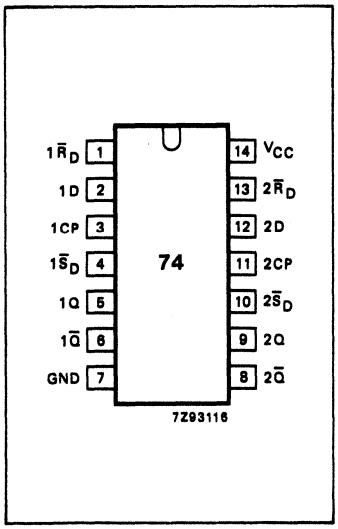

27
1A 1
1B 2
2A 3
2B 4
2C 5
2Y 6
GND 7
14 VCC
13 1C
12 1Y
11 3C
10 3B
9 3A
8 3Y
7Z87417.1

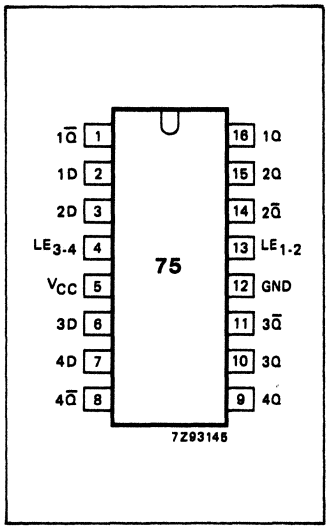

30
A 1
B 2
C 3
D 4
E 5
F 6
GND 7
14 VCC
13 n.c.
12 H
11 G
10 n.c.
9 n.c.
8 Y

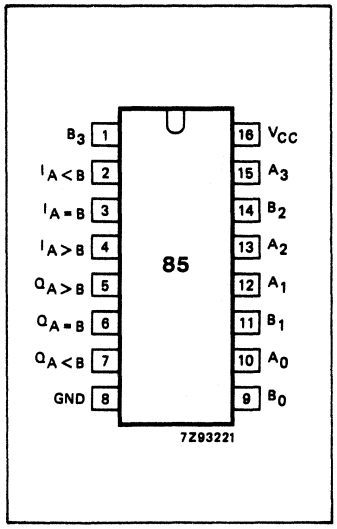

32
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z87419.1

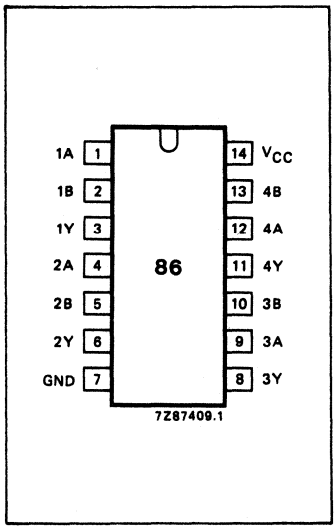

42
$\overline{Y}_0$ 1
$\overline{Y}_1$ 2
$\overline{Y}_2$ 3
$\overline{Y}_3$ 4
$\overline{Y}_4$ 5
$\overline{Y}_5$ 6
$\overline{Y}_6$ 7
GND 8
16 VCC
15 A_0
14 A_1
13 A_2
12 A_3
11 $\overline{Y}_9$
10 $\overline{Y}_8$
9 $\overline{Y}_7$

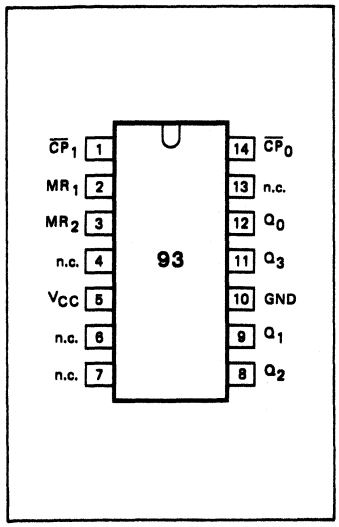

73
1$\overline{CP}$ 1
1$\overline{R}$ 2
1K 3
VCC 4
2$\overline{CP}$ 5
2$\overline{R}$ 6
2J 7
14 1J
13 1$\overline{Q}$
12 1Q
11 GND
10 2K
9 2Q
8 2$\overline{Q}$
7Z93186

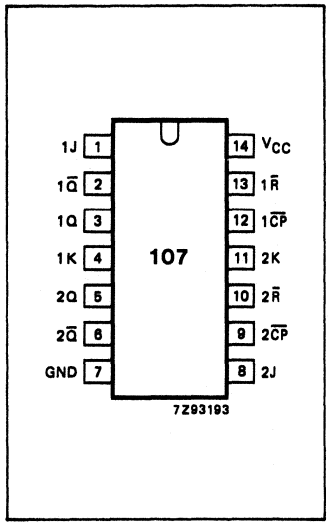

74
1$\overline{R}_D$ 1
1D 2
1CP 3
1$\overline{S}_D$ 4
1Q 5
1$\overline{Q}$ 6
GND 7
14 VCC
13 2$\overline{R}_D$
12 2D
11 2CP
10 2$\overline{S}_D$
9 2Q
8 2$\overline{Q}$
7Z93116

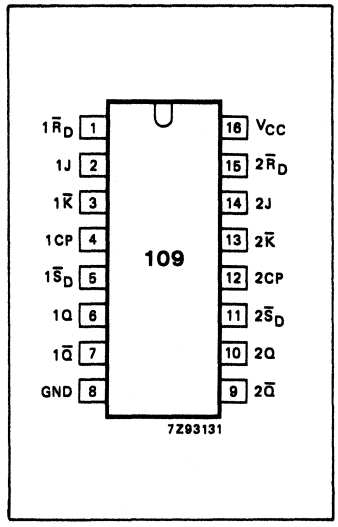

75
1$\overline{Q}$ 1
1D 2
2D 3
LE_{3-4} 4
VCC 5
3D 6
4D 7
4$\overline{Q}$ 8
16 1Q
15 2Q
14 2$\overline{Q}$
13 LE_{1-2}
12 GND
11 3$\overline{Q}$
10 3Q
9 4Q
7Z93145

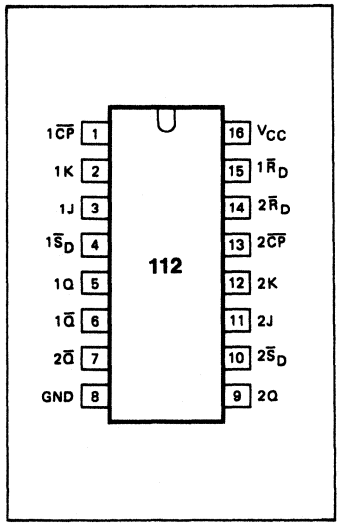

85
B_3 1
$I_{A<B}$ 2
$I_{A=B}$ 3
$I_{A>B}$ 4
$Q_{A>B}$ 5
$Q_{A=B}$ 6
$Q_{A<B}$ 7
GND 8
16 VCC
15 A_3
14 B_2
13 A_2
12 A_1
11 B_1
10 A_0
9 B_0
7Z93221

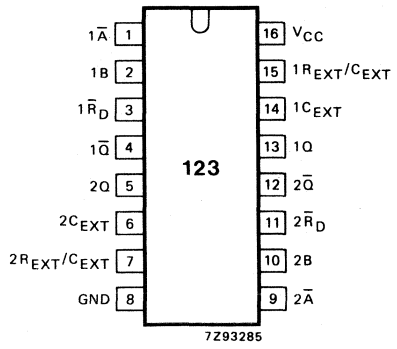

86
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z87409.1

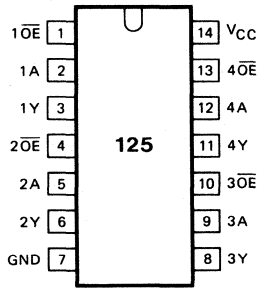

93
$\overline{CP}_1$ 1
MR_1 2
MR_2 3
n.c. 4
VCC 5
n.c. 6
n.c. 7
14 $\overline{CP}_0$
13 n.c.
12 Q_0
11 Q_3
10 GND
9 Q_1
8 Q_2

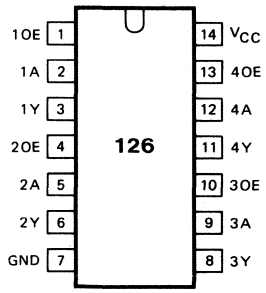

107
1J 1
1$\overline{Q}$ 2
1Q 3
1K 4
2Q 5
2$\overline{Q}$ 6
GND 7
14 VCC
13 1$\overline{R}$
12 1$\overline{CP}$
11 2K
10 2$\overline{R}$
9 2$\overline{CP}$
8 2J
7Z93193

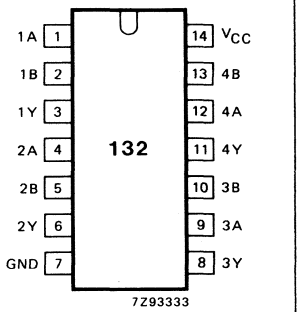

109
1$\overline{R}_D$ 1
1J 2
1$\overline{K}$ 3
1CP 4
1$\overline{S}_D$ 5
1Q 6
1$\overline{Q}$ 7
GND 8
16 VCC
15 2$\overline{R}_D$
14 2J
13 2$\overline{K}$
12 2CP
11 2$\overline{S}_D$
10 2Q
9 2$\overline{Q}$
7Z93131

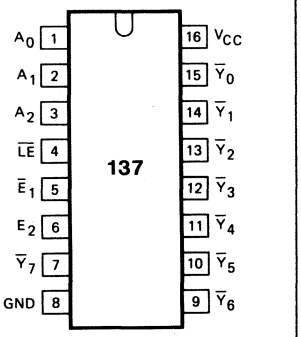

112
1$\overline{CP}$ 1
1K 2
1J 3
1$\overline{S}_D$ 4
1Q 5
1$\overline{Q}$ 6
2$\overline{Q}$ 7
GND 8
16 VCC
15 1$\overline{R}_D$
14 2$\overline{R}_D$
13 2$\overline{CP}$
12 2K
11 2J
10 2$\overline{S}_D$
9 2Q

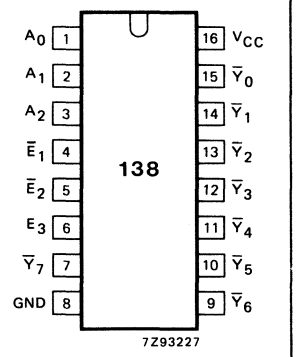

123
1$\overline{A}$ 1
1B 2
1$\overline{R}_D$ 3
1$\overline{Q}$ 4
2Q 5
$2C_{EXT}$ 6
$2R_{EXT}/C_{EXT}$ 7
GND 8
16 V_{CC}
15 $1R_{EXT}/C_{EXT}$
14 $1C_{EXT}$
13 1Q
12 2$\overline{Q}$
11 2$\overline{R}_D$
10 2B
9 2$\overline{A}$
7Z93285

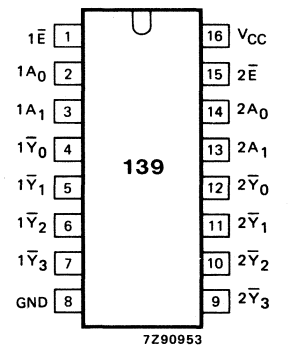

125
1$\overline{OE}$ 1
1A 2
1Y 3
2$\overline{OE}$ 4
2A 5
2Y 6
GND 7
14 V_{CC}
13 4$\overline{OE}$
12 4A
11 4Y
10 3$\overline{OE}$
9 3A
8 3Y

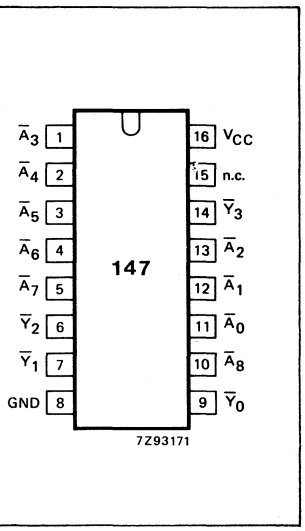

126
1OE 1
1A 2
1Y 3
2OE 4
2A 5
2Y 6
GND 7
14 V_{CC}
13 4OE
12 4A
11 4Y
10 3OE
9 3A
8 3Y

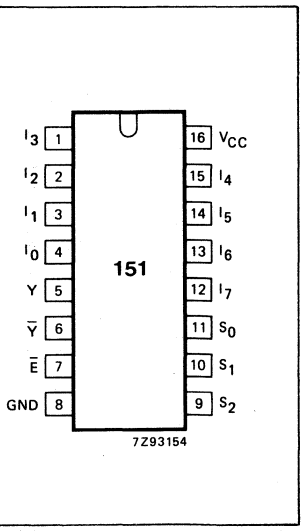

132
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 V_{CC}
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z93333

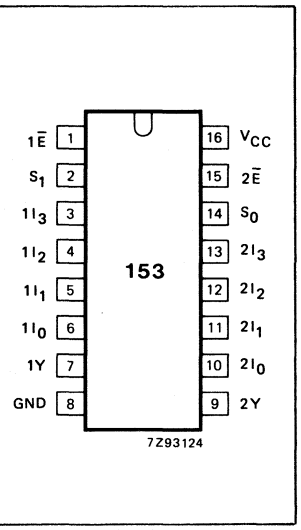

137
A_0 1
A_1 2
A_2 3
$\overline{LE}$ 4
$\overline{E}_1$ 5
E_2 6
$\overline{Y}_7$ 7
GND 8
16 V_{CC}
15 $\overline{Y}_0$
14 $\overline{Y}_1$
13 $\overline{Y}_2$
12 $\overline{Y}_3$
11 $\overline{Y}_4$
10 $\overline{Y}_5$
9 $\overline{Y}_6$

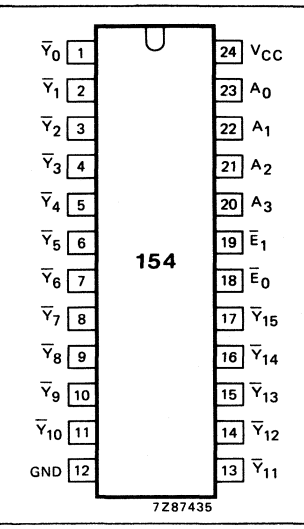

138
A_0 1
A_1 2
A_2 3
$\overline{E}_1$ 4
$\overline{E}_2$ 5
E_3 6
$\overline{Y}_7$ 7
GND 8
16 V_{CC}
15 $\overline{Y}_0$
14 $\overline{Y}_1$
13 $\overline{Y}_2$
12 $\overline{Y}_3$
11 $\overline{Y}_4$
10 $\overline{Y}_5$
9 $\overline{Y}_6$
7Z93227

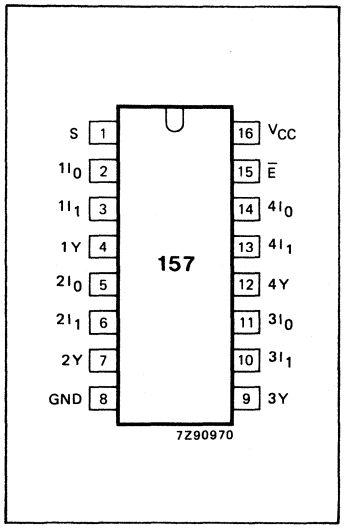

139
1$\overline{E}$ 1
$1A_0$ 2
$1A_1$ 3
$1\overline{Y}_0$ 4
$1\overline{Y}_1$ 5
$1\overline{Y}_2$ 6
$1\overline{Y}_3$ 7
GND 8
16 V_{CC}
15 2$\overline{E}$
14 $2A_0$
13 $2A_1$
12 $2\overline{Y}_0$
11 $2\overline{Y}_1$
10 $2\overline{Y}_2$
9 $2\overline{Y}_3$
7Z90953

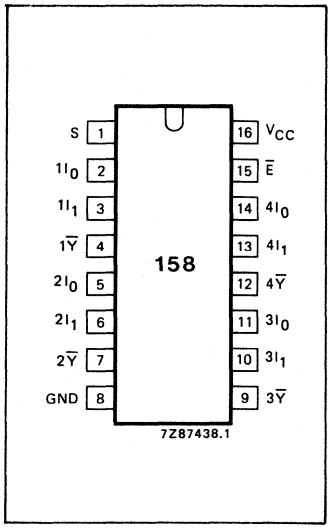

147
$\overline{A}_3$ 1
$\overline{A}_4$ 2
$\overline{A}_5$ 3
$\overline{A}_6$ 4
$\overline{A}_7$ 5
$\overline{Y}_2$ 6
$\overline{Y}_1$ 7
GND 8
16 V_{CC}
15 n.c.
14 $\overline{Y}_3$
13 $\overline{A}_2$
12 $\overline{A}_1$
11 $\overline{A}_0$
10 $\overline{A}_8$
9 $\overline{Y}_0$
7Z93171

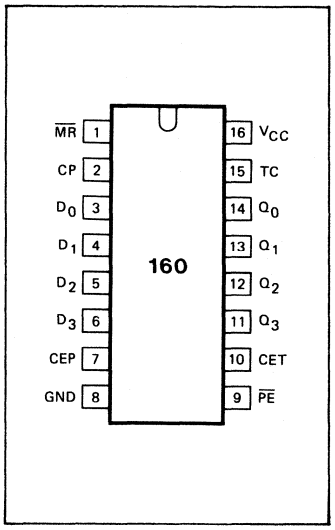

151
I_3 1
I_2 2
I_1 3
I_0 4
Y 5
$\overline{Y}$ 6
$\overline{E}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2
7Z93154

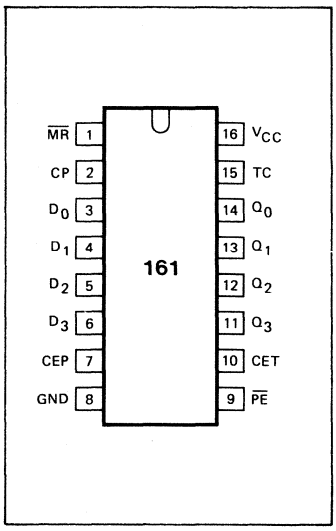

153
1$\overline{E}$ 1
S_1 2
$1I_3$ 3
$1I_2$ 4
$1I_1$ 5
$1I_0$ 6
1Y 7
GND 8
16 V_{CC}
15 2$\overline{E}$
14 S_0
13 $2I_3$
12 $2I_2$
11 $2I_1$
10 $2I_0$
9 2Y
7Z93124

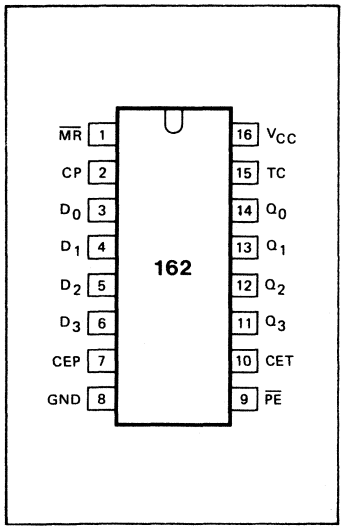

154
$\overline{Y}_0$ 1
$\overline{Y}_1$ 2
$\overline{Y}_2$ 3
$\overline{Y}_3$ 4
$\overline{Y}_4$ 5
$\overline{Y}_5$ 6
$\overline{Y}_6$ 7
$\overline{Y}_7$ 8
$\overline{Y}_8$ 9
$\overline{Y}_9$ 10
$\overline{Y}_{10}$ 11
GND 12
24 V_{CC}
23 A_0
22 A_1
21 A_2
20 A_3
19 $\overline{E}_1$
18 $\overline{E}_0$
17 $\overline{Y}_{15}$
16 $\overline{Y}_{14}$
15 $\overline{Y}_{13}$
14 $\overline{Y}_{12}$
13 $\overline{Y}_{11}$
7Z87435

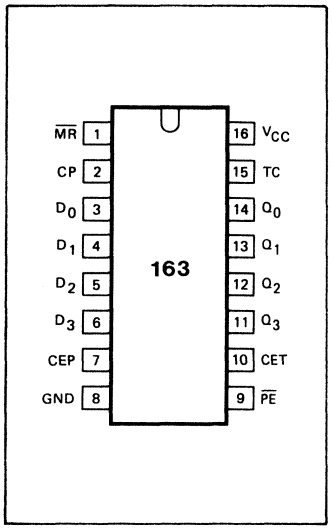

157
S 1
1I0 2
1I1 3
1Y 4
2I0 5
2I1 6
2Y 7
GND 8
16 VCC
15 E
14 4I0
13 4I1
12 4Y
11 3I0
10 3I1
9 3Y
7Z90970

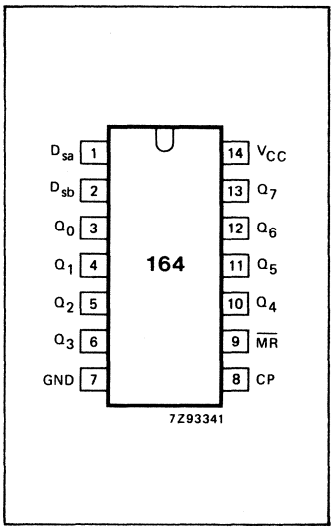

158
S 1
1I0 2
1I1 3
1Y 4
2I0 5
2I1 6
2Y 7
GND 8
16 VCC
15 E
14 4I0
13 4I1
12 4Y
11 3I0
10 3I1
9 3Y
7Z87438.1

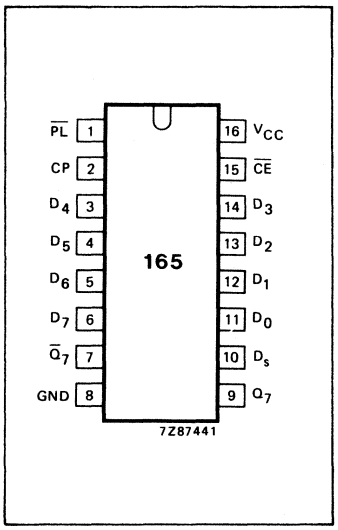

160
MR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE

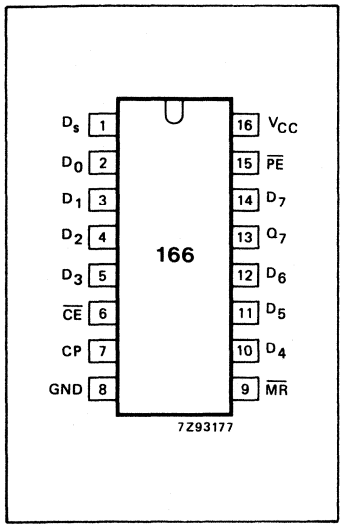

161
MR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE

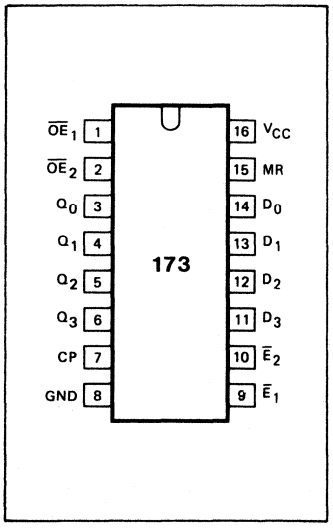

162
MR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE

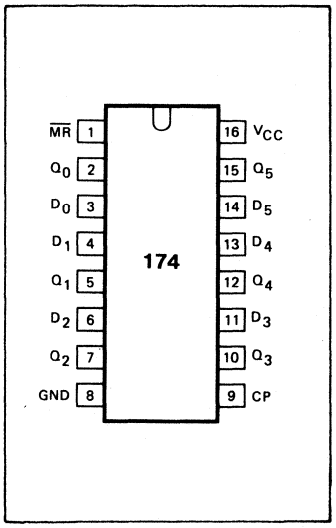

163
MR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE

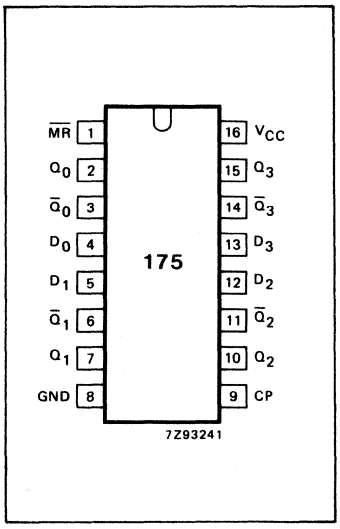

164
Dsa 1
Dsb 2
Q0 3
Q1 4
Q2 5
Q3 6
GND 7
14 VCC
13 Q7
12 Q6
11 Q5
10 Q4
9 MR
8 CP
7Z93341

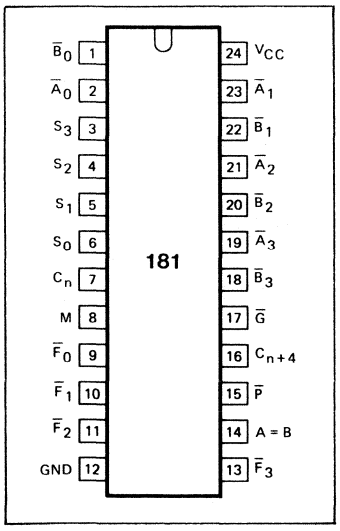

165
PL 1
CP 2
D4 3
D5 4
D6 5
D7 6
Q7 7
GND 8
16 VCC
15 CE
14 D3
13 D2
12 D1
11 D0
10 Ds
9 Q7
7Z87441

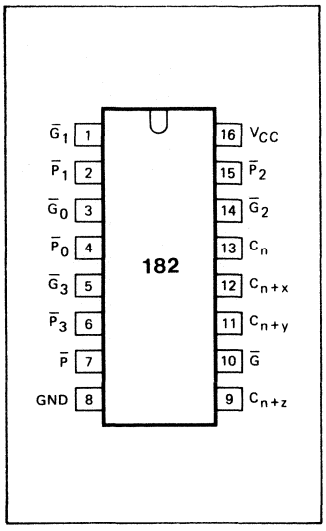

166
Ds 1
D0 2
D1 3
D2 4
D3 5
CE 6
CP 7
GND 8
16 VCC
15 PE
14 D7
13 Q7
12 D6
11 D5
10 D4
9 MR
7Z93177

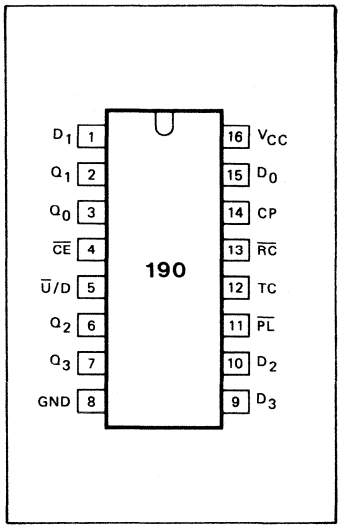

173
OE1 1
OE2 2
Q0 3
Q1 4
Q2 5
Q3 6
CP 7
GND 8
16 VCC
15 MR
14 D0
13 D1
12 D2
11 D3
10 E2
9 E1

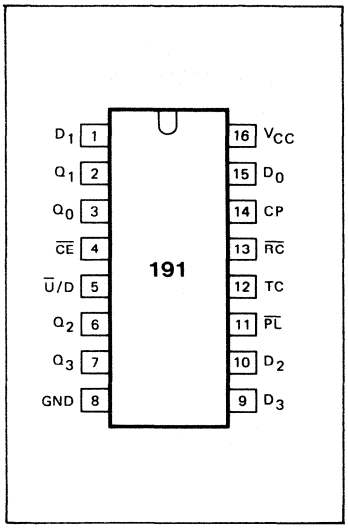

174
MR 1
Q0 2
D0 3
D1 4
Q1 5
D2 6
Q2 7
GND 8
16 VCC
15 Q5
14 D5
13 D4
12 Q4
11 D3
10 Q3
9 CP

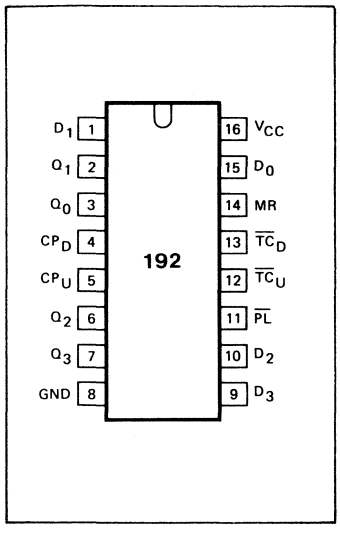

175
MR 1
Q0 2
Q0 3
D0 4
D1 5
Q1 6
Q1 7
GND 8
16 VCC
15 Q3
14 Q3
13 D3
12 D2
11 Q2
10 Q2
9 CP
7Z93241

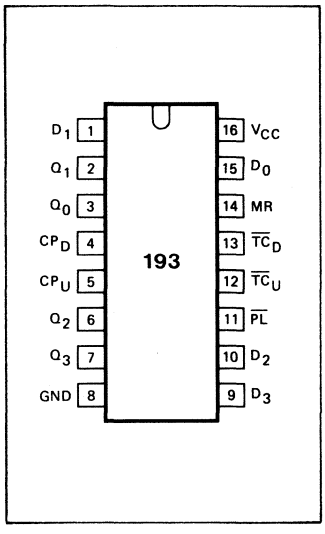

181
$\overline{B}_0$ 1
$\overline{A}_0$ 2
S_3 3
S_2 4
S_1 5
S_0 6
C_n 7
M 8
$\overline{F}_0$ 9
$\overline{F}_1$ 10
$\overline{F}_2$ 11
GND 12
24 V_{CC}
23 $\overline{A}_1$
22 $\overline{B}_1$
21 $\overline{A}_2$
20 $\overline{B}_2$
19 $\overline{A}_3$
18 $\overline{B}_3$
17 $\overline{G}$
16 C_{n+4}
15 $\overline{P}$
14 A = B
13 $\overline{F}_3$

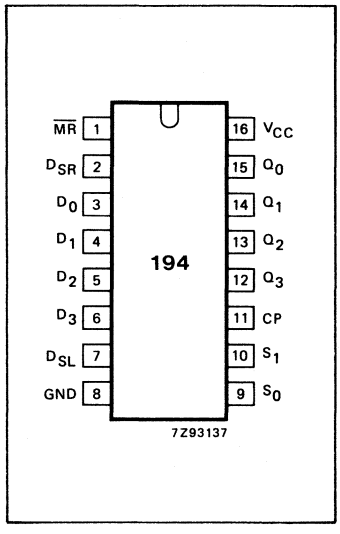

182
$\overline{G}_1$ 1
$\overline{P}_1$ 2
$\overline{G}_0$ 3
$\overline{P}_0$ 4
$\overline{G}_3$ 5
$\overline{P}_3$ 6
$\overline{P}$ 7
GND 8
16 V_{CC}
15 $\overline{P}_2$
14 $\overline{G}_2$
13 C_n
12 C_{n+x}
11 C_{n+y}
10 $\overline{G}$
9 C_{n+z}

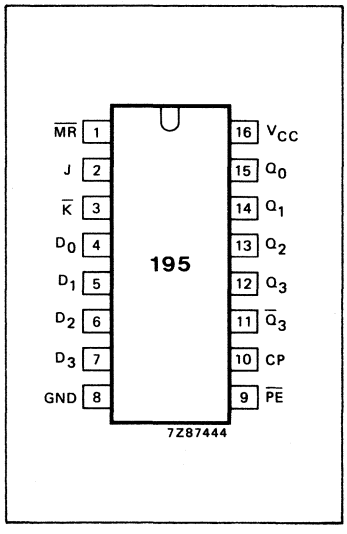

190
D_1 1
Q_1 2
Q_0 3
$\overline{CE}$ 4
$\overline{U}/D$ 5
Q_2 6
Q_3 7
GND 8
16 V_{CC}
15 D_0
14 CP
13 $\overline{RC}$
12 TC
11 $\overline{PL}$
10 D_2
9 D_3

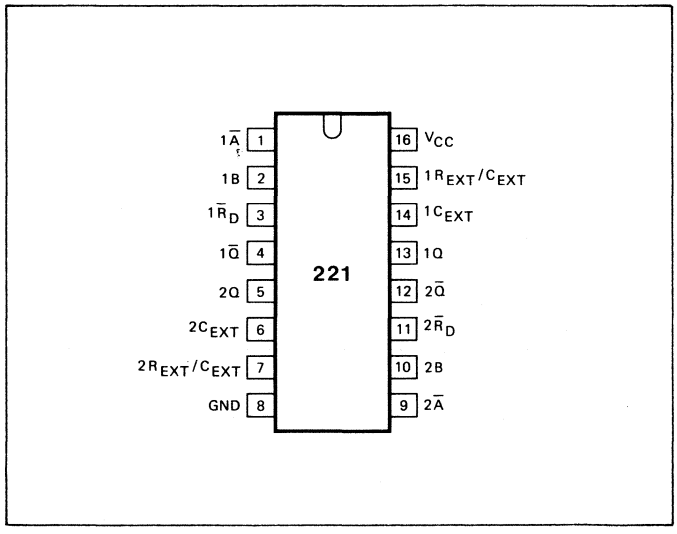

191
D_1 1
Q_1 2
Q_0 3
$\overline{CE}$ 4
$\overline{U}/D$ 5
Q_2 6
Q_3 7
GND 8
16 V_{CC}
15 D_0
14 CP
13 $\overline{RC}$
12 TC
11 $\overline{PL}$
10 D_2
9 D_3

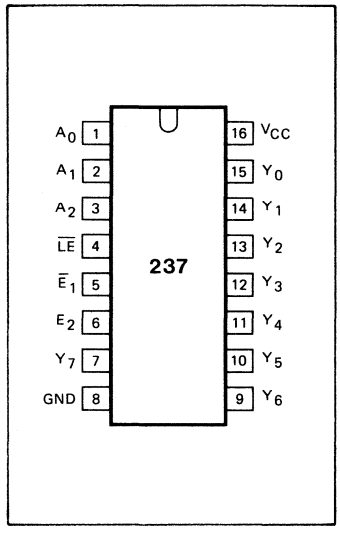

192
D_1 1
Q_1 2
Q_0 3
CP_D 4
CP_U 5
Q_2 6
Q_3 7
GND 8
16 V_{CC}
15 D_0
14 MR
13 $\overline{TC}_D$
12 $\overline{TC}_U$
11 $\overline{PL}$
10 D_2
9 D_3

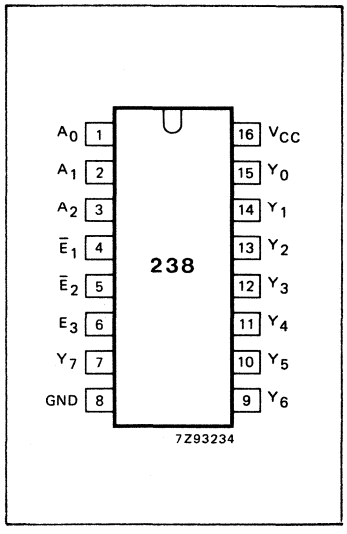

193
D_1 1
Q_1 2
Q_0 3
CP_D 4
CP_U 5
Q_2 6
Q_3 7
GND 8
16 V_{CC}
15 D_0
14 MR
13 $\overline{TC}_D$
12 $\overline{TC}_U$
11 $\overline{PL}$
10 D_2
9 D_3

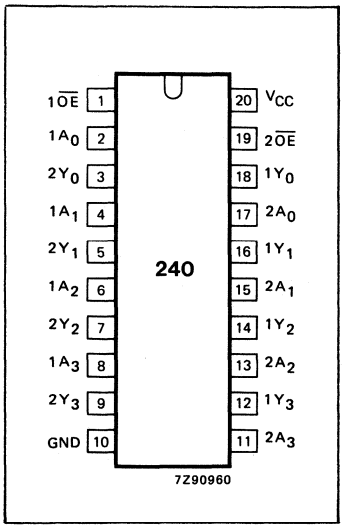

194
$\overline{MR}$ 1
D_{SR} 2
D_0 3
D_1 4
D_2 5
D_3 6
D_{SL} 7
GND 8
16 V_{CC}
15 Q_0
14 Q_1
13 Q_2
12 Q_3
11 CP
10 S_1
9 S_0
7Z93137

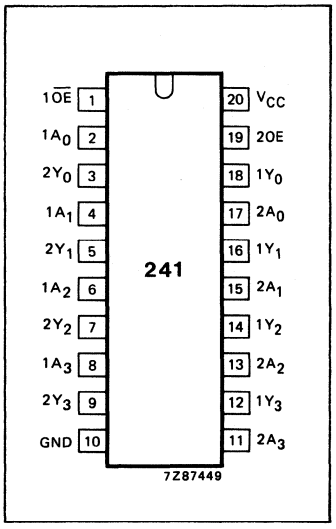

195
$\overline{MR}$ 1
J 2
$\overline{K}$ 3
D_0 4
D_1 5
D_2 6
D_3 7
GND 8
16 V_{CC}
15 Q_0
14 Q_1
13 Q_2
12 Q_3
11 $\overline{Q}_3$
10 CP
9 $\overline{PE}$
7Z87444

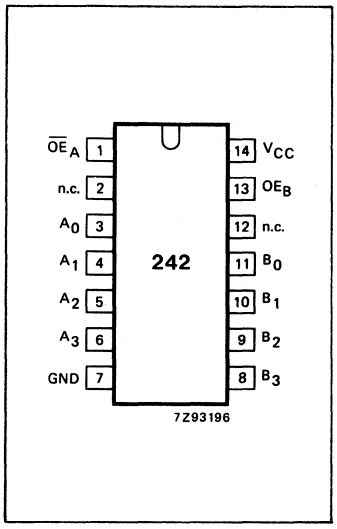

221
$1\overline{A}$ 1
1B 2
$1\overline{R}_D$ 3
$1\overline{Q}$ 4
2Q 5
$2C_{EXT}$ 6
$2R_{EXT}/C_{EXT}$ 7
GND 8
16 V_{CC}
15 $1R_{EXT}/C_{EXT}$
14 $1C_{EXT}$
13 1Q
12 $2\overline{Q}$
11 $2\overline{R}_D$
10 2B
9 $2\overline{A}$

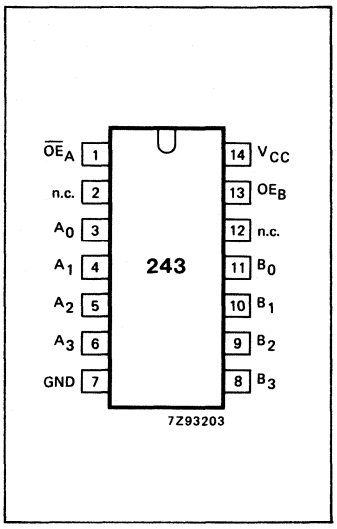

237
A_0 1
A_1 2
A_2 3
$\overline{LE}$ 4
$\overline{E}_1$ 5
E_2 6
Y_7 7
GND 8
16 V_{CC}
15 Y_0
14 Y_1
13 Y_2
12 Y_3
11 Y_4
10 Y_5
9 Y_6

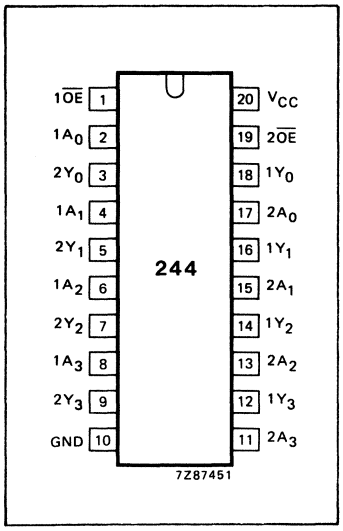

238
A_0 1
A_1 2
A_2 3
$\overline{E}_1$ 4
$\overline{E}_2$ 5
E_3 6
Y_7 7
GND 8
16 V_{CC}
15 Y_0
14 Y_1
13 Y_2
12 Y_3
11 Y_4
10 Y_5
9 Y_6
7Z93234

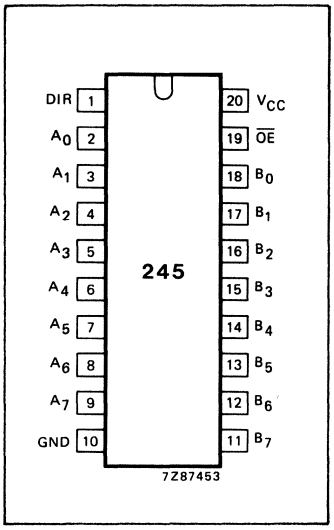

240
1$\overline{OE}$ 1
1A$_0$ 2
2Y$_0$ 3
1A$_1$ 4
2Y$_1$ 5
1A$_2$ 6
2Y$_2$ 7
1A$_3$ 8
2Y$_3$ 9
GND 10
20 V$_{CC}$
19 2$\overline{OE}$
18 1Y$_0$
17 2A$_0$
16 1Y$_1$
15 2A$_1$
14 1Y$_2$
13 2A$_2$
12 1Y$_3$
11 2A$_3$
7Z90960

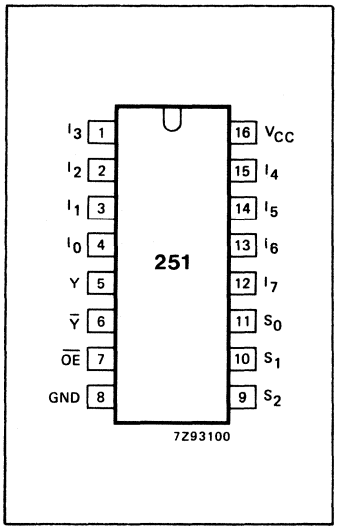

241
1$\overline{OE}$ 1
1A$_0$ 2
2Y$_0$ 3
1A$_1$ 4
2Y$_1$ 5
1A$_2$ 6
2Y$_2$ 7
1A$_3$ 8
2Y$_3$ 9
GND 10
20 V$_{CC}$
19 2OE
18 1Y$_0$
17 2A$_0$
16 1Y$_1$
15 2A$_1$
14 1Y$_2$
13 2A$_2$
12 1Y$_3$
11 2A$_3$
7Z87449

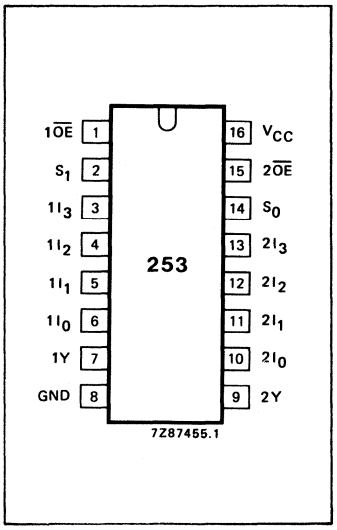

242
$\overline{OE}_A$ 1
n.c. 2
A$_0$ 3
A$_1$ 4
A$_2$ 5
A$_3$ 6
GND 7
14 V$_{CC}$
13 OE$_B$
12 n.c.
11 B$_0$
10 B$_1$
9 B$_2$
8 B$_3$
7Z93196

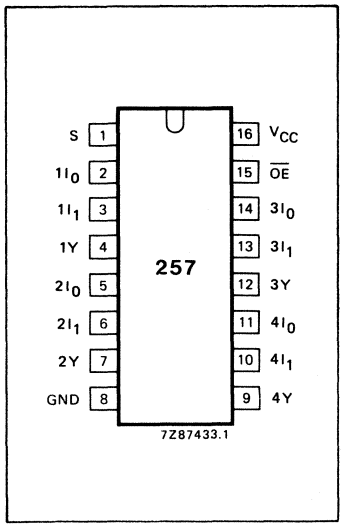

243
$\overline{OE}_A$ 1
n.c. 2
A$_0$ 3
A$_1$ 4
A$_2$ 5
A$_3$ 6
GND 7
14 V$_{CC}$
13 OE$_B$
12 n.c.
11 B$_0$
10 B$_1$
9 B$_2$
8 B$_3$
7Z93203

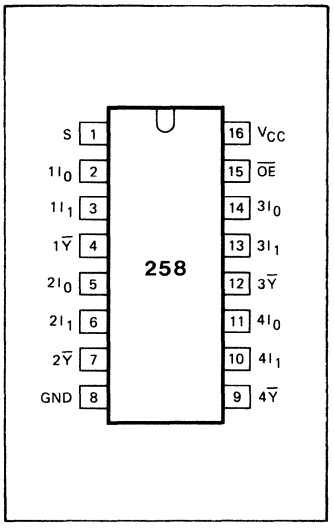

244
1$\overline{OE}$ 1
1A$_0$ 2
2Y$_0$ 3
1A$_1$ 4
2Y$_1$ 5
1A$_2$ 6
2Y$_2$ 7
1A$_3$ 8
2Y$_3$ 9
GND 10
20 V$_{CC}$
19 2$\overline{OE}$
18 1Y$_0$
17 2A$_0$
16 1Y$_1$
15 2A$_1$
14 1Y$_2$
13 2A$_2$
12 1Y$_3$
11 2A$_3$
7Z87451

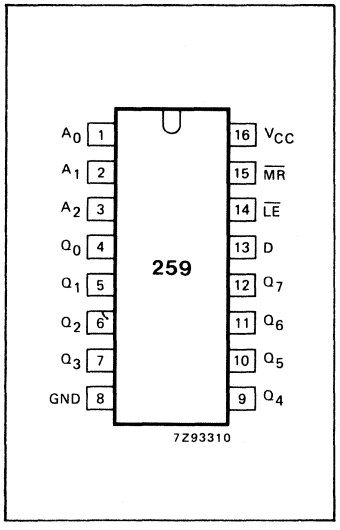

245
DIR 1
A$_0$ 2
A$_1$ 3
A$_2$ 4
A$_3$ 5
A$_4$ 6
A$_5$ 7
A$_6$ 8
A$_7$ 9
GND 10
20 V$_{CC}$
19 $\overline{OE}$
18 B$_0$
17 B$_1$
16 B$_2$
15 B$_3$
14 B$_4$
13 B$_5$
12 B$_6$
11 B$_7$
7Z87453

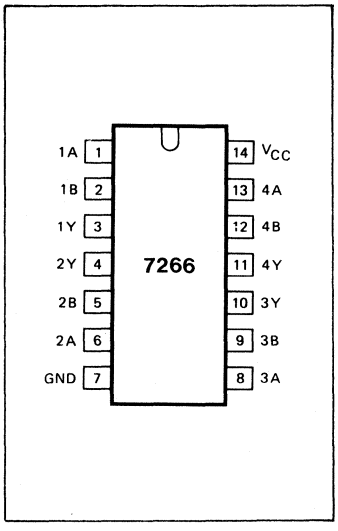

251
I$_3$ 1
I$_2$ 2
I$_1$ 3
I$_0$ 4
Y 5
$\overline{Y}$ 6
$\overline{OE}$ 7
GND 8
16 V$_{CC}$
15 I$_4$
14 I$_5$
13 I$_6$
12 I$_7$
11 S$_0$
10 S$_1$
9 S$_2$
7Z93100

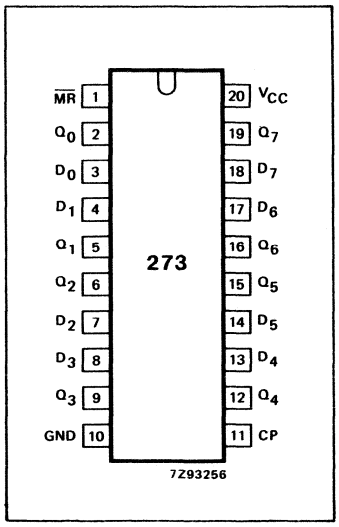

253
1$\overline{OE}$ 1
S$_1$ 2
1I$_3$ 3
1I$_2$ 4
1I$_1$ 5
1I$_0$ 6
1Y 7
GND 8
16 V$_{CC}$
15 2$\overline{OE}$
14 S$_0$
13 2I$_3$
12 2I$_2$
11 2I$_1$
10 2I$_0$
9 2Y
7Z87455.1

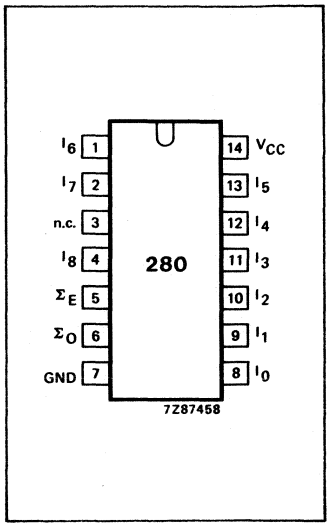

257
S 1
1I$_0$ 2
1I$_1$ 3
1Y 4
2I$_0$ 5
2I$_1$ 6
2Y 7
GND 8
16 V$_{CC}$
15 $\overline{OE}$
14 3I$_0$
13 3I$_1$
12 3Y
11 4I$_0$
10 4I$_1$
9 4Y
7Z87433.1

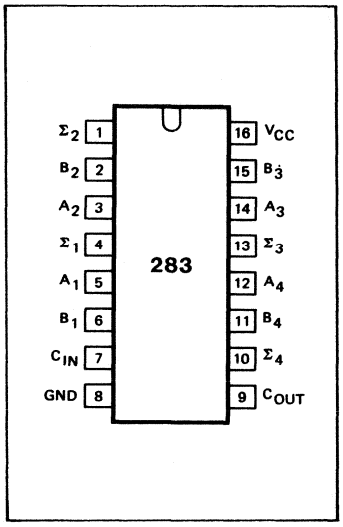

258
S 1
1I$_0$ 2
1I$_1$ 3
1$\overline{Y}$ 4
2I$_0$ 5
2I$_1$ 6
2$\overline{Y}$ 7
GND 8
16 V$_{CC}$
15 $\overline{OE}$
14 3I$_0$
13 3I$_1$
12 3$\overline{Y}$
11 4I$_0$
10 4I$_1$
9 4$\overline{Y}$

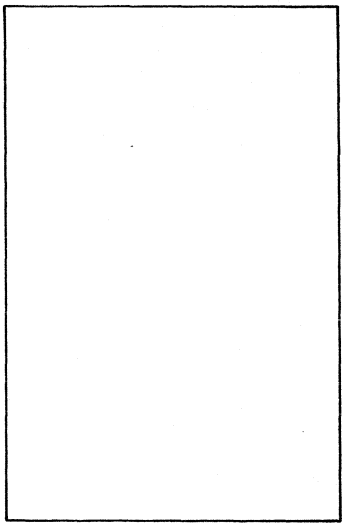

259
A$_0$ 1
A$_1$ 2
A$_2$ 3
Q$_0$ 4
Q$_1$ 5
Q$_2$ 6
Q$_3$ 7
GND 8
16 V$_{CC}$
15 $\overline{MR}$
14 $\overline{LE}$
13 D
12 Q$_7$
11 Q$_6$
10 Q$_5$
9 Q$_4$
7Z93310

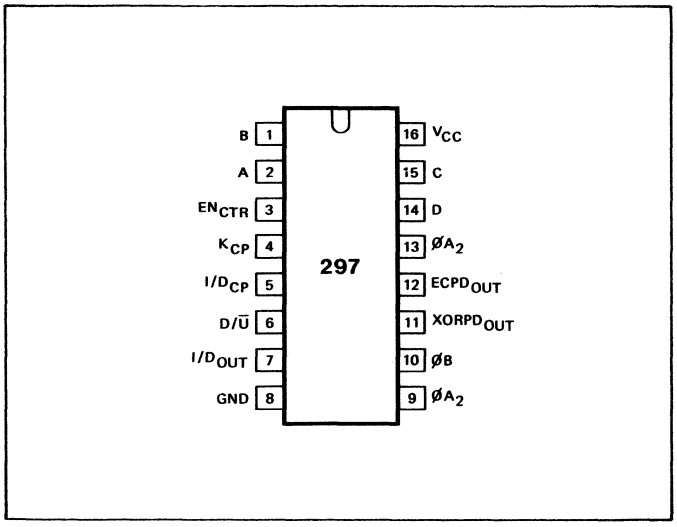

7266
1A 1
1B 2
1Y 3
2Y 4
2B 5
2A 6
GND 7
14 V$_{CC}$
13 4A
12 4B
11 4Y
10 3Y
9 3B
8 3A

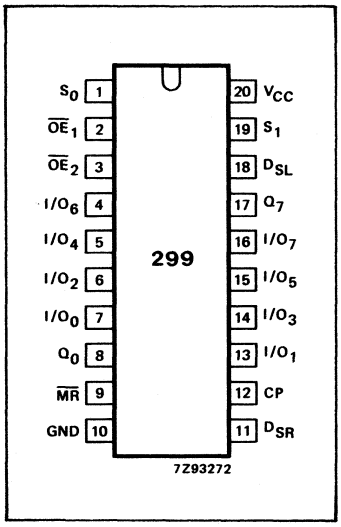

273
MR 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 VCC
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 CP
7Z93256

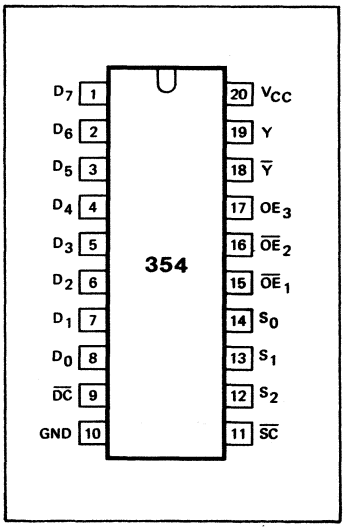

280
I6 1
I7 2
n.c. 3
I8 4
ΣE 5
ΣO 6
GND 7
14 VCC
13 I5
12 I4
11 I3
10 I2
9 I1
8 I0
7Z87458

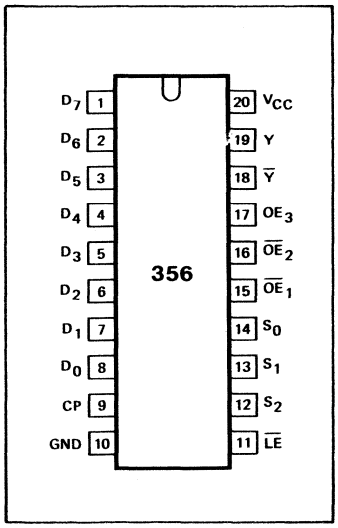

283
Σ2 1
B2 2
A2 3
Σ1 4
A1 5
B1 6
CIN 7
GND 8
16 VCC
15 B3
14 A3
13 Σ3
12 A4
11 B4
10 Σ4
9 COUT

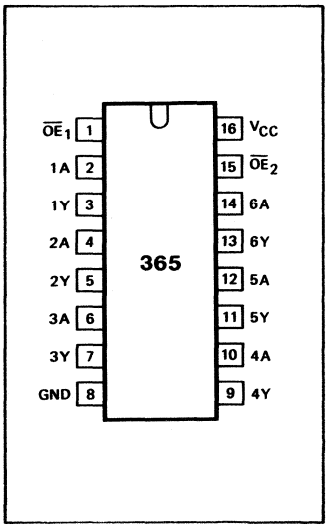


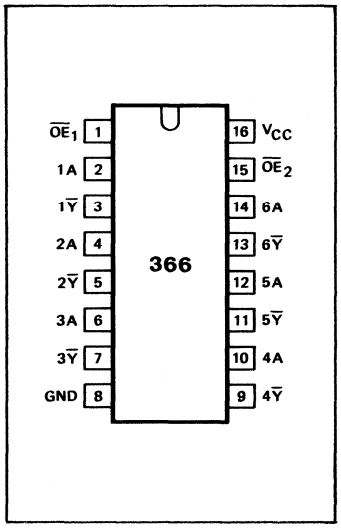

297
B 1
A 2
ENCTR 3
KCP 4
I/DCP 5
D/U 6
I/DOUT 7
GND 8
16 VCC
15 C
14 D
13 ØA2
12 ECPDOUT
11 XORPDOUT
10 ØB
9 ØA2

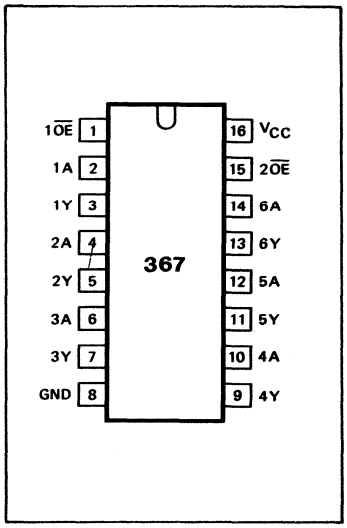

299
S0 1
OE1 2
OE2 3
I/O6 4
I/O4 5
I/O2 6
I/O0 7
Q0 8
MR 9
GND 10
20 VCC
19 S1
18 DSL
17 Q7
16 I/O7
15 I/O5
14 I/O3
13 I/O1
12 CP
11 DSR
7Z93272

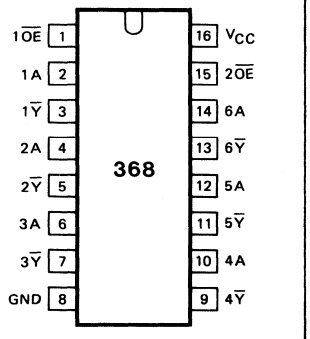

354
D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
DC 9
GND 10
20 VCC
19 Y
18 Y
17 OE3
16 OE2
15 OE1
14 S0
13 S1
12 S2
11 SC

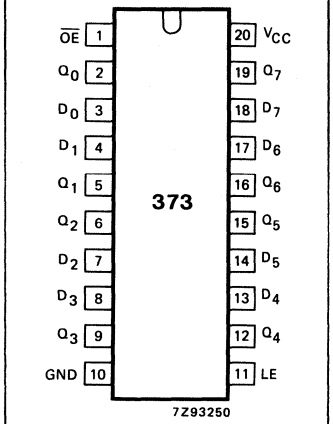

356
D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
CP 9
GND 10
20 VCC
19 Y
18 Y
17 OE3
16 OE2
15 OE1
14 S0
13 S1
12 S2
11 LE

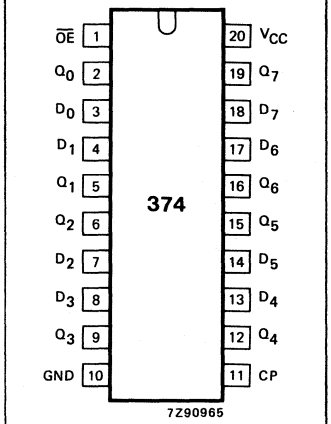

365
OE1 1
1A 2
1Y 3
2A 4
2Y 5
3A 6
3Y 7
GND 8
16 VCC
15 OE2
14 6A
13 6Y
12 5A
11 5Y
10 4A
9 4Y

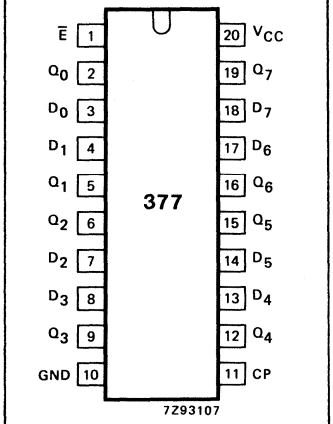

366
OE1 1
1A 2
1Y 3
2A 4
2Y 5
3A 6
3Y 7
GND 8
16 VCC
15 OE2
14 6A
13 6Y
12 5A
11 5Y
10 4A
9 4Y

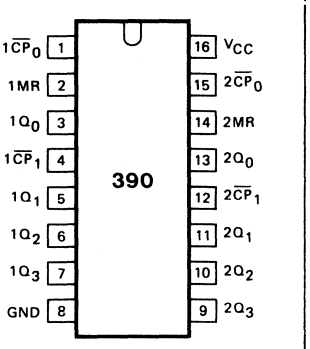

367
1OE 1
1A 2
1Y 3
2A 4
2Y 5
3A 6
3Y 7
GND 8
16 VCC
15 2OE
14 6A
13 6Y
12 5A
11 5Y
10 4A
9 4Y

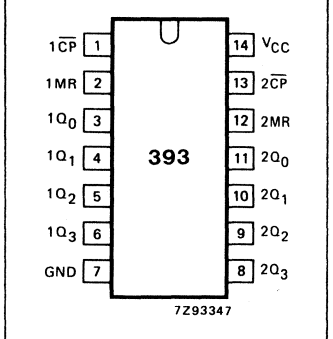

368
1$\overline{OE}$ 1
1A 2
1$\overline{Y}$ 3
2A 4
2$\overline{Y}$ 5
3A 6
3$\overline{Y}$ 7
GND 8
16 V_{CC}
15 2$\overline{OE}$
14 6A
13 6$\overline{Y}$
12 5A
11 5$\overline{Y}$
10 4A
9 4$\overline{Y}$

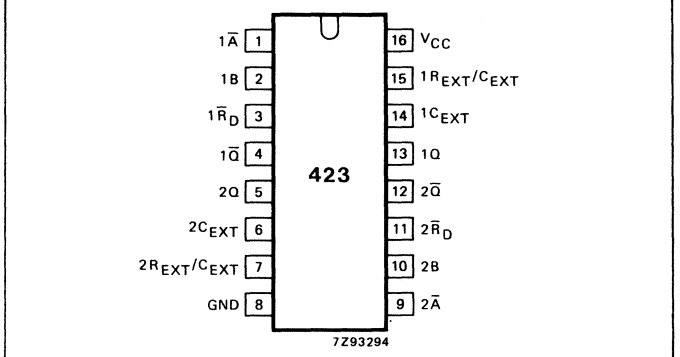

373
$\overline{OE}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 LE
7Z93250

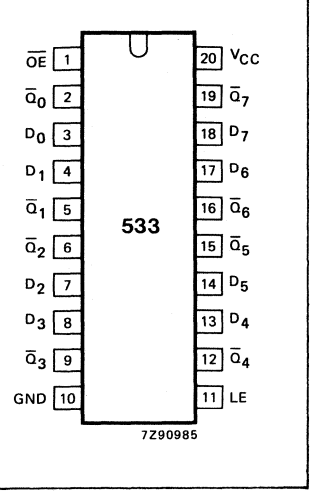

374
$\overline{OE}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP
7Z90965

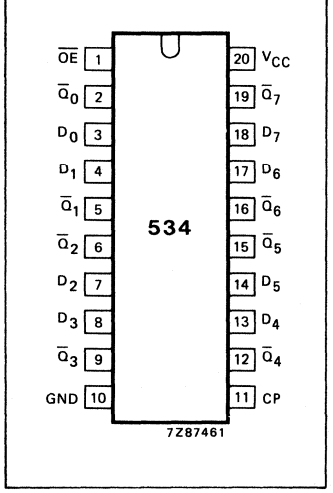

377
$\overline{E}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP
7Z93107

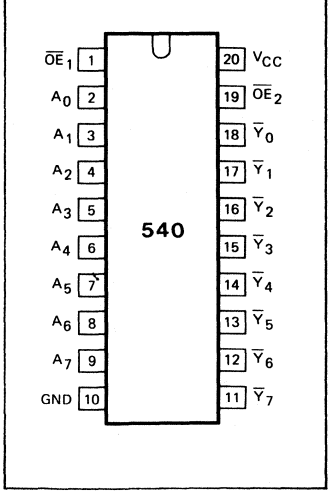

390
1$\overline{CP}_0$ 1
1MR 2
1Q_0 3
1$\overline{CP}_1$ 4
1Q_1 5
1Q_2 6
1Q_3 7
GND 8
16 V_{CC}
15 2$\overline{CP}_0$
14 2MR
13 2Q_0
12 2$\overline{CP}_1$
11 2Q_1
10 2Q_2
9 2Q_3

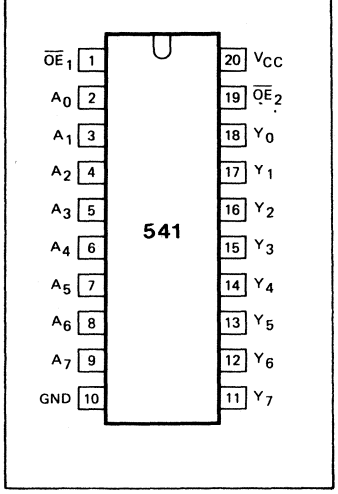

393
1$\overline{CP}$ 1
1MR 2
1Q_0 3
1Q_1 4
1Q_2 5
1Q_3 6
GND 7
14 V_{CC}
13 2$\overline{CP}$
12 2MR
11 2Q_0
10 2Q_1
9 2Q_2
8 2Q_3
7Z93347

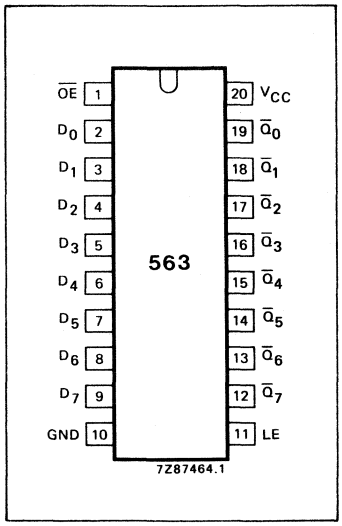

423
1$\overline{A}$ 1
1B 2
1$\overline{R}_D$ 3
1$\overline{Q}$ 4
2Q 5
$^2C_{EXT}$ 6
$^2R_{EXT}/^2C_{EXT}$ 7
GND 8
16 V_{CC}
15 $^1R_{EXT}/^1C_{EXT}$
14 $^1C_{EXT}$
13 1Q
12 2$\overline{Q}$
11 2$\overline{R}_D$
10 2B
9 2$\overline{A}$
7Z93294

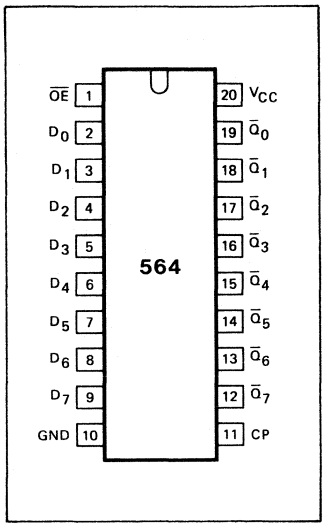

533
$\overline{OE}$ 1
$\overline{Q}_0$ 2
D_0 3
D_1 4
$\overline{Q}_1$ 5
$\overline{Q}_2$ 6
D_2 7
D_3 8
$\overline{Q}_3$ 9
GND 10
20 V_{CC}
19 $\overline{Q}_7$
18 D_7
17 D_6
16 $\overline{Q}_6$
15 $\overline{Q}_5$
14 D_5
13 D_4
12 $\overline{Q}_4$
11 LE
7Z90985

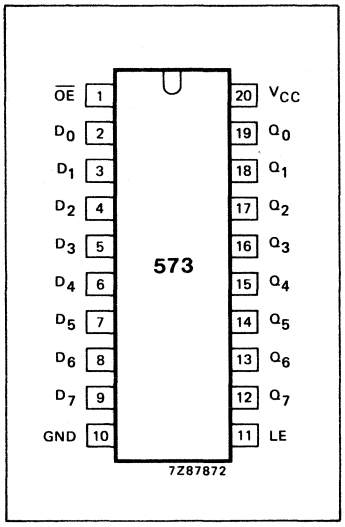

534
$\overline{OE}$ 1
$\overline{Q}_0$ 2
D_0 3
D_1 4
$\overline{Q}_1$ 5
$\overline{Q}_2$ 6
D_2 7
D_3 8
$\overline{Q}_3$ 9
GND 10
20 V_{CC}
19 $\overline{Q}_7$
18 D_7
17 D_6
16 $\overline{Q}_6$
15 $\overline{Q}_5$
14 D_5
13 D_4
12 $\overline{Q}_4$
11 CP
7Z87461

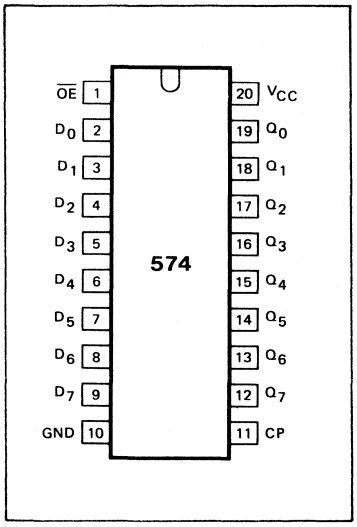

540
$\overline{OE}_1$ 1
A_0 2
A_1 3
A_2 4
A_3 5
A_4 6
A_5 7
A_6 8
A_7 9
GND 10
20 V_{CC}
19 $\overline{OE}_2$
18 $\overline{Y}_0$
17 $\overline{Y}_1$
16 $\overline{Y}_2$
15 $\overline{Y}_3$
14 $\overline{Y}_4$
13 $\overline{Y}_5$
12 $\overline{Y}_6$
11 $\overline{Y}_7$

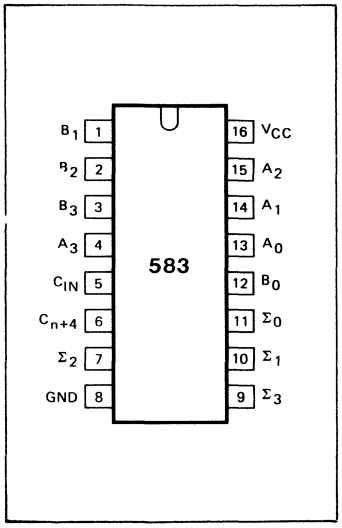

541
$\overline{OE}_1$ 1
A_0 2
A_1 3
A_2 4
A_3 5
A_4 6
A_5 7
A_6 8
A_7 9
GND 10
20 V_{CC}
19 $\overline{OE}_2$
18 Y_0
17 Y_1
16 Y_2
15 Y_3
14 Y_4
13 Y_5
12 Y_6
11 Y_7

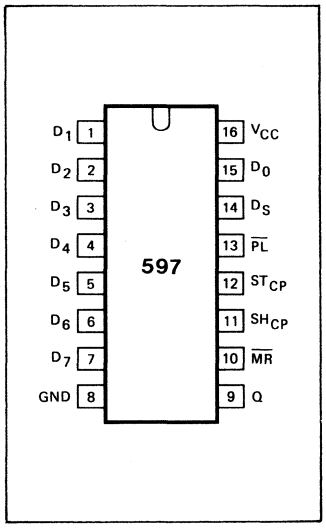

563
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 LE
7Z87464.1

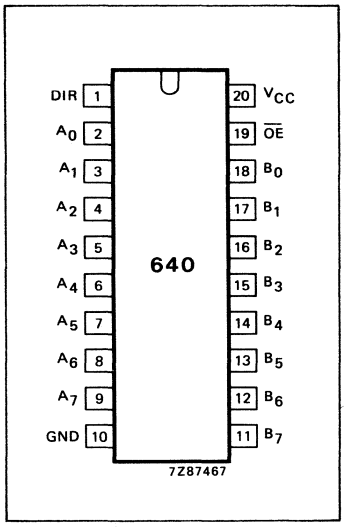

564
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 CP

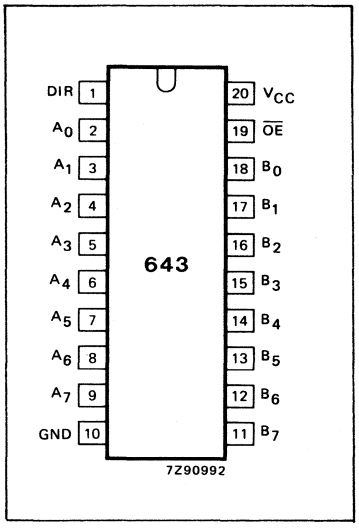

573
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 LE
7Z87872

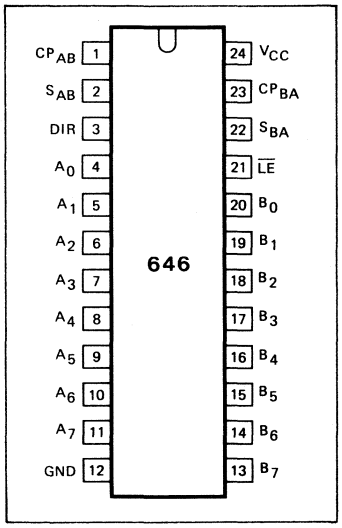

574
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 CP

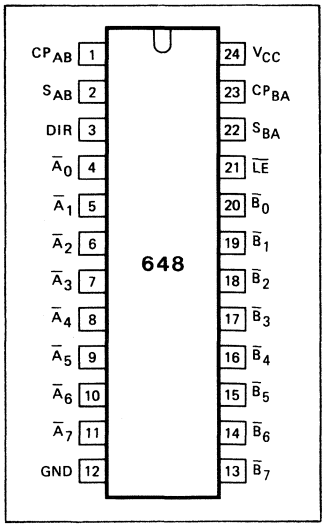

583
B1 1
B2 2
B3 3
A3 4
CIN 5
Cn+4 6
Σ2 7
GND 8
16 VCC
15 A2
14 A1
13 A0
12 B0
11 Σ0
10 Σ1
9 Σ3

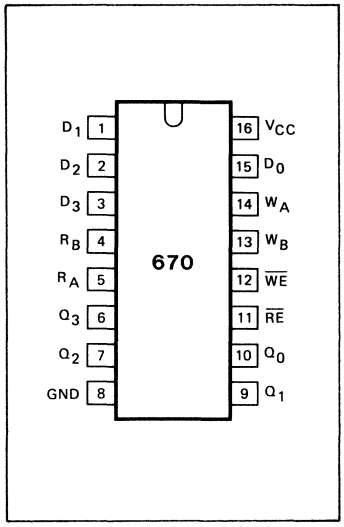

597
D1 1
D2 2
D3 3
D4 4
D5 5
D6 6
D7 7
GND 8
16 VCC
15 D0
14 DS
13 PL
12 STCP
11 SHCP
10 MR
9 Q

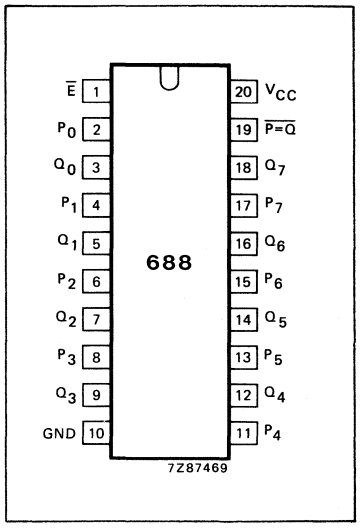

640
DIR 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
7Z87467

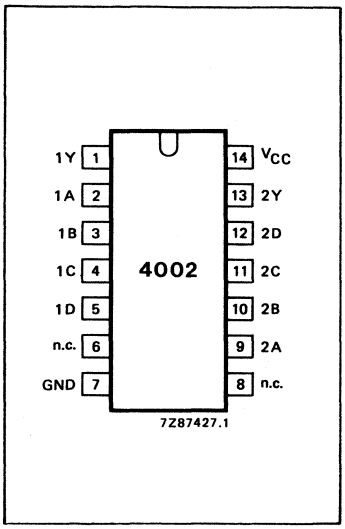

643
DIR 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
7Z90992

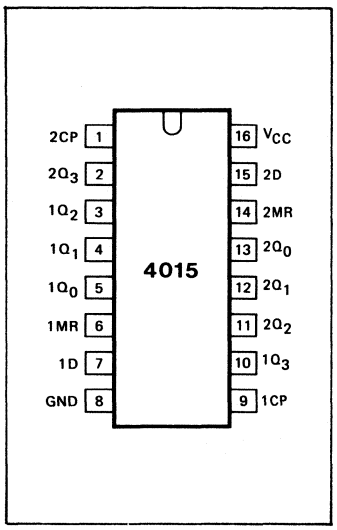

646
CPAB 1
SAB 2
DIR 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 LE
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7

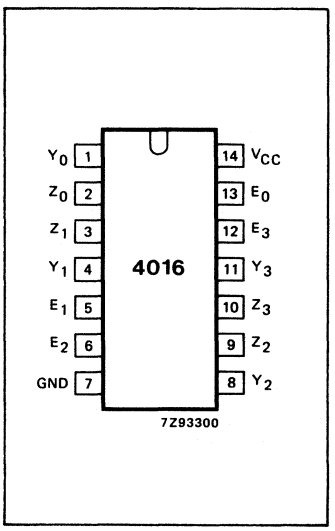

648
CPAB 1
SAB 2
DIR 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 LE
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7

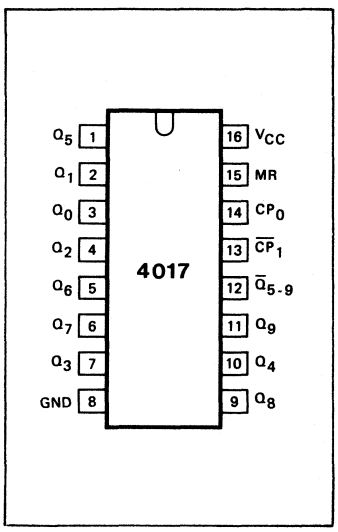

670
D1 1
D2 2
D3 3
RB 4
RA 5
Q3 6
Q2 7
GND 8
16 VCC
15 D0
14 WA
13 WB
12 WE
11 RE
10 Q0
9 Q1

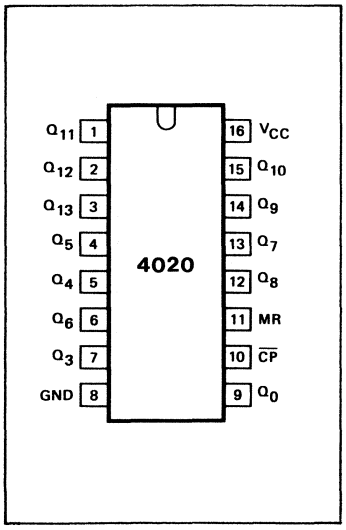

688
E 1
P0 2
Q0 3
P1 4
Q1 5
P2 6
Q2 7
P3 8
Q3 9
GND 10
20 VCC
19 P=Q
18 Q7
17 P7
16 Q6
15 P6
14 Q5
13 P5
12 Q4
11 P4
7Z87469

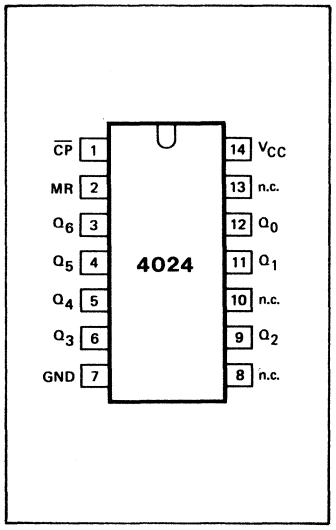

4002
1Y 1
1A 2
1B 3
1C 4
1D 5
n.c. 6
GND 7
14 VCC
13 2Y
12 2D
11 2C
10 2B
9 2A
8 n.c.
7Z87427.1

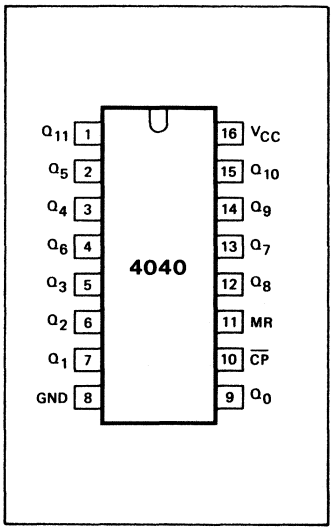

4015
2CP 1
2Q3 2
1Q2 3
1Q1 4
1Q0 5
1MR 6
1D 7
GND 8
16 VCC
15 2D
14 2MR
13 2Q0
12 2Q1
11 2Q2
10 1Q3
9 1CP

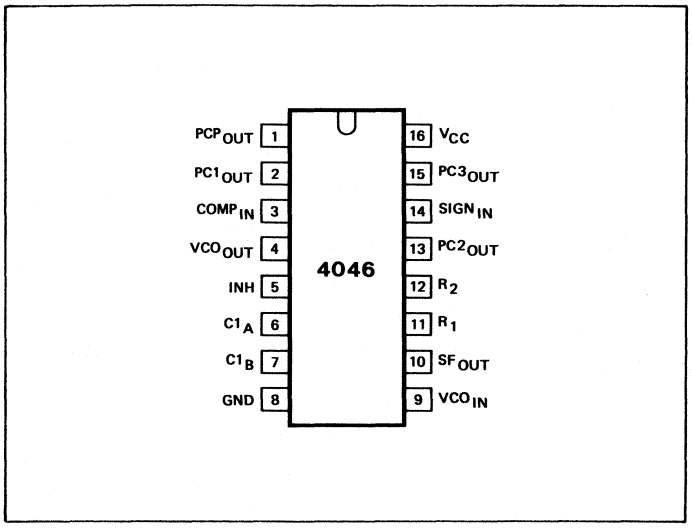

4016
Y0 1
Z0 2
Z1 3
Y1 4
E1 5
E2 6
GND 7
14 VCC
13 E0
12 E3
11 Y3
10 Z3
9 Z2
8 Y2
7Z93300

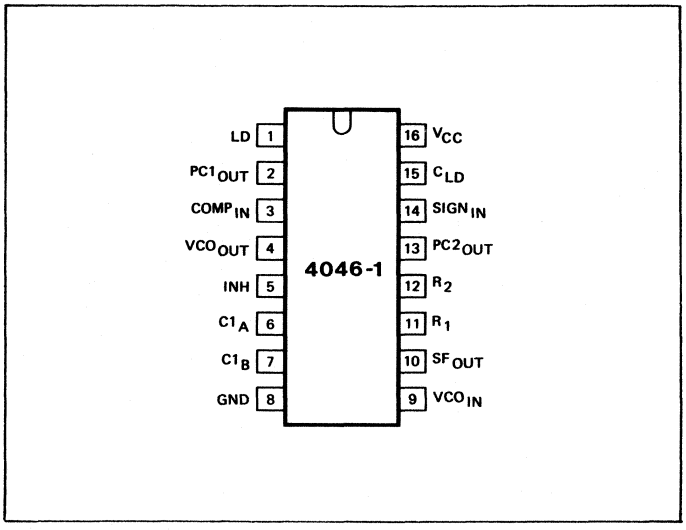

4017
Q5 1
Q1 2
Q0 3
Q2 4
Q6 5
Q7 6
Q3 7
GND 8
16 VCC
15 MR
14 CP0
13 CP1
12 Q5-9
11 Q9
10 Q4
9 Q8

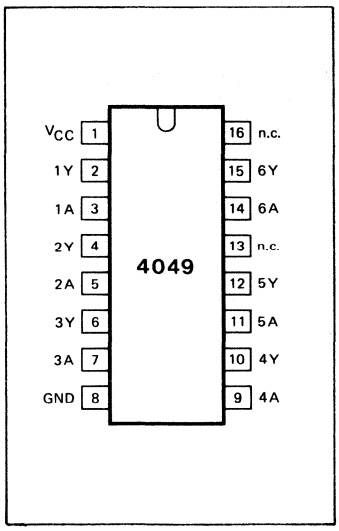

4020
Q11 1
Q12 2
Q13 3
Q5 4
Q4 5
Q6 6
Q3 7
GND 8
16 VCC
15 Q10
14 Q9
13 Q7
12 Q8
11 MR
10 CP
9 Q0

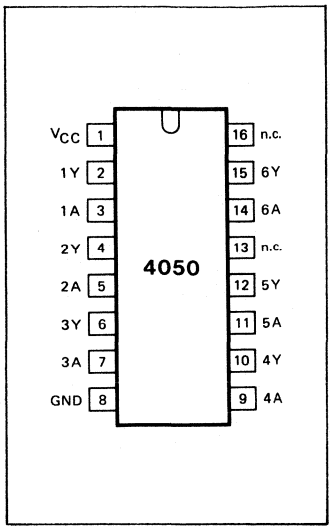

4024
CP 1
MR 2
Q6 3
Q5 4
Q4 5
Q3 6
GND 7
14 VCC
13 n.c.
12 Q0
11 Q1
10 n.c.
9 Q2
8 n.c.

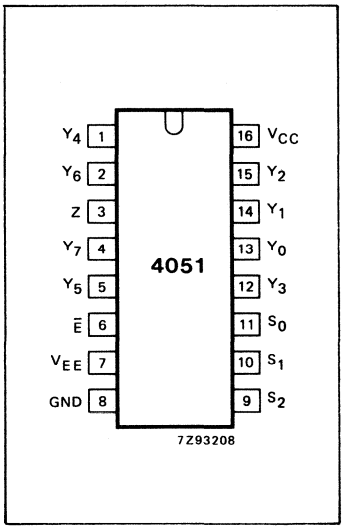

4040
Q11 1
Q5 2
Q4 3
Q6 4
Q3 5
Q2 6
Q1 7
GND 8
16 VCC
15 Q10
14 Q9
13 Q7
12 Q8
11 MR
10 CP
9 Q0

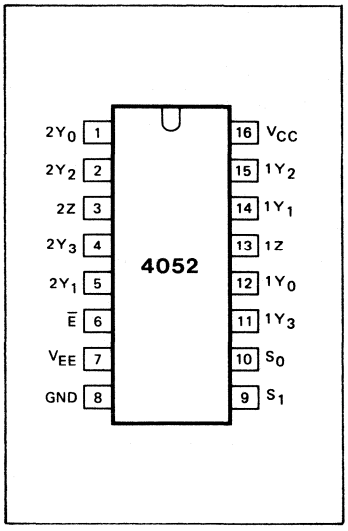

4046
PCPOUT 1
PC1OUT 2
COMPIN 3
VCOOUT 4
INH 5
C1A 6
C1B 7
GND 8
16 VCC
15 PC3OUT
14 SIGNIN
13 PC2OUT
12 R2
11 R1
10 SFOUT
9 VCOIN

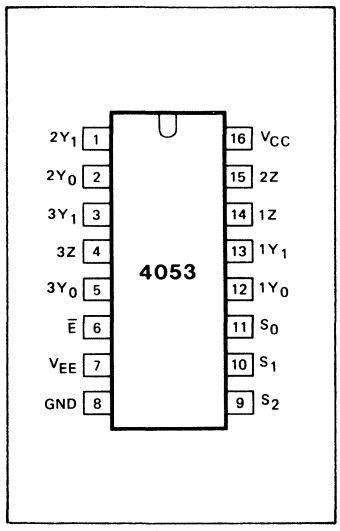

4046-1
LD 1
PC1OUT 2
COMPIN 3
VCOOUT 4
INH 5
C1A 6
C1B 7
GND 8
16 VCC
15 CLD
14 SIGNIN
13 PC2OUT
12 R2
11 R1
10 SFOUT
9 VCOIN

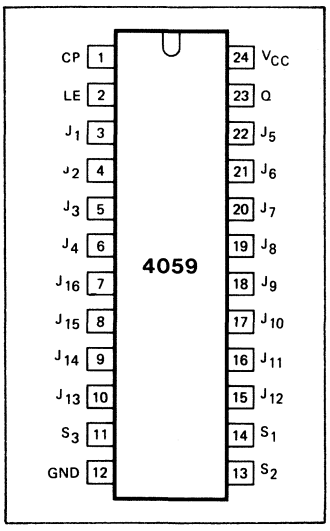

4049
VCC 1
1Y 2
1A 3
2Y 4
2A 5
3Y 6
3A 7
GND 8
16 n.c.
15 6Y
14 6A
13 n.c.
12 5Y
11 5A
10 4Y
9 4A

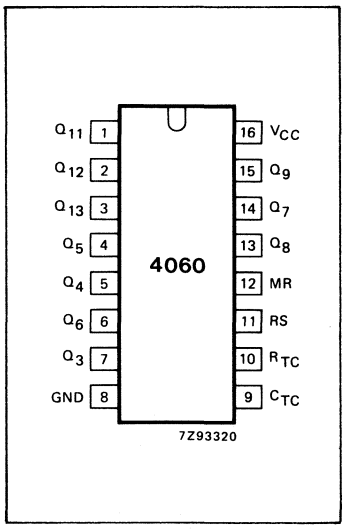

4050
VCC 1
1Y 2
1A 3
2Y 4
2A 5
3Y 6
3A 7
GND 8
16 n.c.
15 6Y
14 6A
13 n.c.
12 5Y
11 5A
10 4Y
9 4A

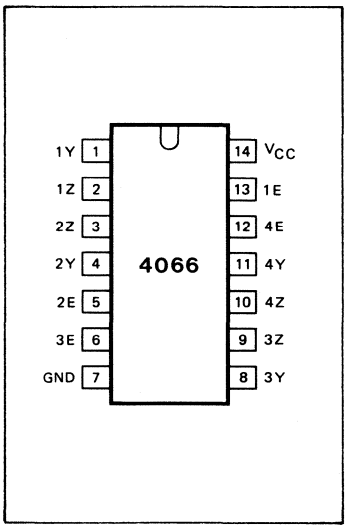

4051
Y4 1
Y6 2
Z 3
Y7 4
Y5 5
E 6
VEE 7
GND 8
16 VCC
15 Y2
14 Y1
13 Y0
12 Y3
11 S0
10 S1
9 S2
7Z93208

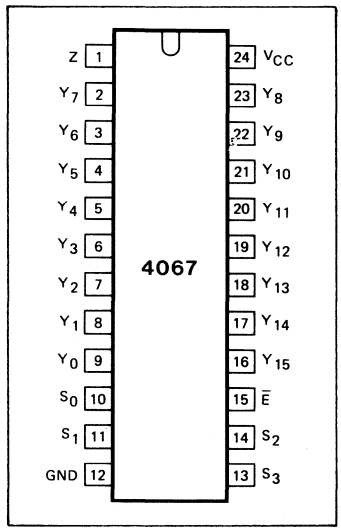

4052
2Y0 1
2Y2 2
2Z 3
2Y3 4
2Y1 5
E 6
VEE 7
GND 8
16 VCC
15 1Y2
14 1Y1
13 1Z
12 1Y0
11 1Y3
10 S0
9 S1

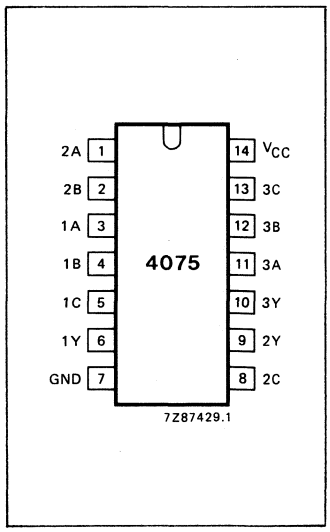

4053
2Y1 1
2Y0 2
3Y1 3
3Z 4
3Y0 5
E 6
VEE 7
GND 8
16 VCC
15 2Z
14 1Z
13 1Y1
12 1Y0
11 S0
10 S1
9 S2

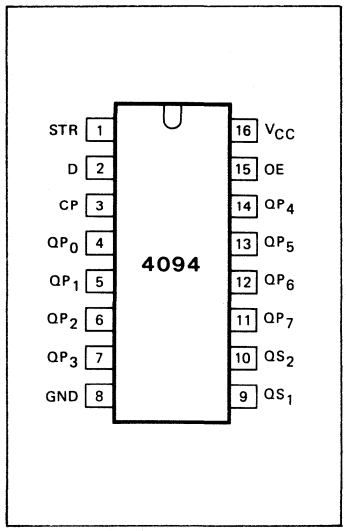

4059
CP 1
LE 2
J1 3
J2 4
J3 5
J4 6
J16 7
J15 8
J14 9
J13 10
S3 11
GND 12
24 VCC
23 Q
22 J5
21 J6
20 J7
19 J8
18 J9
17 J10
16 J11
15 J12
14 S1
13 S2

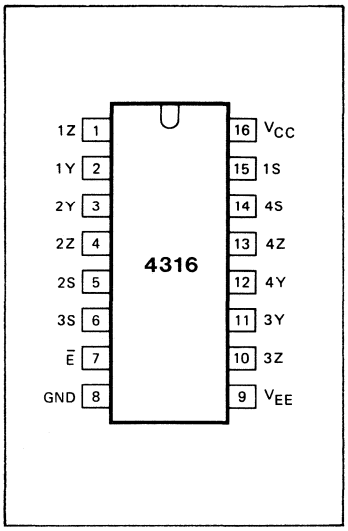

4060
Q11 1
Q12 2
Q13 3
Q5 4
Q4 5
Q6 6
Q3 7
GND 8
16 VCC
15 Q9
14 Q7
13 Q8
12 MR
11 RS
10 RTC
9 CTC
7Z93320

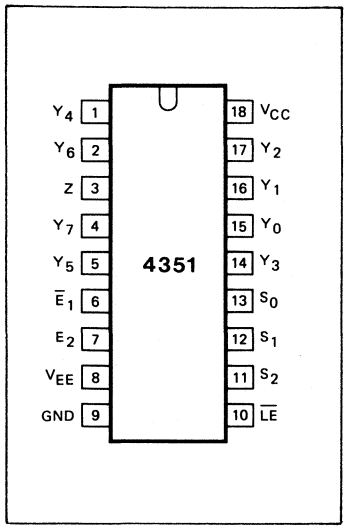

4066
1Y 1
1Z 2
2Z 3
2Y 4
2E 5
3E 6
GND 7
14 VCC
13 1E
12 4E
11 4Y
10 4Z
9 3Z
8 3Y

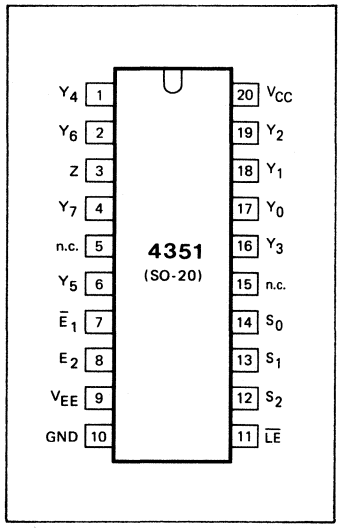

4067
Z 1
Y7 2
Y6 3
Y5 4
Y4 5
Y3 6
Y2 7
Y1 8
Y0 9
S0 10
S1 11
GND 12
24 VCC
23 Y8
22 Y9
21 Y10
20 Y11
19 Y12
18 Y13
17 Y14
16 Y15
15 E
14 S2
13 S3

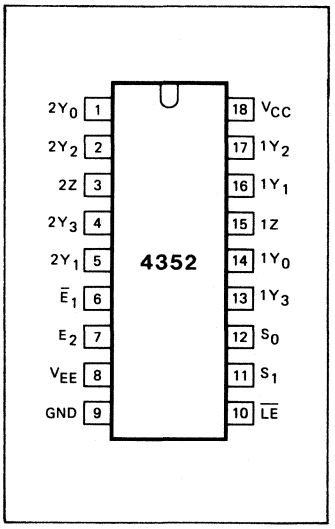

2A 1
2B 2
1A 3
1B 4
1C 5
1Y 6
GND 7
4075
14 VCC
13 3C
12 3B
11 3A
10 3Y
9 2Y
8 2C
7Z87429.1

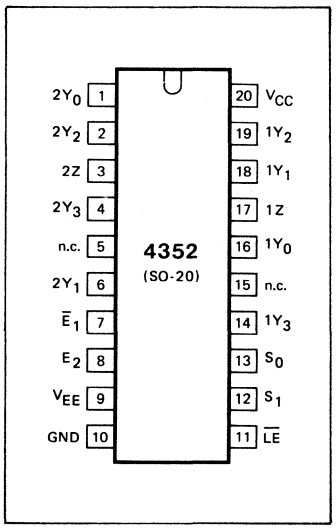

4094
STR 1
D 2
CP 3
QP0 4
QP1 5
QP2 6
QP3 7
GND 8
16 VCC
15 OE
14 QP4
13 QP5
12 QP6
11 QP7
10 QS2
9 QS1

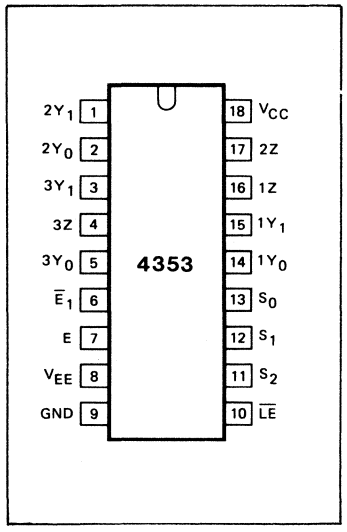

4316
1Z 1
1Y 2
2Y 3
2Z 4
2S 5
3S 6
E 7
GND 8
16 VCC
15 1S
14 4S
13 4Z
12 4Y
11 3Y
10 3Z
9 VEE

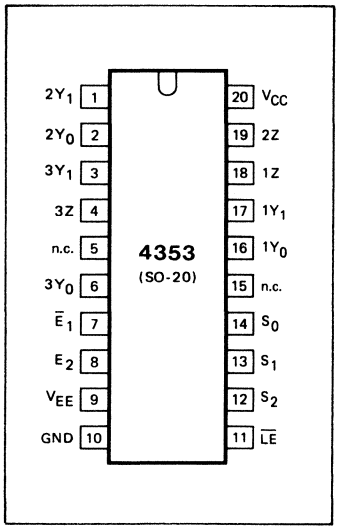

4351
Y4 1
Y6 2
Z 3
Y7 4
Y5 5
E1 6
E2 7
VEE 8
GND 9
18 VCC
17 Y2
16 Y1
15 Y0
14 Y3
13 S0
12 S1
11 S2
10 LE

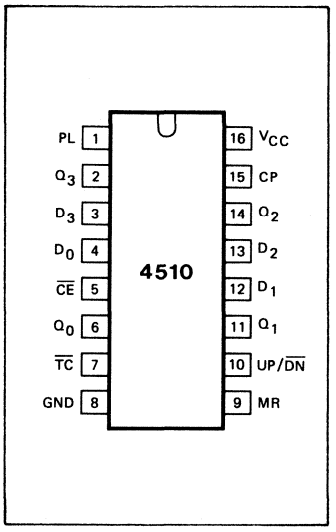

4351
(SO-20)
Y4 1
Y6 2
Z 3
Y7 4
n.c. 5
Y5 6
E1 7
E2 8
VEE 9
GND 10
20 VCC
19 Y2
18 Y1
17 Y0
16 Y3
15 n.c.
14 S0
13 S1
12 S2
11 LE

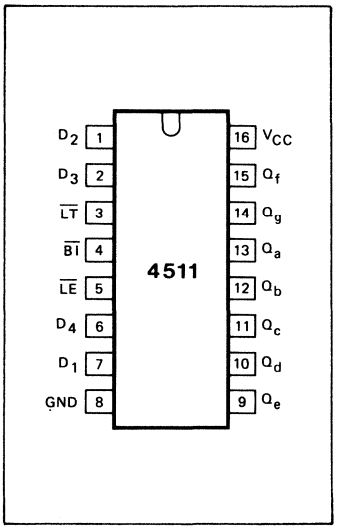

4352
2Y0 1
2Y2 2
2Z 3
2Y3 4
2Y1 5
E1 6
E2 7
VEE 8
GND 9
18 VCC
17 1Y2
16 1Y1
15 1Z
14 1Y0
13 1Y3
12 S0
11 S1
10 LE

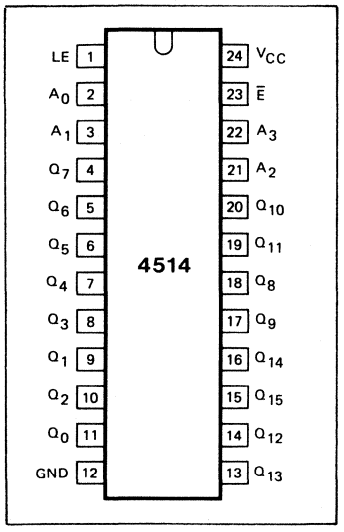

4352
(SO-20)
2Y0 1
2Y2 2
2Z 3
2Y3 4
n.c. 5
2Y1 6
E1 7
E2 8
VEE 9
GND 10
20 VCC
19 1Y2
18 1Y1
17 1Z
16 1Y0
15 n.c.
14 1Y3
13 S0
12 S1
11 LE

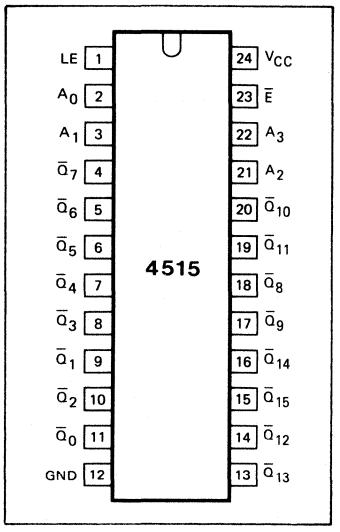

4353
2Y1 1
2Y0 2
3Y1 3
3Z 4
3Y0 5
E1 6
E 7
VEE 8
GND 9
18 VCC
17 2Z
16 1Z
15 1Y1
14 1Y0
13 S0
12 S1
11 S2
10 LE

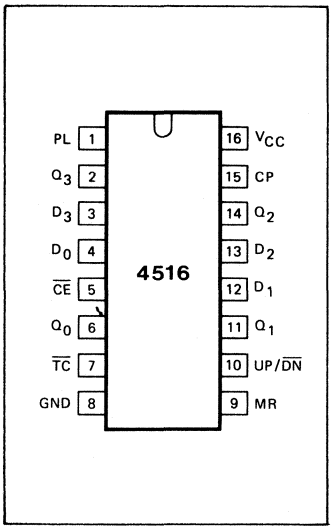

4353
(SO-20)
2Y1 1
2Y0 2
3Y1 3
3Z 4
n.c. 5
3Y0 6
E1 7
E2 8
VEE 9
GND 10
20 VCC
19 2Z
18 1Z
17 1Y1
16 1Y0
15 n.c.
14 S0
13 S1
12 S2
11 LE


4510
PL 1
Q3 2
D3 3
D0 4
CE 5
Q0 6
TC 7
GND 8
16 VCC
15 CP
14 Q2
13 D2
12 D1
11 Q1
10 UP/DN
9 MR


4511
D2 1
D3 2
LT 3
BI 4
LE 5
D4 6
D1 7
GND 8
16 VCC
15 Qf
14 Qg
13 Qa
12 Qb
11 Qc
10 Qd
9 Qe


4514
LE 1
A0 2
A1 3
Q7 4
Q6 5
Q5 6
Q4 7
Q3 8
Q1 9
Q2 10
Q0 11
GND 12
24 VCC
23 E
22 A3
21 A2
20 Q10
19 Q11
18 Q8
17 Q9
16 Q14
15 Q15
14 Q12
13 Q13


4515
LE 1
A0 2
A1 3
Q7 4
Q6 5
Q5 6
Q4 7
Q3 8
Q1 9
Q2 10
Q0 11
GND 12
24 VCC
23 E
22 A3
21 A2
20 Q10
19 Q11
18 Q8
17 Q9
16 Q14
15 Q15
14 Q12
13 Q13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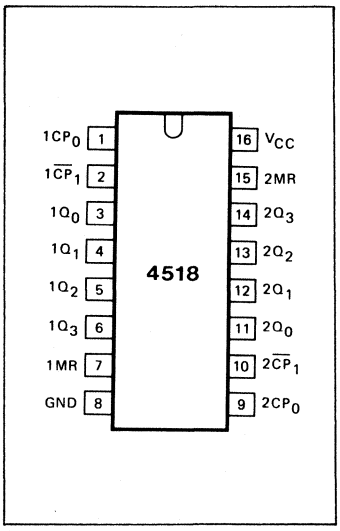
PL 1
Q3 2
D3 3
D0 4
CE 5
Q0 6
TC 7
GND 8
16 VCC
15 CP
14 Q2
13 D2
12 D1
11 Q1
10 UP/DN
9 MR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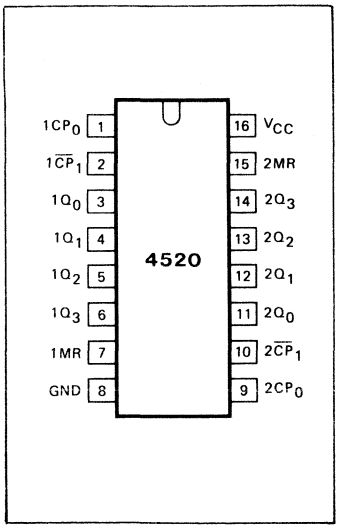
1CP1 2
1Q0 3
1Q1 4
1Q2 5
1Q3 6
1MR 7
GND 8
16 VCC
15 2MR
14 2Q3
13 2Q2
12 2Q1
11 2Q0
10 2CP1
9 2CP0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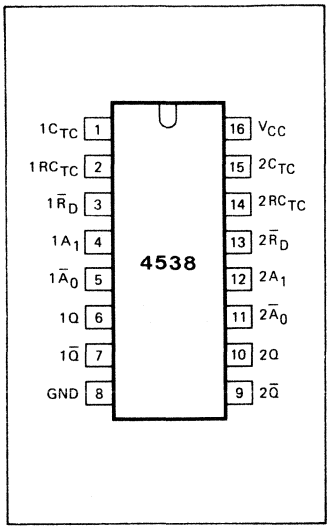
1CP1 2
1Q0 3
1Q1 4
1Q2 5
1Q3 6
1MR 7
GND 8
16 VCC
15 2MR
14 2Q3
13 2Q2
12 2Q1
11 2Q0
10 2CP1
9 2CP0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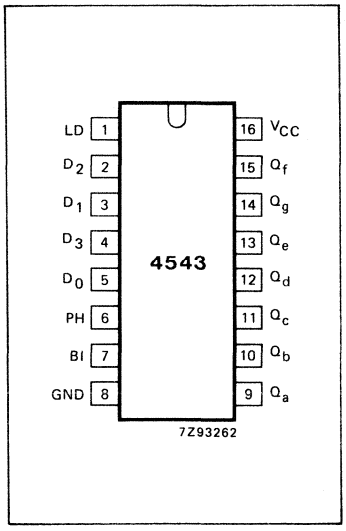
1CTC 1
1RCTC 2
1RD 3
1A1 4
1A0 5
1Q 6
1Q 7
GND 8
16 VCC
15 2CTC
14 2RCTC
13 2RD
12 2A1
11 2A0
10 2Q
9 2Q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LD 1
D2 2
D1 3
D3 4
D0 5
PH 6
BI 7
GND 8
16 VCC
15 Qf
14 Qg
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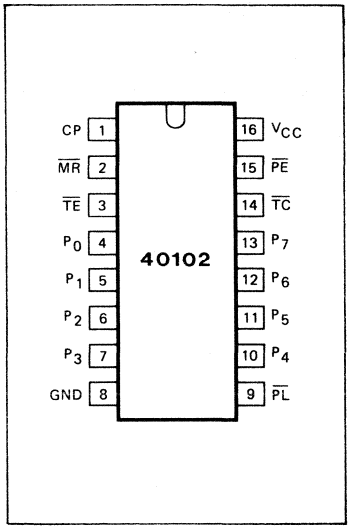
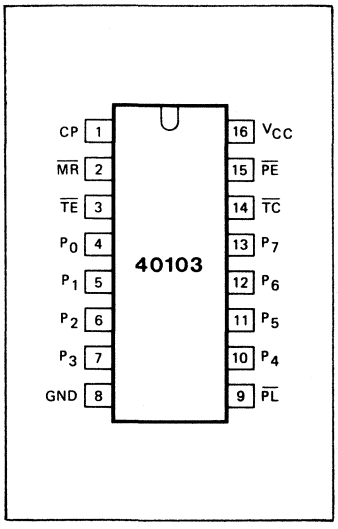
12 Qd
11 Qc
10 Qb
9 Qa
7Z93262


40102
CP 1
MR 2
TE 3
P0 4
P1 5
P2 6
P3 7
GND 8
16 VCC
15 PE
14 TC
13 P7
12 P6
11 P5
10 P4
9 PL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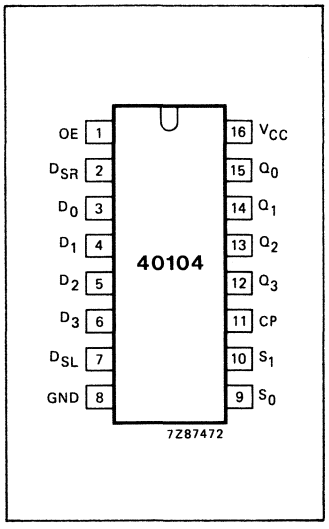
CP 1
MR 2
TE 3
P0 4
P1 5
P2 6
P3 7
GND 8
16 VCC
15 PE
14 TC
13 P7
12 P6
11 P5
10 P4
9 PL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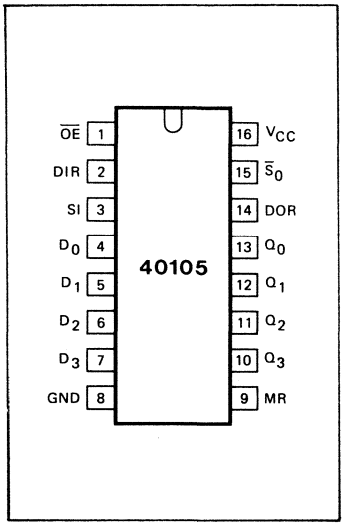
OE 1
DSR 2
D0 3
D1 4
D2 5
D3 6
DSL 7
GND 8
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 CP
10 S1
9 S0
7Z87472


40105
OE 1
DIR 2
SI 3
D0 4
D1 5
D2 6
D3 7
GND 8
16 VCC
15 S0
14 DOR
13 Q0
12 Q1
11 Q2
10 Q3
9 MR

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USER GUIDE

INTRODUCTION

The PC54/74 family is a comprehensive range of high-speed CMOS (HCMOS) integrated circuits. Whilst retaining all the advantages of CMOS technology - wide operating voltage range, very low power consumption, high input noise immunity and wide operating temperature range - they have the high-speed and drive capabilities of low-power Schottky TTL (LSTTL). These performance parameters, together with an extensive product range (most TTL functions and some popular devices from the successful HE4000B series - analog multiplexers, long time- constant multivibrators, phase-locked-loops) opens new avenues of possibility in system design.

For comparison, the key performance parameters of HCMOS are shown with those of other technologies in Table 1 and Fig. 1. It can be seen that metal-gate CMOS CD4000B was too slow for many applications and that our HE4000B series offered a solution without sacrificing the best qualities of CMOS. Now, our 3 μm gate HCMOS technology gives speeds comparable to LSTTL and still retains the important CMOS qualities.

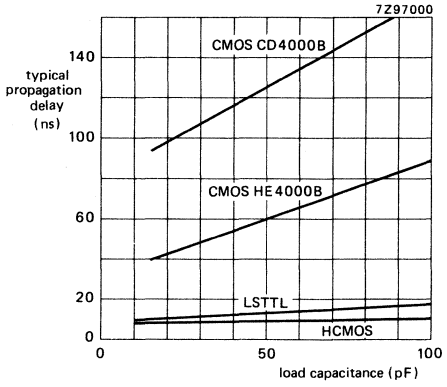


Fig. 1 Propagation versus load capacitance; V_{CC} = 5 V, T_{amb} = 25 °C.

Table 1 Comparison of performance parameters
Supply voltage V_{CC} = 5 V; ambient temperature T_{amb} = 25 °C; load capacitance C_L = 15 pF

parameters / technology		HCMOS	metal gate CMOS	standard TTL	low-power Schottky TTL	Schottky TTL	advanced low-power Schottky TTL	advanced Schottky TTL	Fairchild advanced Schottky TTL
	family	74HC	4000 CD HE	74	74LS	74S	74ALS	74AS	74F
Power dissipation (mW)									
Gate	static	0.0000025	0.001	10	2	19	1.2	8.5	5.5
	dynamic @ 100 kHz	0.075	0.1	10	2	19	1.2	8.5	5.5
Counter	static	0.000005	0.001	300	100	500	60	–	190
	dynamic @ 100 kHz	0.125	0.120	300	100	500	60	–	190
Propagation delay (ns)									
Gate	typical	7	94 40	10	9.5	3	4	1.5	3
	maximum	14	190 80	20	15	5	7	2.5	4
Delay/power product (pJ)									
Gate	at 100 kHz	0.52	9 4	100	19	57	4.8	13	16.5
Maximum clock frequency (MHz)									
D-type flip-flop	typical	55	4 12	25	33	100	60	160	125
	minimum	30	2 6	15	25	75	40	–	100
Counter	typical	45	2 6	32	32	70	45	–	125
	minimum	25	1 3	25	25	40	–	–	100
Output drive (mA)									
	standard outputs	4	0.51 0.8	16	8	20	8	20	20
	bus outputs	6	1.6	48	24	64	24	48	64
Fan-out (LS-loads)									
	standard outputs	10	1 2	40	20	50	20	50	50
	bus outputs	15	4	120	60	160	60	120	160

Our very fast 3 μm gate HCMOS family is a result of a continuing development programme to enhance the proven polysilicon-gate process. The CMOS evolution is depicted in Fig. 2 which shows a basic inverter with 6 μm gate from the HE4000B series and its 3 μm gate HCMOS successor; the electrical equivalent is shown in Fig. 3.

The switching speed of a CMOS inverter is related to inherent parasitic capacitance and current-drive capability. In HCMOS, parasitic capacitance is reduced by smaller clearances, and available charge/discharge currents are increased by smaller gate-lengths and thinner gate-oxides. The features and characteristics obtained with this enhanced process are discussed in the following paragraphs.

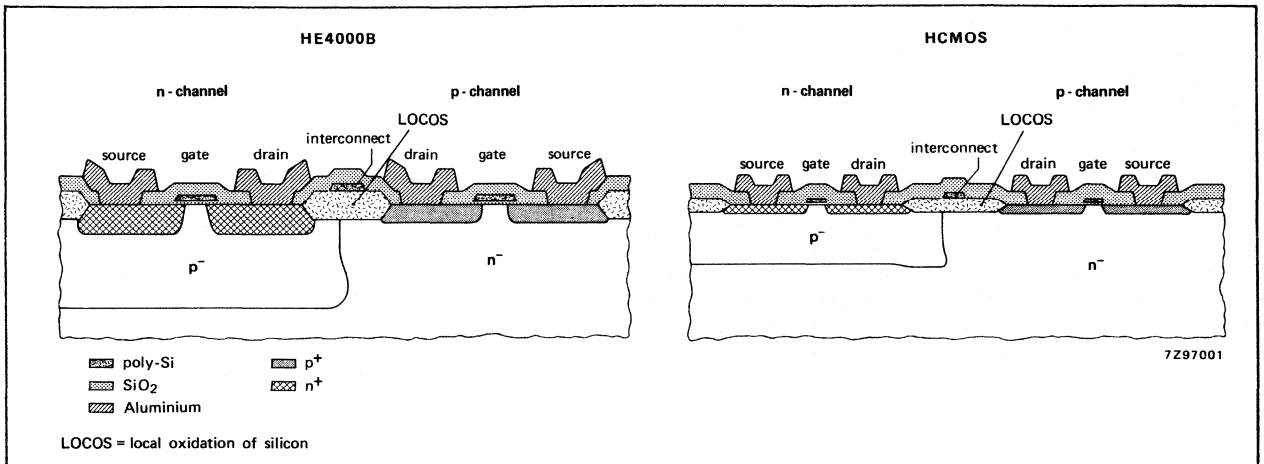


Fig. 2 Proccess comparison showing cross-sections of basic inverters from HCMOS and HE4000B families.

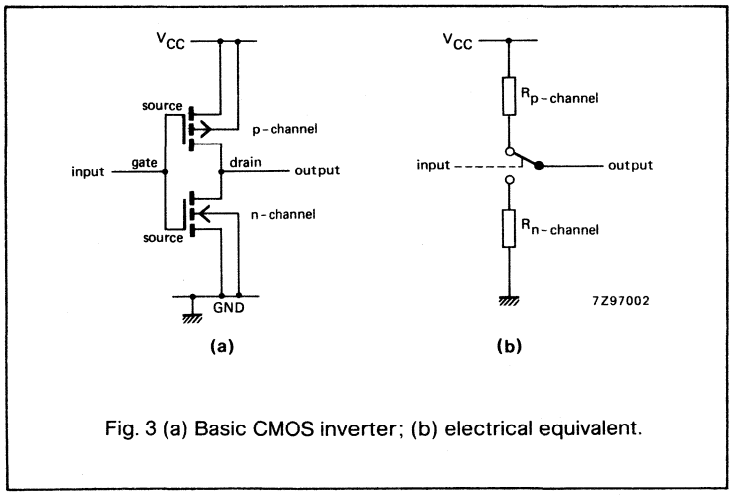


Fig. 3 (a) Basic CMOS inverter; (b) electrical equivalent.

Note: The information in this section is intended as a design-aid and does not constitute a guarantee.

AC CHARACTERISTICS

Test conditions

Performance parameters of the HCMOS PC54/74 family are guaranteed when devices are tested according to the conditions stated in the 'a.c. test circuits and waveforms' section of this publication. For some devices the test conditions are defined further by a.c. set-up requirements as, for example, with counters and flip-flops where set- up and hold times are involved.

Values given in the data sheets are for the whole operating temperature range and the supply voltages used are 2.0 V, 4.5 V and 6.0 V for HC, and 4.5 V for HCT devices. All a.c. characteristics are guaranteed for a capacitive test load of 50 pF, a more practical value than the favoured 15 pF load for it allows leeway in dealing with stray capacitance and loads the device during rising and falling transitions. The values given closely resemble those of a typical application and provide the designer with directly representitive delay figures.

Propagation delays and transition times

A key feature of the PC54/74 family is its speed, as this is generally comparable with equivalent circuits from the LSTTL range. The symmetrical push-pull output structure of both HC and HCT types gives symmetrical rise/fall times and provides for a well-balanced design. The influence of capacitive loading on output transitions is shown graphically in Fig. 4, and Table 2 gives extrapolation formulae for typical output transition times.

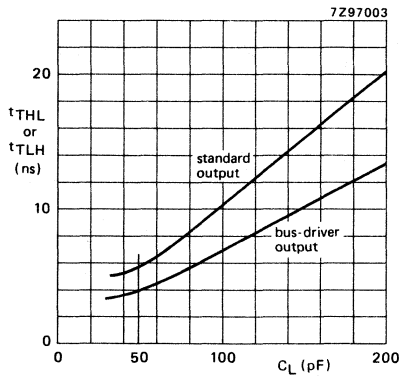
Table 2 Extrapolation formulae for typical output transition times for values of capacitance above the 50 pF standard load

V_{CC}	standard output*	bus-driver output*
2.0 V	18.5 ns + 0.32 ns/pF	12.5 ns + 0.22 ns/pF
4.5 V	6.6 ns + 0.12 ns/pF	4.5 ns + 0.077 ns/pF
6.0 V	5.6 ns + 0.10 ns/pF	3.8 ns + 0.065 ns/pF

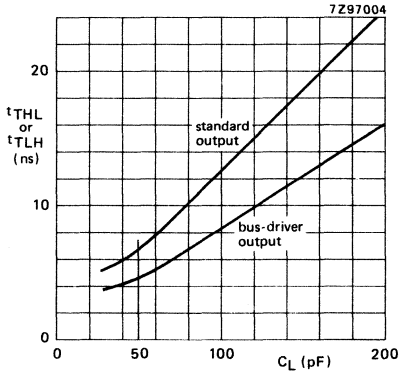
* $t_{THL} = t_{TLH}$

One of the parameters specified for TTL devices is the output short-circuit current HIGH (I_{OS}). Originally intended to reassure the TTL user that the circuit would withstand accidental grounding, this parameter became a measure of the ability of the circuit to charge the line capacitance and used in the calculation of propagation delay times. In CMOS, however, there is no need for I_{OS} because the purely capacitive loads allow extrapolation of a.c. parameters over the whole loading range. Graphs showing increases in delay timing with capacitive loading are given in Figs 5 and 6. The additional propagation times for loads greater than 50 pF can be calculated from the output saturation current (short-circuit current). Referring to the output characteristics (Figs 26 to 29), the propagation time is the time taken for the voltage to reach 50% of V_{CC} for HC devices, or 1.3 V for HCT devices. Also, as the output transistors act as current sources when operating in their saturation region, the additional delay time can be calculated from the formula $\Delta t = \Delta CV/I$; where ΔC is the difference in capacitance from 50pF, V is the voltage swing at the output to the switching level of the next device, and I is the average source current of the saturated output.

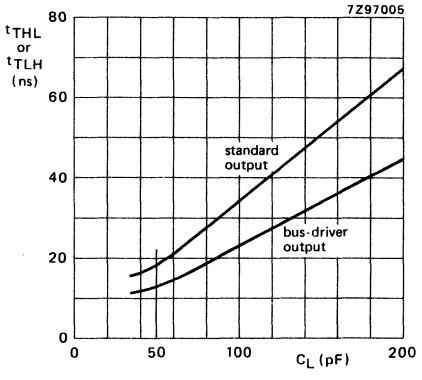
The influence of supply voltage on propagation time and operating frequency is shown in Figs 7 and 8.



(a) V_{CC} = 6 V

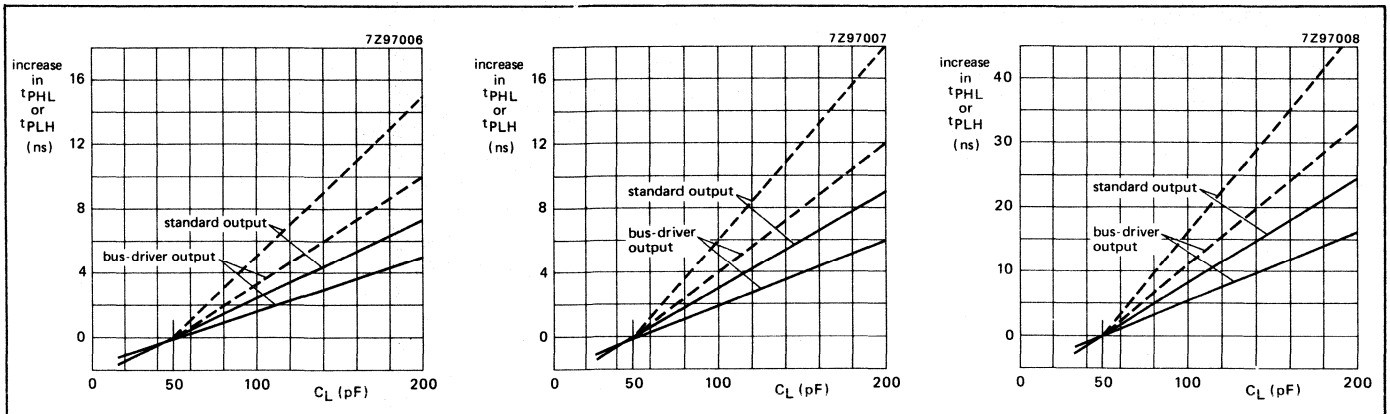


(b) V_{CC} = 4.5 V



(c) V_{CC} = 2 V

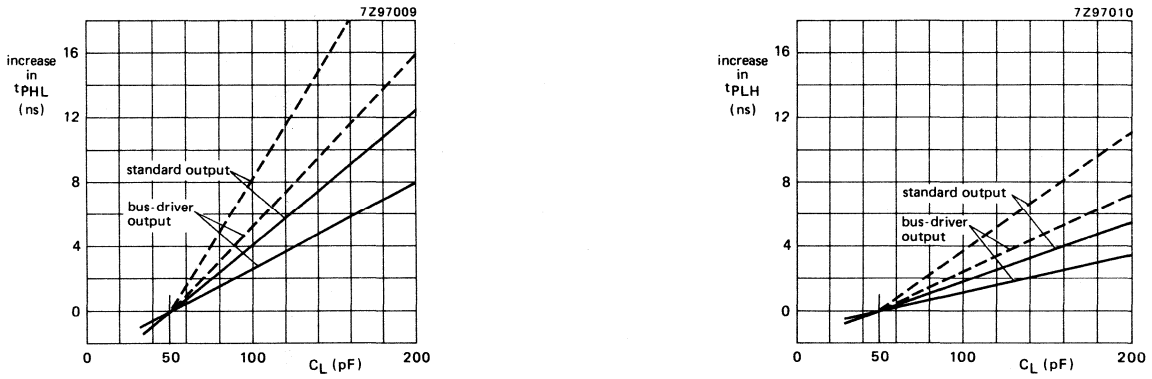
Fig. 4 Typical output transition times versus load capacitance; T_{amb} = 25 °C; HCT devices at V_{CC} = 4.5 V only.



(a) V_{CC} = 6 V (b) V_{CC} = 4.5 V (c) V_{CC} = 2 V

- - - - - expected maximum
——— typical value

Fig. 5 Increase in propagation delay time of HC devices versus load capacitance; T_{amb} = 25 °C.



(a) HIGH-to-LOW transition (b) LOW-to-HIGH transition

- - - - - expected maximum
——— typical value

Fig. 6 Increase in propagation delay time of HCT devices versus load capacitance; the different values for t_{HL} and t_{LH} are due to the asymmetrical reference level of 1.3 V at the outputs; T_{amb} = 25 °C; V_{CC} = 4.5 V.

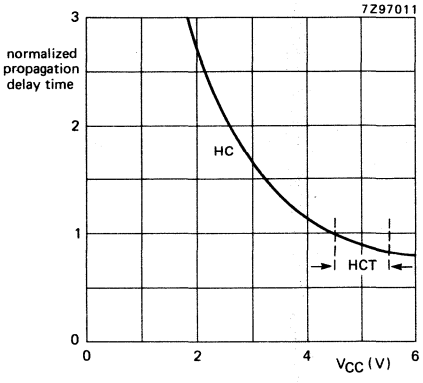


Fig. 7 Propagation time versus supply voltage; T_{amb} = 25 °C; C_L = 50 pF.

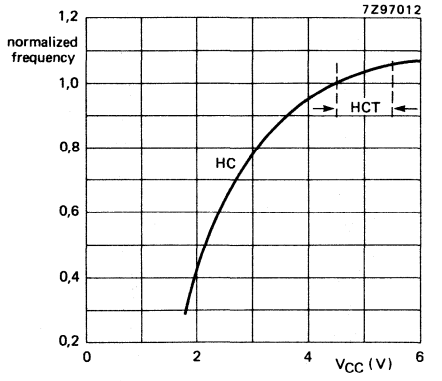


Fig. 8 Operating frequency versus supply voltage; T_{amb} = 25 °C; C_L = 50 pF.

AC CHARACTERISTICS (continued)

Temperature effect

Temperature dependence of HCMOS is much simpler than that of TTL where three factors contribute; increasing temperature causes increasing beta, increasing resistance values and decreasing junction forward-voltage drops. In HCMOS essentially only the carrier mobility changes with temperature, this affects the impedance and hence the delay time.

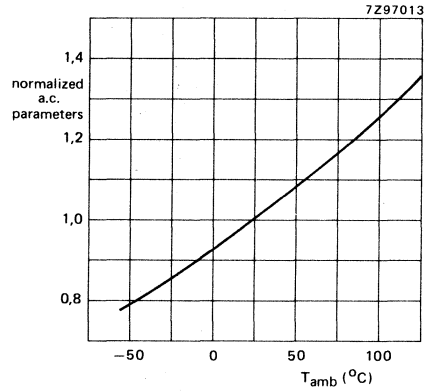


Fig. 9 Typical effect of temperature on a.c. parameters; V_{CC} = 5 V.

Clock pulse requirements

All HCMOS flip-flops and counters contain master-slave devices with level-sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of voltage threshold levels for clocking is an improvement over a.c. coupled clock inputs but it does not make the devices totally insensitive to clock-edge rates. The threshold level for HC devices is typically 50% of V_{CC} and that for HCT devices is 28% of V_{CC} (1.4 V at V_{CC} = 5 V). Temperature has little effect on the clock threshold levels.

When clocking occurs, the internal gates and output circuits of the device dump current to ground. This results in a noise transient that is equal to the algebraic sum of internal and external ground plane noise. When a number of loaded outputs change at the same time, it is possible for the chip ground reference level (and therefore the clock reference level) to rise by as much as 500 mV. If the clock input of a positive-edge triggered device is at, or near to its threshold level during a noise transient period, multiple triggering can occur. To prevent this, the rise and fall times of the clock inputs should be less than the data sheet maximum value (500ns at V_{CC} = 4.5 V).

In the HCMOS family, all the J-K flip-flops have a Schmitt-trigger circuit at their clock input and this eliminates the maximum limit of rise/fall time on the clock waveform. The flip-flops HC/HCT 73, 74, 107, 109 and 112 have special Schmitt-trigger circuits which increase their tolerance to slow rise/fall times and to high levels of ground noise.

POWER DISSIPATION

Static

In static conditions, the p-channel and n-channel transistors do not conduct at the same time, thus only leakage current flows from the positive V_{CC} to the negative GND supply connections. This leakage current is very low, typically a few nA, making HCMOS power consumption figures attractively low.

Static power dissipation is calculated, for both HC and HCT types, from the quiescent current maximum specified in the data sheets.

Dynamic

When an operating device is clocked, power is consumed in charging and discharging on-chip parasitic and load capacitances. Power is also consumed at the moment of transition when both p-type and n-type transistors are partially conducting, but this transient energy loss is typically only 10% of that lost through parasitic capacitance.

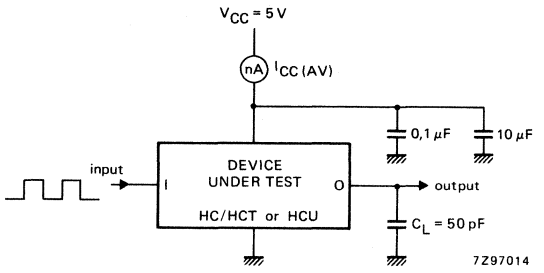
Dynamic power consumption (P_D) is proportional to the clocking frequency, to the load capacitance and to the square of the supply voltage, and is given by the formula:

$$P_D = C_{PD}V_{CC}^2f_i + \Sigma(C_LV_{CC}^2f_o) \quad (1)$$

The Σ term means summing the effective output load capacitance and frequency and this can be done by taking, per output, the product of the load capacitance and its frequency. The resulting calculation is most accurate when each device on a circuit board is considered in this way. A simpler approach is to use a C_{PD} that is the sum of C_{PD} and load capacitance for all HCMOS ICs on the circuit board and then, assuming an average frequency, apply formula (1).

For one-shot circuits, gates configured as oscillators, phase-lock loops and devices used in a linear mode, additional losses occur due to static currents and these are given in the device data sheets.

The equivalent power dissipation capacitance, C_{PD}, is specified in the device data sheets and the parameter given is a simplification of the worst-case operating mode of the device in typical operating conditions. The test set-up for determination of C_{PD} is shown in Fig. 10.



Input pulse = square wave with $t_r = t_f \leqslant 6$ ns between V_{CC} and GND.

All swiching outputs loaded with 50 pF (including any jig capacitance).

Unused inputs are connected to V_{CC} or GND.

Fig. 10 Test set-up for determination of C_{PD}.

The recommended test frequency for the determination of C_{PD} is 1 MHz, but this is best increased to 10 MHz when I_{CC} is low and the device quiescient current influences $I_{CC(AV)}$. Loading of the switched outputs gives a more practical value of C_{PD} (if the outputs are not loaded, transient 'through-currents' occur in the output stages).

The C_{PD} calculation is performed as follows:

$$I_{D(device)} = I_{CC(AV)} - I_{D(load)}$$

$$I_{D(load)} = \Sigma(C_LV_{CC}f_o)$$

$$C_{PD} = \frac{I_{D(device)}}{V_{CC}f_i}$$

Conditions for C_{PD} tests

The values of C_{PD} given in the data sheets are obtained in tests that comply with the conditions described in the following paragraphs. The worst case for C_{PD} is always chosen and the maximum amount of internal and output circuits are toggled simultaneously, within the constraints listed in the data sheet.

Gates. All inputs except one are held at either V_{CC} or GND, depending on which state causes the output to toggle. The remaining input is toggled at a known frequency and C_{PD} is given on a per- gate basis.

Decoders. One input is toggled to cause the outputs to toggle at the same rate (normally one of the address-select pins is switched while the decoder is enabled). All other inputs are tied to V_{CC} or GND, whichever enables operation. The C_{PD} value is given on a per-independent-decoder basis.

Multiplexers. One data input is tied HIGH and the other is tied LOW. The address-select and enable inputs are configured so that, by toggling one address input, the two data inputs are selected alternately causing the outputs to toggle. With three-state multiplexers, C_{PD} is given for enabled outputs and is measured per output function.

Three-state buffers and transceivers. C_{PD} is measured with outputs enabled on a per-buffer basis. Measurement is performed as for simple gates.

Latches. The device is clocked and data is toggled on alternate clock pulses. Other preset or clear inputs are held so that output toggling is enabled. If the device has common-locking latches then one latch is toggled by the clock. Three-state latches are measured with their outputs enabled. C_{PD} is given on a per-latch basis.

Flip-flops. Measurement is performed as for latches. The inputs to the device are configured to toggle and any preset or clear inputs are held inactive.

Shift registers. The register is clocked and the serial data input is toggled at alternate clock pulses (as described for latches). Clear and load inputs are held inactive and parallel data are held at V_{CC} or GND. Three-state devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to shift the data out and then reloaded.

Counters. A signal is applied to the clock input but other clear or load inputs are held inactive. Separate values for C_{PD} are given for each counter in the package.

Arithmetic circuits. Adders, magnitude comparators, encoders, parity generators, ALUs and miscellaneous circuits are exercised to obtain the maximum number of simultaneously toggling outputs when toggling only one or two inputs.

Display drivers. The C_{PD} value is not normally required for LED drivers because LEDs consume so much power as to make the effect of C_{PD} negligible. Moreover, when blanked, the drivers are rarely driven at significant speeds. For when it is needed, C_{PD} is measured with outputs enabled and disabled while toggling between lamp test and blank (if provided), or between a display of numbers 6 and 7.

LCD drivers are tested by toggling the phase inputs that control the segment and backplane waveforms outputs.

If either of the driver types (LCD or LED) has latched inputs, then the latches are set to a flow-through mode.

One-shot circuits. In some cases, when the device I_{CC} is significant, C_{PD} may not be specified. When it is specified, C_{PD} is measured by toggling one trigger input to make the output a squarewave. The timing resistor is tied to a separate V_{CC} supply to eliminate its power contribution.

Additional power dissipation in HCT devices

When the inputs of an HCT device are driven by a TTL device at the specified minimum of $V_{OH} = 2.4$ V, the input stage p-channel transistor does not completely switch off and there is an additional quiescent supply current (ΔI_{CC}). This current has been considerably reduced by proprietary development of the HCT input stages, the precise current path is shown in the HCT input stage description.

The value of ΔI_{CC} specified in the data sheets is at the worst-case input voltage of V_{CC}-2.1 V for the V_{CC} range 4.5 to 5.5 V, on a per-input basis. The value of 2.1 V is the maximum voltage drop across a TTL output HIGH (minimum V_{CC} and minimum V_{OH}).

The additional power dissipation is calculated using the formula:

$P = V_{CC} \times \Delta I_{CC} \times$ duty factor HIGH x unit load coefficient

Unit load coeffient for a particular input is a factor by which the value of ΔI_{CC} given in the data sheet has to be multiplied. This factor is given in the data sheet for each HCT input and correlates with the size of the input p-channel transistor.

Power consumption due to slow input rise and fall times

During switching transitions there is a brief period when both transistors of a transistor pair conduct. The resulting 'through-current' is additional to the normal supply current and causes power consuption to increase linearly with the input rise or fall time. As long as the input voltage is below the n-channel transistor threshold voltage, or is higher than V_{CC} minus the p-channel transistor threshold voltage, one of the input transistors is always in the OFF-state and no through-current flows.

When the input voltage equals the n-channel transistor threshold voltage (typ. 0.7 V), the n-channel transistor starts to conduct and through-current starts to flow. The supply current reaches a maximum at 0.5 V_{CC} for HC devices, and 28% V_{CC} for HCT devices; the value of the peak is determined by the geometry of the input transistors. The through-current is proportional to V_{CC}^n, in which $n > 2$. The supply current for a typical HCMOS input is shown as a function of input voltage transient in Fig. 11.

When squaring-up slow pulses by means of Schmitt triggers, through-current due to slow rise and fall times at the Schmitt-trigger inputs gives additional power dissipation.

By applying RC oscillators, or oscillators constructed with Schmitt triggers, the phenomenon described gives a frequency-independent power consumption.

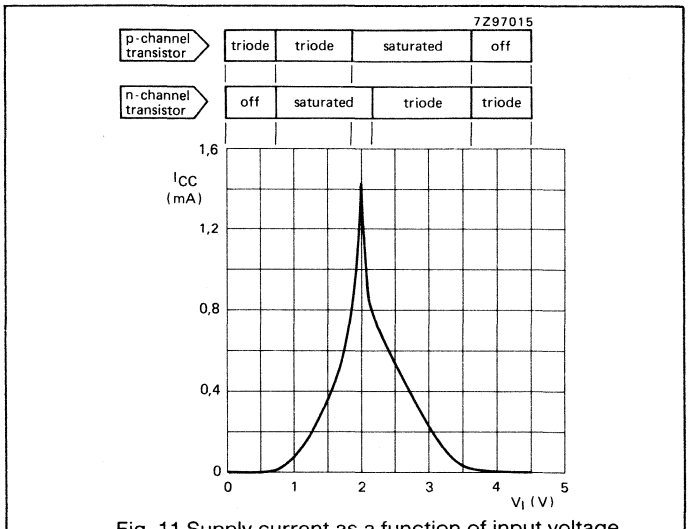


Fig. 11 Supply current as a function of input voltage.

SUPPLY VOLTAGE

Range

For new designs, HCMOS HC and HCU types are faster alternatives to the earlier CMOS types. The supply voltage lower limit is extended to 2 V to give an overall range of 2 to 6 V, bringing the important advantage of continued use of HCMOS with future generations of memories and microcomputers requiring supply voltages of less than 5 V. The 3:1 ratio between lower and upper supply voltage limits allows simpler power supplies, facilitates battery operation and allows lithium battery back-up. (For circuits operating in the linear mode, such as RC or crystal oscillators, a minimum supply of 3 V is recommended.)

HCMOS HCT types are pin-compatible with LSTTL circuits and are intended as replacements to reduce power consumption in existing circuits. The HCT circuits retain the traditional 5 V LSTTL supply but the voltage range is extended to ± 10% for both temperature ranges (-40 to + 85 °C for 74 prefix and -55 to + 125 °C for 54 prefix). This allows extended temperature range LSTTL devices to be replaced by standard temperature range HCMOS.

The maximum rated supply voltage is 7 V and any voltage above this may ruin the device, even though the on-chip diode break-down voltage is 18 V and the threshold voltage of parasitic thick-field oxide transistors is 15 V.

The V_{CC} and GND potentials must never be reversed as this can cause excessive currents to flow through the V_{CC}/GND diode circuits.

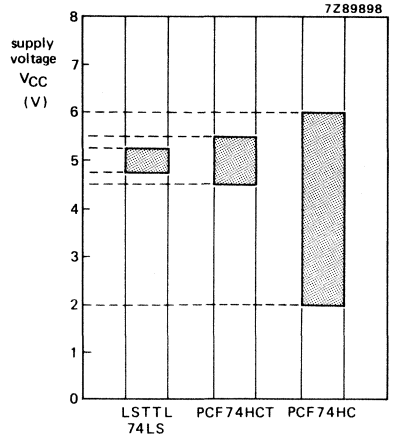


Fig. 12 Supply voltage ranges showing that HCMOS HCT devices have 5% more margin than standard range LSTTL (74LS), and that HCMOS HC devices operate with a supply voltage as low as 2 V.

Battery back-up

Battery back-up can be easily implemented in systems of HCMOS HC/HCU devices and an example of this is shown in Fig. 13. The minimum battery voltage required is only 2 V plus one diode drop.

In the example, HIGH-to-LOW level-shifters (HC4049 or HC4050) are used to prevent positive input currents into the system due to input voltage levels being greater than one diode drop above V_{CC}. If the circuit is such that input voltages can exceed V_{CC}, then external resistors should be included to limit input currents to 2 mA. External resistors may also be necessary in the output circuits where, if the output can be pulled above V_{CC} or below GND, the currents should be limited to 2 mA. These currents are due to inherent V_{CC}/GND diodes that are present in all outputs, including three-state outputs.

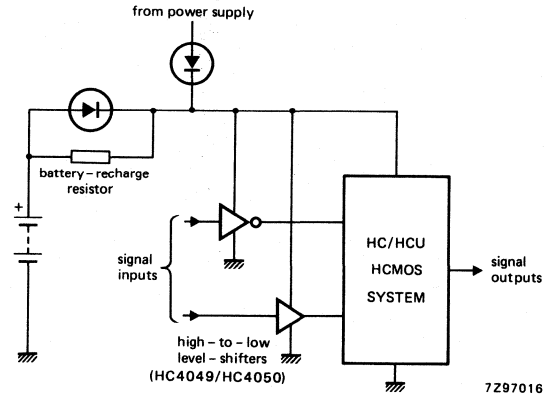


Fig. 13 Example of an HCMOS system with battery back-up.

Power supply regulation and decoupling

The wide power supply range of 2 to 6 V may suggest that voltage regulation is not necessary but it must be realized that a changing supply voltage affects system speed, noise immunity and power consumption. Noise immunity, and even the correct operation of the circuit, can be affected by noise spikes on the supply lines and therefore matched decoupling is always necessary in dynamic systems.

Both HC and HCT types have the same power supply regulation and decoupling requirements. The best method of minimizing spiking on the supply lines is by implementing good power supply and ground bussing and having low a.c. impedances from the V_{CC} and GND pins of each device. The minimum value of a decoupling capacitor depends on the voltage spikes that can be allowed and, as a general rule, it is satisfactory to restrict ground and V_{CC} noise peaks to 400 mV. A local voltage regulator on the printed circuit board can be decoupled using an electrolytic capacitor of 10 to 50 μF. Localized decoupling of devices can be provided by 22 nF per every two to five packages and a 1 μF tantalum capacitor for every ten packages. The V_{CC} line of bus driver circuits and level-sensitive devices can be efficiently decoupled from instantaneous loads by a 22 nF ceramic capacitor connected as close to the package as possible.

A practical example of determining the value of a decoupling capacitor follows: assume a buffer output sees a 100 Ω dynamic load and the output LOW-to-HIGH transition is 5 V, then the current demand is 50 mA per output. If it is an octal buffer, then the current demand would be 0.4 A per package in approximately 6 ns time.

To determine the value of a decoupling capacitor, a formula is derived as follows:

The instantaneous value of the term $Q = CV$ is given by $(\Delta Q/\Delta t) = C(\Delta V/\Delta t)$.

Since $\Delta Q/\Delta t = I$, the equation becomes $I = C(\Delta V/\Delta t)$.

Hence $C = (I\Delta t)/(\Delta V)$.

From the example of an octal buffer, assuming the change in V_{CC} to be 0.4 V, then

$C = (0.4\ A \times 6 \times 10^{-9} ns)/(0.4\ V) = 6 \times 10^{-9}\ F = 6\ nF$.

INPUT/OUTPUT PROTECTION

The gate input of any MOS transistor acts as a small value capacitor (< 1 pF) with very low leakage current (< 1 pA). Such inputs, if without special protection, could be electrostatically charged to a high voltage causing a destructive breakdown of the dialectric and permanent damage to the device.

The improved integration process of the PC54/74 family allows polysilicon to be used as a resistor structure at all inputs to slow down fast input transients caused by electrostatic discharge and to dissipate some of their energy. These resistors also ensure that the input impedance is at least 100 Ω under all biasing conditions, even when V_{CC} is short-circuited to GND - an improvement over direct input diode clamps that do not have this advantage during power-up.

The standard input protection comprises a series polysilicon resistor and two stages of diode clamping (Fig. 14). The diodes exhibit typical forward voltage drops of 0.9 V at 2 mA and reverse breakdown voltages of 18 V. In some applications such as oscillators, the diodes actually conduct during normal operation, in this case the input current should be limited to 2 mA.

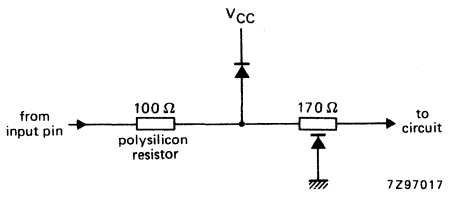


Fig. 14 Standard input protection of HC/HCT/HCU inputs against electrostatic discharge.

High-to-low level shifters HC4049 and HC4050 have a single-sided input protection network (Fig. 15). The diode D1 is the inherent drain-to-GND diode of the thick field oxide protection device. Under operating conditions this input may exceed the supply voltage V_{CC}.

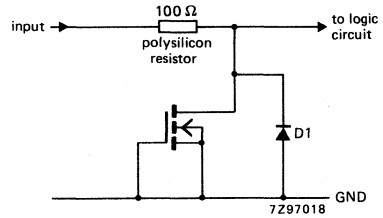


Fig. 15 Input protection for HC4049 and HC4050.

All input pins can sustain discharge tests to typically 2.5 kV (tests according to MIL-STD-883B, method 3015). The output configurations of standard, bus driver, three-state, open drain and I/O ports are typically above 3 kV because of the large diodes formed by the drain surfaces of the output transistors.

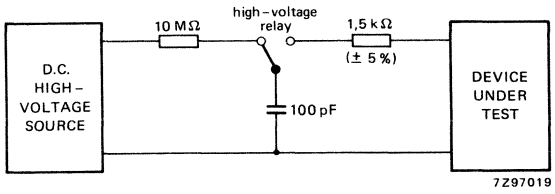


Fig. 16 Electrostatic discharge test circuit.

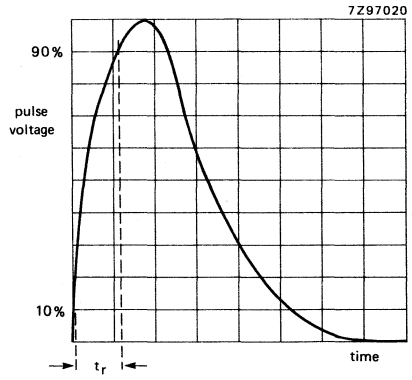


Fig. 17 Pulse waveform at device under test.

The rise time t_r in Fig. 17 is prescribed by MIL-STD-883B to be $\leqslant$ 15 ns but in practice it is helpful to adjust the test set-up to give 13 $\pm$ 2 ns to avoid correlation problems.

Although all inputs and outputs are protected against electrostatic discharge, the standard CMOS handling precautions should be observed (see 'Handling CMOS devices').

INPUT CIRCUITS

HC inputs

The HC input circuit (Fig. 18) includes the resistor/diode network for electrostatic discharge protection and clamps input voltages exceeding V_{CC} or GND. The circuit is intended for a.c. working and cannot handle heavy d.c. currents for long periods; a maximum input diode current of 2 mA is allowed for proper operational functioning.

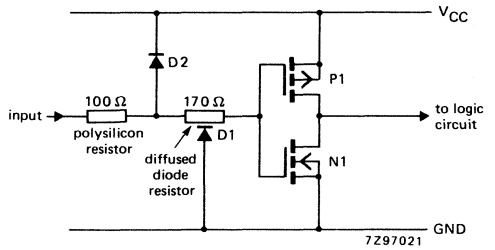


Fig. 18 HC input circuit.

The HC input circuit has no active input current; the only current flowing is across the reversed-biased diodes D1 and D2 and is typically in the nA region, reaching a maximum when $V_I = V_{CC}$ or GND.

The MOS transistors P1 (p-channel) and N1 (n-channel) have the same conductance when switched on, giving the device a typical switching point of 50% V_{CC}. The switching point moves very little with temperature because the current gain factor (β) and voltage threshold (V_T) of both N1 and P1 move in the same direction, a typical variation of the switching point as temperature changes from - 55 to + 125 °C is ± 60 mV. The only other factors that affect the switching point are the relative spreads of β and V_T of P1 and N1.

There is no current path from V_{CC} to GND when the input is lower than V_{TN}, or higher than V_{CC}-V_{TP}, since MOS transistors do not conduct when the input voltage is near V_{CC} or GND. However, when the input voltage is in the linear region, a static current path from V_{CC} to GND flows in the input stage (Fig. 11). This current is small enough to be neglegible under normal operating conditions when the input rise time $t_r \leqslant 15$ ns, but the power dissipation should be taken into account for devices used in the linear region. Due to the voltage gain of the input stage, no static flow-through current occurs in the second and subsequent stages. Small amounts of current do flow in these stages during operation when both n-channel and p- channel transistors conduct for brief periods and this factor is included in the C_{PD} value given in the data sheet.

All digital technology is prone to oscillation or premature triggering when very slow input rise and fall times are used. With the input hovering at or near to the switching point, noise on the line will be amplified and can cause oscillation and this, if the frequency is low enough, can cause succeeding stages to switch and give unexpected results. For this reason Schmitt-trigger devices are recommended if rise/fall times are likely to exceed 500 ns at V_{CC} = 5 V. The flip-flops with Schmitt-trigger action are HC/HCT 73, 74, 107, 109 and 112, the 14 and 132 are dedicated Schmitt triggers with specified input levels.

HCT inputs

The HCT input stage has characteristics similar to those of an HC input but the switching level is reduced to 1.4 V at V_{CC} = 5 V. The input circuit, shown in Fig. 19, has an enlarged n-channel transistor (N1) and a level-shift diode (D3) has been added. The natural voltage level of the drain of the p-channel transistor (P1) is approximately V_{CC}-0.6 Vbut when the input voltage is at a low level, an auxiliary pull-up transistor (P2) raises this to V_{CC} causing p-channel transistor P3 to completely cut off. The input stage is well balanced to the load of the second stage so that symmetrical propagation delays are obtained.

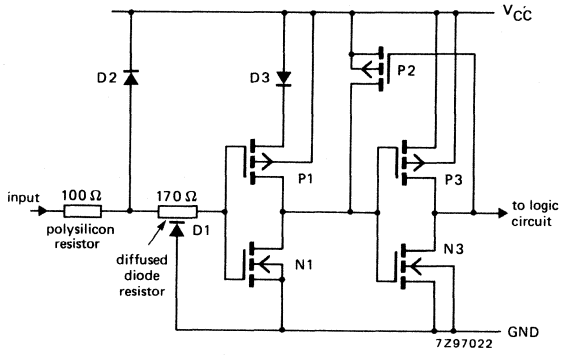


Fig. 19 HCT input circuit.

A TTL HIGH level can be as low as 2.4 V and, as an input of this order would not cut off P1 completely, additional supply current will flow through the input stage. Level-shift diode D3 together with the influence of the back-gate (substrate) connection to P1 minimizes power dissipation caused by this through-current and yields an input switching level compatible to LSTTL. The reduction in power achieved by D3 is depicted in Fig. 20 which shows the input stage through-current with and without the diode circuit.

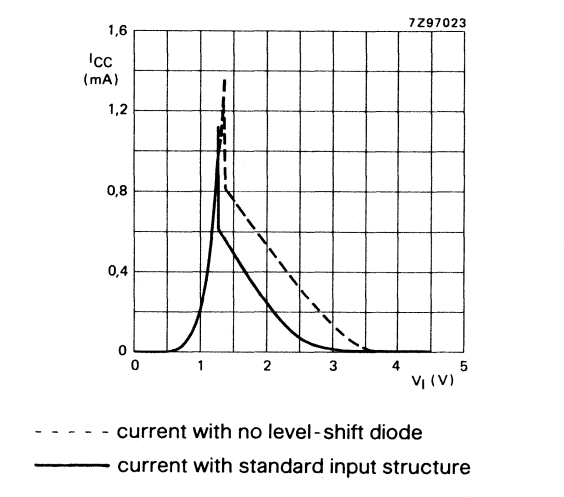


Fig. 20 HCT input through-current versus input voltage.

The input stage through-current is almost zero when a typical TTL HIGH level of 3.5 V is applied, thus this unique HCT input structure gives true CMOS low power-consumption when driven by TTL. Typical and worst-case through-currents are given in the data sheets on a per-input basis as ΔI_{CC}.

Unused inputs

For both HC and HCT types, all unused inputs should be connected to V_{CC} or GND, or tied to a well-defined HIGH or LOW level. This is to avoid excess through-currents flowing due to open-circuit inputs having a bias at or near to the switching level. Also, due to their high gain, buffered devices with open inputs can go into oscillation from noise in the system and this will cause an additional current drain. It is possible too that open inputs can degrade the switching speed of the device.

Input capacitance

Since CMOS inputs present essentially no load, their fan-out is limited only by their input capacitance. This is typically 3.5 pF and comprises package, bonding pad/interconnecting track, input protection diode and transistor gate capacitances. Typical input capacitances for powered HC and HCT devices are shown in Figs 21 and 22; the decrease that can be seen as V_I rises from zero or falls from 5 V is due to increased reverse bias on the protection diodes, the peaking is caused by internal Miller feedback capacitance that is active when the inverter is in its linear mode. A conservative value for maximum capacitance is 10 pF. Input capacitance is measured with all other inputs tied to ground.

Coupling of adjacent inputs

It is possible that parasitic bipolar pnp transistors are present between adjacent inputs, e.g. between the protection diode to V_{CC} and the same diode at the adjacent input, as shown in Fig. 23. If the recommended operating input voltage is exceeded, perhaps by ringing of more than 0.7 V, current flowing into the terminal (I_1) can cause the parasitic transistor to pass current (I_2) to the adjacent input (Fig. 24). As the I_2 current collected in the adjacent input has to be drained by the source driving that input, the ohmic value (R) of this source must be low. If R is not low enough, the parasitic current can lift the source voltage and cause unwanted switching.

The ratio of forced input current (I_1) to parasitic adjacent input current (I_2) is represented by

$$\alpha = (I_2)/(I_1)$$

This factor has been reduced to less than 0.05 in the PC54/74 family by careful implementation of layout (deep guard rings or bonding pad spacing).

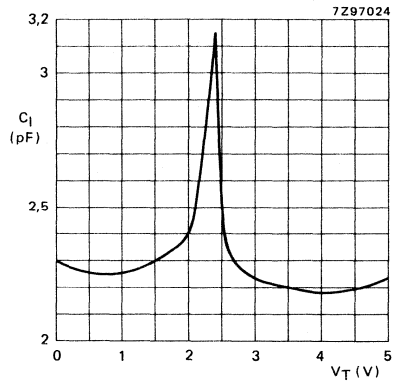


Fig. 21 Typical input capacitance of an HC device versus input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

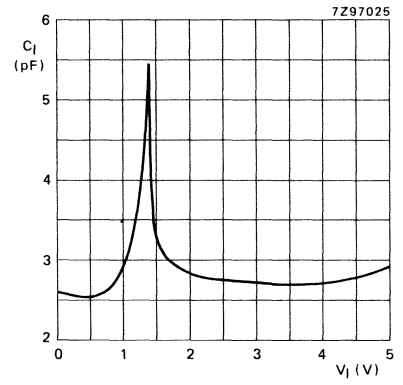


Fig. 22 Typical input capacitance of an HCT device versus input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

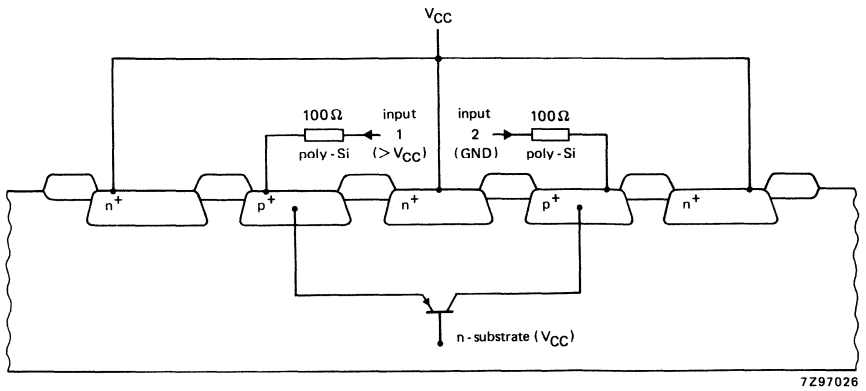


Fig. 23 Cross section of input protection showing parasitic pnp transistor.

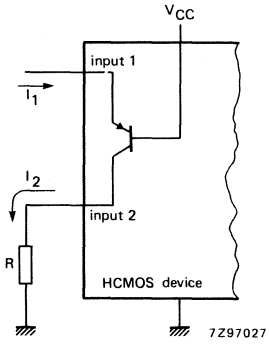


Fig. 24 Equivalent circuit of parasitic pnp transistor.

OUTPUT CIRCUITS

There are three different output configurations in the PC54/74 family: push-pull, three-state and open n-drain. Each of these can be as a standard output or as a bus driver (typically 1.5 times the current-handling capability of a standard output). All HC and HCT outputs are buffered to ensure consistency of output current drive and a.c. characteristics throughout the PC54/74 range. The output n-channel and p-channel transistors are of equal order so as to give symmetrical output rise and fall times.

To compare the output drive capabilities of HCMOS with those of LSTTL:

LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This guarantees that the worst-case low and high input thresholds will be met and the existing margins of noise immunity preserved.

HCMOS capability is expressed as source/sink current at a specified output voltage. Since HCMOS requires virtually no input current, the unit load concept does not apply.

With a specified output drive of 0.4 mA/0.4 V the HCMOS capability exceeds 1000 ULs, and with a 20 μA/0.1 V specification the HCMOS capability is 20 ULs. The drive capability of standard HCMOS outputs is that each can drive ten LSTTL loads and maintain $V_{OL} \leqslant 0.4$ V over the full temperature range. Bus driver outputs can drive 15 LSTTL loads under the same conditions. The output drive capabilities of HCMOS expressed in LSTTL unit loads are shown in Table 3.

Table 3 Comparison of output drive capabilities

LS device	output drive		HCMOS equiv.	type	output drive	
74LS00	4 mA	10 UL	74HC00	standard	4 mA	10 UL
74LS138	4 mA	10 UL	74HC138	standard	4 mA	10 UL
74LS245	12 mA	30 UL	74HC245	bus	6 mA	15 UL
74LS374	12 mA	30 UL	74HC374	bus	6 mA	15 UL

Output current derating versus temperature is shown in Fig. 25 and is valid for all types of output. Output source and sink drives at V_{CC} = 2, 4.5, and 6 V are given in Figs 26 to 29 which show output currents versus output voltages; these graphs indicate the typical and minimum output currents that can be expected and can serve as a design aid in calculating transmission line effects on charging highly capacitive loads.

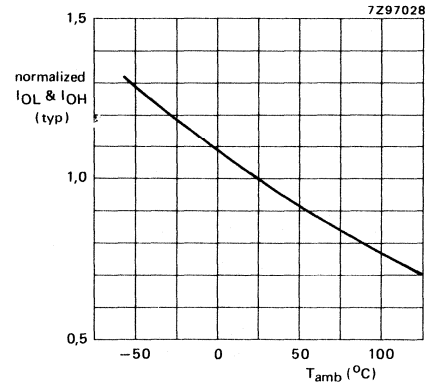
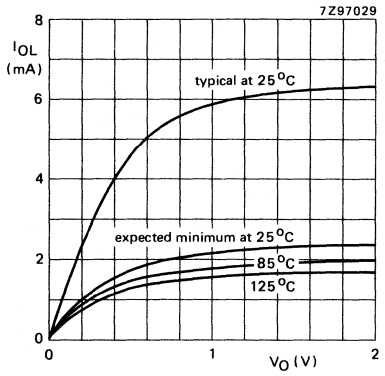
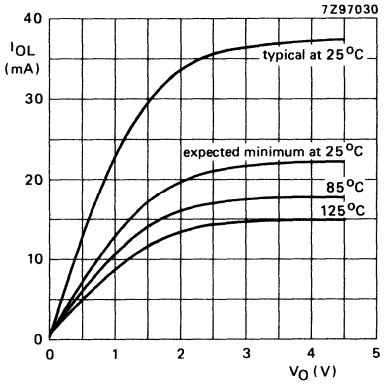


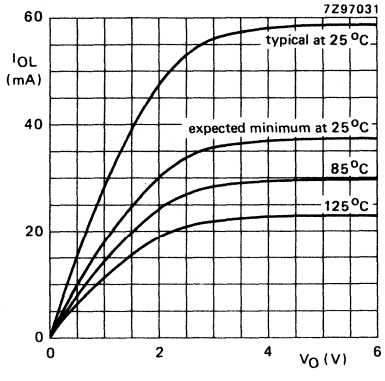
Fig. 25 Normalized temperature effect on output drive I_{OL} and I_{OH}.



(a) V_{CC} = 2 V



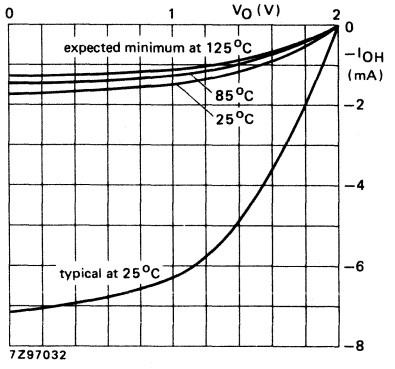
(b) V_{CC} = 4.5 V



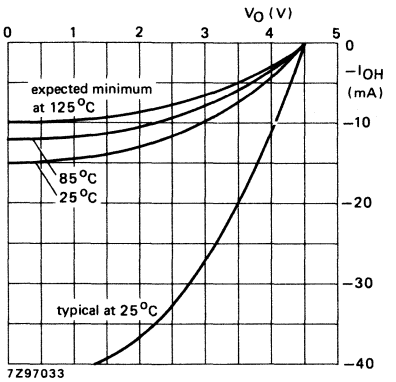
(c) V_{CC} = 6 V

Fig. 26 Standard output n-channel sink current.

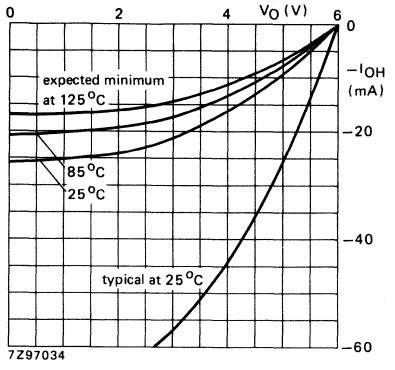
Note to Figs 26 to 29. The expected minimum curves are included as an aid to design and are not guaranteed.



(a) V_{CC} = 2 V

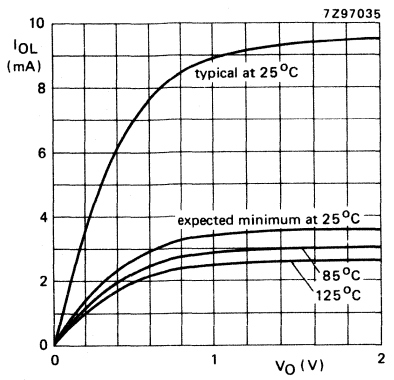


(b) V_{CC} = 4.5 V

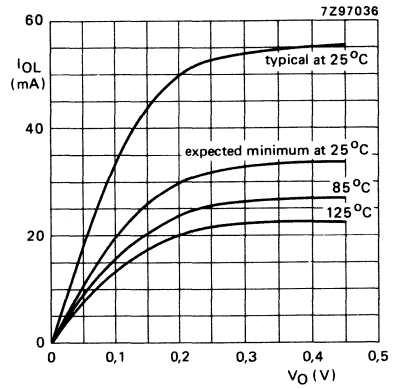


(c) V_{CC} = 6 V

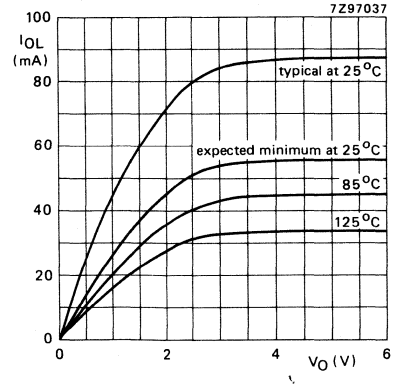
Fig. 27 Standard output p-channel source current.



(a) V_{CC} = 2 V

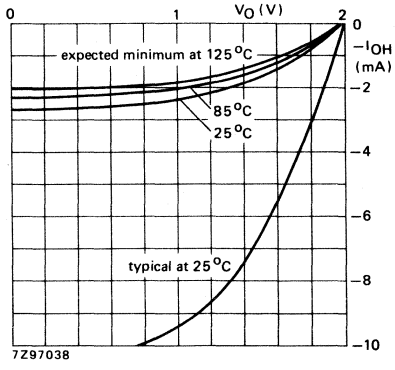


(b) V_{CC} = 4.5 V

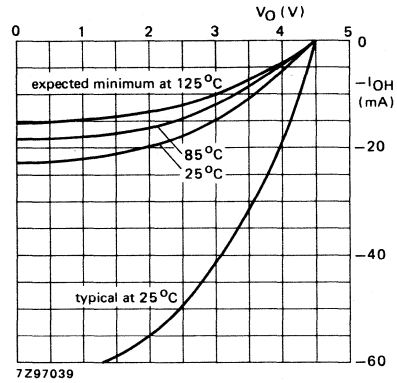


(c) V_{CC} = 6 V

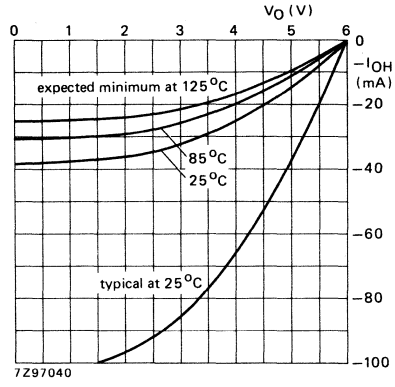
Fig. 28 Bus-driver output n-channel sink current.



(a) V_{CC} = 2 V



(b) V_{CC} = 4.5 V



(c) V_{CC} = 6 V

Fig. 29 Bus-driver output p-channel source current.

Push-pull outputs

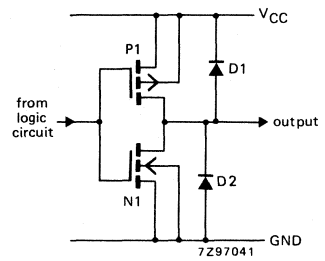


Fig. 30 Basic CMOS output stage.

A typical push-pull output stage is shown in Fig. 30. The inherent transistor-drain diodes (D1 and D2) limit the outputs of all HCMOS devices to externally-forced voltages of $-0.5 \leqslant V_O \leqslant V_{CC} + 0.5$ V. For voltages outside of this range, the diodes and parasitic bipolar elements start to conduct. Although the maximum ratings state that the diode currents have to be limited to 20 mA d.c., line ringing and power supply spiking in normal high-speed systems cause unavoidable current-peaks that exceed the ratings. With this in mind, carefull chip-layout and adequate aluminium traces ensure that the current peaks will not damage the diodes or degrade the internal circuitry.

The maximum rated d.c. current for a standard output is 25 mA and that for a bus-driver output is 35 mA. These limits are dictated by the current capability of on-chip metal traces but it is expected that output currents during switching transients will, at times, exceed the maximum ratings.

The output short-circuit currents of HCMOS will typically exceed the maximum d.c. current ratings but, for logic testing, outputs may be shorted for up to one second without damaging the device.

Three-state outputs

In the typical three-state output circuit shown in Fig. 31, when EO is HIGH the output is enabled and transistors P4 and N4 act as a transmission gate connecting the gates of the output transistors together. A LOW at EO puts the output in the high impedance OFF-state and transistors P3 and N3 act as pull-up and pull-down transistors respectively. The logic symbol for a three-state output is shown together with its function table in Fig. 32.

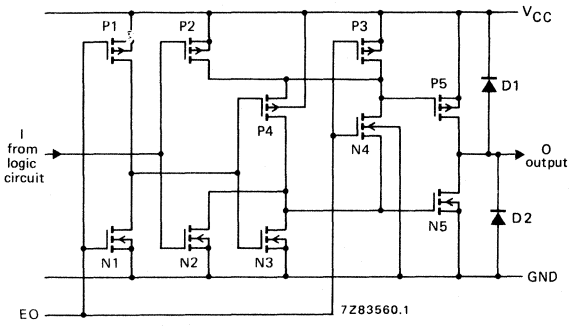
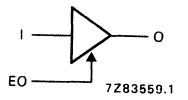


Fig. 31 Typical three-state output circuit.



inputs I	inputs EO	outputs O
X	L	Z
L	H	L
H	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

(a) logic symbol (b) function table

Fig. 32 Three-state output logic symbol and functions.

Three-state outputs are designed to be tied together but are not intended to be active simultaneously. Therefore, to minimize noise and to protect outputs from excessive power dissipation, only one three-state output should be active at any time. Generally this requires that the output enable signals be non-overlapping. When decoders are used to enable three-state outputs, the decoder should be disabled while the address is being changed. This is to avoid overlapping output-enable signals caused by decoding spikes to which all decoder outputs are prone during address-changing.

The diodes D1 and D2 are inherent diodes associated with output transistors P5 and N5 respectively. Diode D1 clamps the output at one diode-drop above V_{CC} making this an important consideration in large systems where sections of the system may be powered-down (V_{CC} = 0 V). In this situation, the output diode current has to be limited to the maximum rating.

I/O ports or transceivers are also equipped with three-state outputs as shown in Fig. 31. The I/O pin is defined as an input when the output is disabled but this pin should be regarded as a real input and not be allowed to float. If left floating, the input to an I/O port can cause V_{CC} current as described in 'Unused inputs'.

Open drain outputs

In TTL families, several functions are offered with open collector outputs to enhance logic functions by using OR-tied logic. The advantage of OR-tied logic is in the saving of logic elements and hence power consumption but this is countered by power loss and reliance on RC time propagation delays. These disadvantages are not met in CMOS and similar applications can be made using devices with 3-state outputs, or simply with the power-saving logic devices. However, a few HCMOS devices do have open drain output circuits as shown in Fig. 33. Here it can be seen that the inherent diode D1 is not present (due to non-implentation of PMOS); this allows the output voltage to be pulled above V_{CC} to V_{Omax} making both HIGH-to-LOW and LOW-to-HIGH level-shifting possible. For digital operation, a pull-up resistor is necessary to establish a logic HIGH level.

The open drain output includes protection against electrostatic discharge.

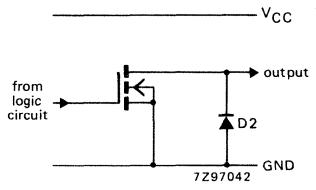


Fig. 33 Open drain output circuit.

Increased drive capability of gates

To increase output drive, inputs and outputs of gates on the same package may be used in parallel. It is advisable to restrict parallel connection to gates within one package to avoid large transient supply currents due to differing gate-switching times.

NOISE IMMUNITY

The LOW level noise immunity is the margin of noise that can be accommodated above the LOW logic level without the device switching LOW and is the voltage difference between V_{ILmax} of the driven device and V_{OLmax} of the driver. Similarly, the HIGH level noise immunity is the difference between V_{OHmin} of the driver and V_{OHmin} of the driven device. For HCMOS HC types, the LOW level noise immunity is 18% of V_{CC} and the HIGH level is 28% V_{CC}. This is a considerable improvement over LSTTL where the LOW level noise immunity is only 8% of V_{CC} and the HIGH level is just 14% V_{CC}. The margins are even greater for HCMOS at higher supply voltages as shown in Fig. 34. As HCMOS HCT types have the same switching levels as LSTTL, their noise immunities are also the same.

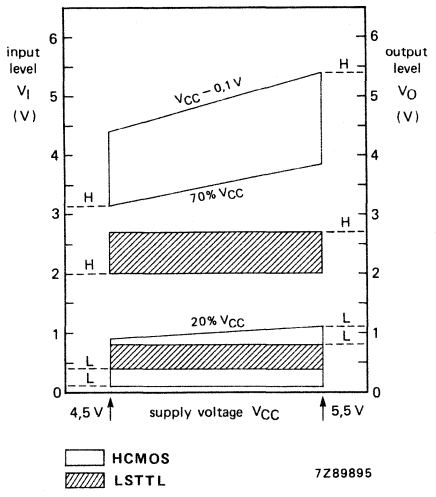


Fig. 34 Worst-case input and output voltages over operating supply range of 4.5 to 5.5 V.

The superior noise immunity of the HC input can be clearly seen from the voltage levels of the input-to-output transfer characteristics shown in Figs 35 and 36. The input-to-output transfer characteristics for the various TTL families are shown in Fig.36 to the same scale as those for HCMOS HC and HCT types in Fig. 35. The improved noise immunity of the HC types is a distinct advantage, especially in industrial applications (more information is given in 'Application notes'.

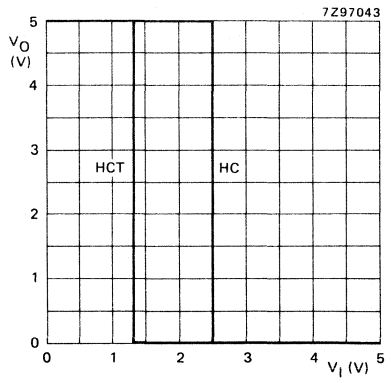


Fig. 35 Typical input-to-output transfer characteristic for HCMOS HC and HCT devices.

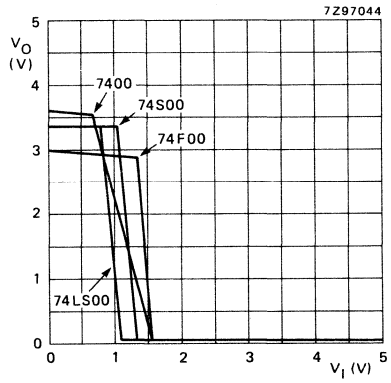


Fig. 36 Input-to-output transfer characteristics for TTL devices.

DEFINITION OF BUFFERED DEVICES

Buffered devices

Often the terms 'buffer devices', 'buffered inputs' or 'buffered outputs' are used without qualification and originate from the very first unbuffered CMOS logic family consisting of one-stage logic elements, usually gates. In these devices, both input switch levels and output impedances were not constant and hence neither were output rise/fall times nor propagation delay times. Now the Jedec JC40,2 committee have defined a buffered device to be at least two active stages with the output independent of the input logic voltage level and independent of the number of inputs being HIGH or LOW.

An example of a true buffering device with the minimum requirement of two stages is shown in the AND-function circuit of Fig. 37. The gain between input and output is high enough to consider the output impedance to be independent of the logic level at the input, and the output impedance is not affected by the state of the logic inputs.

DEFINITION OF BUFFERED DEVICES (continued)

Buffered devices (continued)

All HC and HCT devices comprise a minimum of two stages to minimize any pattern sensitivity of propagation delay time. Their buffering also improves static noise immunity due to increased voltage gain giving almost ideal transfer characteristics.

The designation HCU is used to denote single-stage devices. Basically these devices perform to the same specification as HC devices but their input and output voltage parameters are relaxed. HCU devices do not have the high gain seen in the HC/HCT versions, which makes them suitable for use in RC or crystal oscillators and other feedback circuits operating in the linear mode.

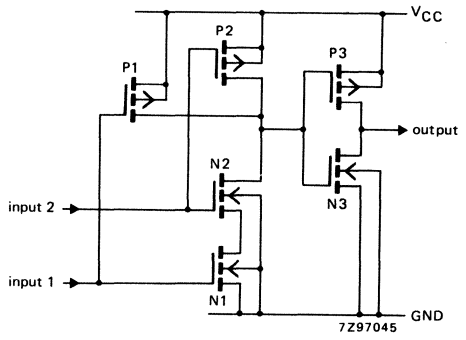


Fig. 37 The minimum number of stages for a buffered device is two. This 2-stage example is an AND function.

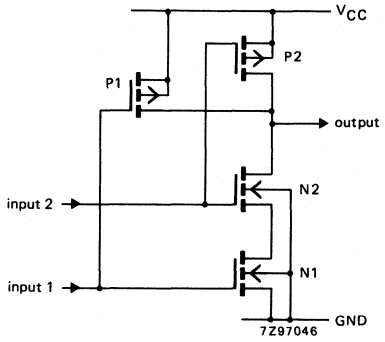


Fig. 38 Unbuffered NAND gate.

Input buffering

An input is regarded as being buffered when its switch level is not affected by the logic states of other inputs. In the example of Fig. 37 that has unbuffered inputs, the actual switch level of Input 1 varies with a HIGH level at Input 2, and vice versa. This is because the series impedance of transistors N1 and N2 determines the switching level of the device. The result can be seen in Fig. 39 where curve 1 + 2 occurs when the two inputs are tied together, and curve 1 or 2 is the switch level when the accompanying input is at V_{CC}.

To give true input buffering, an input must have an inverter stage with sufficient gain to ensure that input logic levels give independent on-chip levels. Some gates in the HC series do have unbuffered inputs, these are usually AND or OR gates but all meet the family logic level requirements. All inputs in the HCT series are buffered.

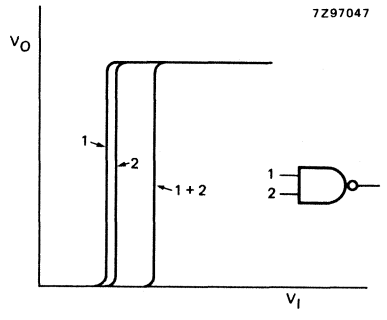


Fig. 39 Example of differing switching levels in unbuffered inputs.

Output buffering

In order to demonstrate the benefits of output buffering it is best to consider what would happen without it. In the single-stage device shown in Fig. 38, the output impedance is directly affected by the d.c. level of the input voltage. Consequently the noise margins at the output become a function of the input voltage, even when V_I is a legal HIGH or LOW.

The steady-state impedance of the circuit of Fig. 38 is also affected by the state of the inputs. Given that both P1 and P2 have identical performances (same physical size), there are then two values of impedance for output HIGH; one when either input is LOW and P1 or P2 conducts, and another when both inputs are LOW and both P1 and P2 conduct. It follows that without output buffering, the state of output conduction depends on the number of inputs being at HIGH or LOW.

All outputs of HC and HCT devices are buffered and the problems described are not encountered.

LATCH-UP PREVENTION

Conventional CMOS circuits are inherently latch-up prone. Latch-up is a thyristor action occurring in four-layer n-p-n-p structures having parasitic pnp and npn transistors. It is usually destructive.

Biasing conditions

When no forward junction is forward-biased, minority-carrier injection does not take place and no parasitic transistors are activated. In practice, forward biasing leading to latch-up is due to input or output voltages exceeding V_{CC} in a positive direction, or GND in a negative direction. Although these voltages are clamped by junctions at the terminals, over-voltage spikes on the supply lines can result in forward biasing through avalanch break-down. Fast switching and supply line spikes can enter through junction capacitance to cause forward biasing at circuit nodes.

Parasitic structures

A CMOS structure in which latch-up can occur is shown in Fig. 40(a); the equivalent circuit formed by parasitic n-channel MOS transistors with adjoining n^+ and p^+ regions is shown in Fig. 40(b). The resistors represent resistance to lateral current flow and their values depend on circuit geometry and doping.

Application of a negative voltage to the output results in a current (I) which, in turn, gives rise to a current $I.h_{FB}$ in the collector of TR2. When the voltage across r_c produced by this current is large enough it causes TR3 to conduct. Since the h_{FE} of TR2 is fairly high, virtually all the collector current of TR3 flows through $r_{bb'1}$ and $r_{bb'2}$. Sufficient voltage dropped across $r_{bb'1}$ turns TR1 on and its collector current further increases the base-drive of TR3, current I due to the negative voltage on the output is no longer necessary: the current through TR1TR3 being, in principle, limited only by the source resistance of the power supply.

Latch-up can also be initiated via the supply line. Fig. 41(a) shows the same circuit structure as Fig. 40(a) but now TR2 is lateral, formed by the source and drain junction of the associated n-channel MOS transistor which is part of a complementary inverter stage. Its p-channel complement (not shown) connects the n-channel drain and consequently, the collector of TR2 to V_{CC}. The equivalent circuit of this arrangement, complete with the actual inverter stage, is shown in Fig. 41(b).

Excessive supply voltage can break down the collector-base junction of TR2. Thyristor TR1TR2 will trigger if the resulting current-flow through $r_{bb'1}$ is sufficient to turn on TR1. Although the breakdown current through TR2 is limited by the on-state resistance of the p-channel MOS transistor, the current through TR1TR3 is limited only by power supply resistance.

It can be seen from Fig. 41(b) that a sharp positive-going transient on the supply line can also produce a trigger voltage across $r_{bb'1}$ directly as the result of current through the capacitance of the collector-base junction of TR2.

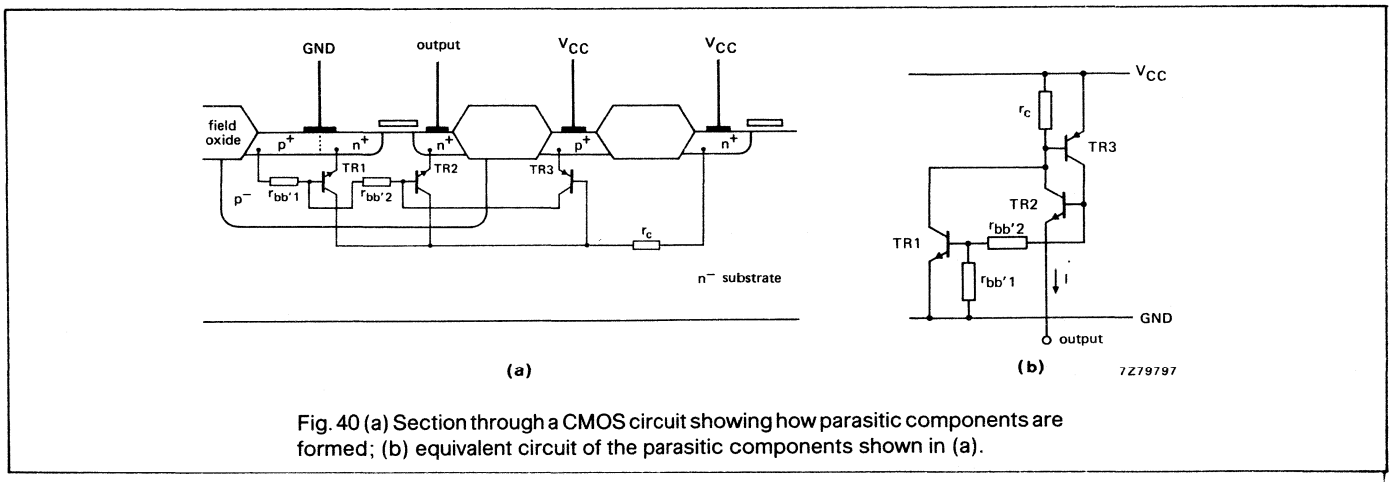


Fig. 40 (a) Section through a CMOS circuit showing how parasitic components are formed; (b) equivalent circuit of the parasitic components shown in (a).

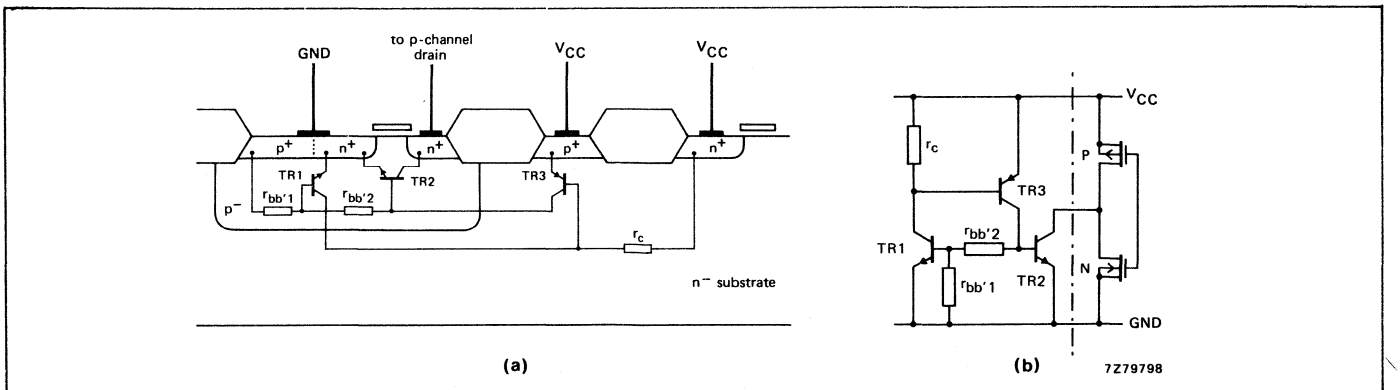


Fig. 41 (a) In the structure of Fig. 40(a), TR2 is now formed laterally; (b) equivalent circuit incorporating lateral transistor TR2.

LATCH-UP PREVENTION (continued)

Precautions

It can be seen from Figs 40 and 41 that both the values of $r_{bb'1}$ and r_c and the topologies of the p^+ and n^+ diffusions to the n- substrate are important factors in susceptibility to thyristor latch- up. Considerable improvement has been made through careful design of the source-to-pocket contacts of the n-channel MOS transistors and the interchange of the p^+ and n^+ diffusions to the substrate, as shown in Fig. 42. The value of r_c can be reduced by arranging the n^+ diffusion as a guard ring around the n-channel device but this solution considerably increases the area of the device. The best way of coping with the problem is to avoid lateral current flow in the n- substrate. This can be achieved by growing an epitaxial layer on a very low resistivity substrate as shown in Fig. 43.

Latch-up-free HCMOS

The properties of our HCMOS process enable both geometric precautions and epitaxial layer to be used. All types from the PC54/74 family have been tested for susceptibility to latch-up. The devices were tested across the full temperature range with currents up to 100 mA d.c. and up to 500 mA pulsed at 100 ns with d = 1%. In these tests no device suffered latch-up. Since beyond the tested values excessive heating occurs or aluminium tracks or bond wires break down, we conclude that our HCMOS devices are latch-up free.

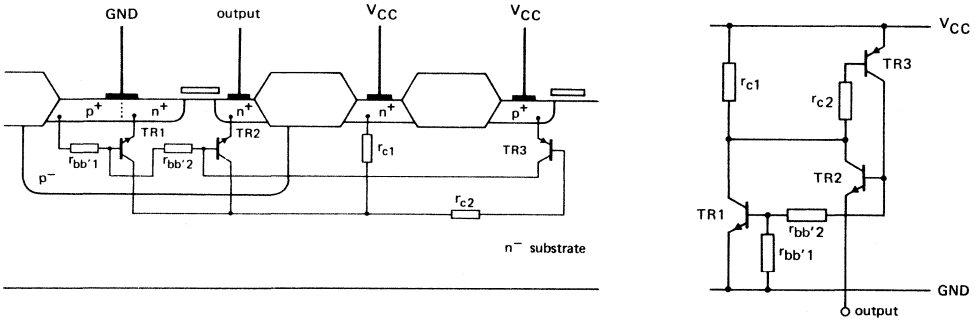


Fig. 42 (a) Rearrangement of the structure shown in Fig. 41(a) greatly reduces susceptibility to latch-up by incorporating base resistance r_{c2}, as shown in equivalent circuit (b).

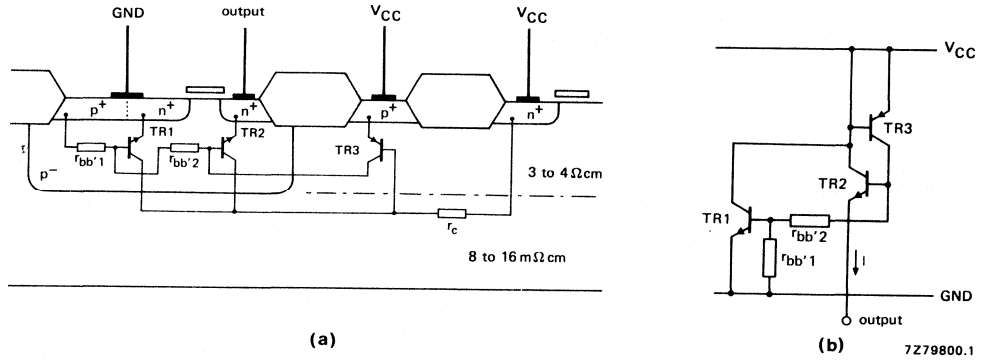


Fig. 43 (a) By growing an epitaxial layer on a very-low resistivity substrate the lateral current flow responsible for latch-up is mostly eliminated; (b) the resulting equivalent circuit.

Measuring latch-up sensitivity

Caution

- The test methods that follow can be destructive.
- They are not intended for use with automatic test equipment.
- Apply currents for at least 2 ms.
- Limit power supply currents to 200 mA.

Input/output-triggered latch-up test

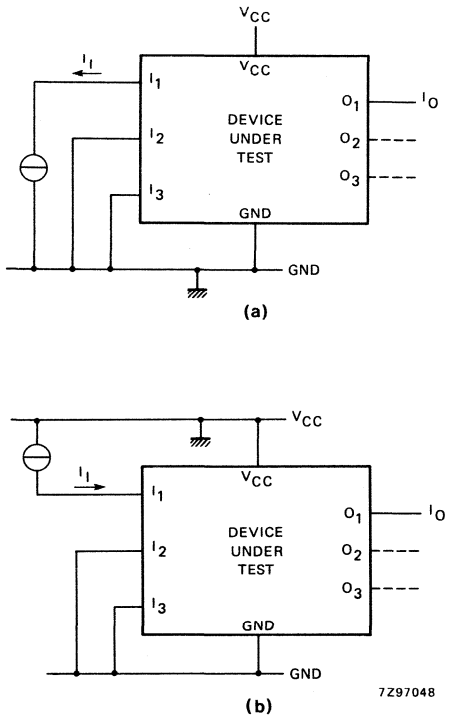


Fig. 44 Test set-up for input/output-triggered latch-up test (two configurations are necessary to avoid negative power supply current flow); (a) circuit for negative current flow ($-I_I$); (b) circuit for positive current flow ($+I_I$).

1) With reference to Fig. 44, apply $+I_I$. Raise V_{CC}-to-GND maximum rating and reduce I_I to zero. The device should not latch- up, i.e. $I_{CC} \leq I_{CC(quiescent)}$.
2) Repeat item 1) but with $-I_I$.
3) Apply inputs to cause a HIGH at the output under test (for three-state outputs, put device into high-impedance state). Apply $+I_O$. Raise V_{CC}-to-GND to maximum rating and reduce I_O to zero. The device should not latch-up, i.e. $I_{CC} \leq I_{CC(quiescent)}$.
4) Repeat item 3) but with $-I_O$ and with test outputs LOW.

V_{CC}-triggered latch-up test

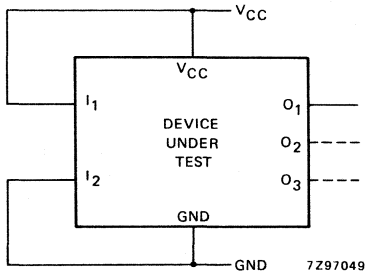


Fig. 45 Test set-up for V_{CC}-triggered latch-up test.

1) With reference to Fig. 45, cause the inputs to alternate between V_{CC} and GND.
2) Source current I into V_{CC}. The sustained voltage ($V_{sustained}$, Fig. 46) should not go below V_{CC} maximum rating.

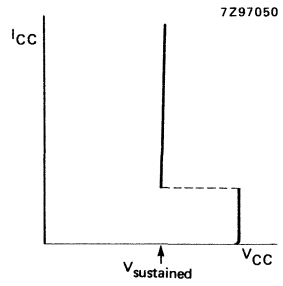


Fig. 46 Supply current characteristic for V_{CC}-triggered latch-up test.

DROP-IN REPLACEMENT

The HCMOS HCT range makes it unnecessary to sacrifice noise margins, speed and quiescent power dissipation in constructing interfaces to achieve mixed-technology designs. This is because HCT devices are TTL compatible and can directly replace LSTTL counterparts without the addition of pull-up resistors at the LSTTL outputs.

Fan-out capabilities should be taken into account when an HCT device is used to replace a TTL part. TTL fan-out is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fan-out is determined by the ability of the outputs to sink current (a TTL input usually sources current). The outputs of HCMOS are classified in two categories: standard and bus- driver. Table 4 shows the fan-out referred to the different TTL families.

Table 4 Fan-out of HCMOS to TTL elements

HCMOS HCT	TTL	LS	ALS	FAST	S & AS
standard	2	10	20	6	2
bus-driver	3	15	30	10	3

The fan-out values shown in Table 4 are derived at a voltage drop of max. 0.4 V (V_{OL}). In the "74" TTL series an extended V_{OL} figure is often seen, e.g. 8 mA at 0.5 V voltage drop for LSTTL. If this figure is used in determining the fan-out of the TTL part it can result in a higher fan-out than is possible with HCMOS. This can be resolved by replacing as many of the driven TTL parts as possible by HCT devices to reduce the sink current requirement (the HCT input current is neglegible). Also a vast reduction in power dissipation is made by using HCMOS.

Devices of the HCT family are power-saving, drop-in replacements for LSTTL parts. The total power consumed by a system depends largely on the number of gates switching at any time and on the switching frequency, but in most systems only about 30% of all circuits switch at the maximum system frequency whilst 70% operate at far lower rates. So, even in systems using ALS, AS, S, and FAST, the HCT family can be used with consequent power-savings in mixed technology designs.

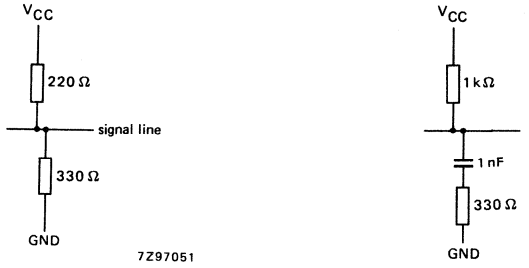
BUS SYSTEMS

Bus systems are commonly used in microprocessor applications. CMOS is entering this area rapidly following the introduction of several versions of the popular NMOS processors.

There are several constraints imposed on microprocessor systems in industrial applications, such as electrically- noisy environments, battery-standby requirements and sealed, gas-tight enclosures. HCMOS bus systems, e.g. the CMOS STD bus (a non-proprietary CMOS bus standard) provides a solution to all these problems. It offers superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

In order to optimize results with HCMOS, the use of only HC devices in circuits which communicate directly with the bus is recommended. By doing this, a new bus termination can be introduced (see Fig. 47(b)) which, unlike the conventional TTL bus termination, draws no heavy d.c. current and is more suited to HCMOS outputs.

The wider supply voltage range of HCMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via the user edge connector. Such pick-up can exceed the CMOS maximum ratings if not limited by a 10 kΩ series resistor in the HCMOS logic line. This will limit current to ±20 mA for external voltages of up to ±200 V, however, for correct functioning, the d.c. input current should be kept below 2 mA. The recommended user edge input protection is shown in Fig. 48.



(a) Conventional termination for TTL buses

(b) Proposed termination for CMOS STD bus equivalents

Fig. 47 Bus terminations.

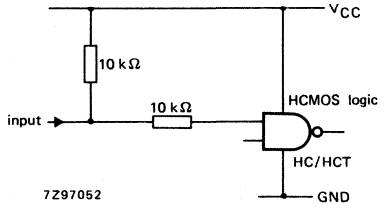


Fig. 48 Example of the user edge input circuit.

In the circuit of Fig. 48, if the input diode current exceeds 2 mA a HIGH-to-LOW level shifter should be used (e.g. HC4049 or HC4050).

Since HCMOS bus-drivers do not have built-in hysteresis, slowly rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the flip-flop series HC/HCT73, 74, 107, 109, 112, or the dedicated Schmitt triggers HC/HCT14 and 132. The rise and fall times can be derived from the information given in 'Propagation delays and transition times'.

PACKAGE OUTLINES

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ICs to package outlines 85

Outline drawings 95

CROSS-REFERENCE LIST: ICs TO PACKAGE OUTLINES

type number	description	package code
PC74HC/HCT00P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT00D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT00T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT02P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT02D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT02T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT03P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT03D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT03T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT04P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT04D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT04T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HCU04P	14-lead DIL; plastic	SOT-27
PC54/74HCU04D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HCU04T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT08P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT08D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT08T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT10P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT10D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT10T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT11P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT11D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT11T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT14P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT14D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT14T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT20P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT20D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT20T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT21P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT21D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT21T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT27P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT27D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT27T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT30P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT30D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT30T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT32P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT32D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT32T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT42P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT42D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT42T	16-lead mini-pack; plastic	SO-16;SOT-109A

CROSS-REFERENCE LIST: ICs TO PACKAGE OUTLINES (continued)

type number	description	package code
PC74HC/HCT73P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT73D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT73T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT74P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT74D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT74T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT75P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT75D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT75T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT85P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT85D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT85T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT86P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT86D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT86T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT93P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT93D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT93T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT107P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT107D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT107T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT109P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT109D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT109T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT112P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT112D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT112T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT123P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT123D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT123T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT125P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT125D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT125T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT126P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT126D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT126T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT132P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT132D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT132T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT137P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT137D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT137T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT138P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT138D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT138T	16-lead mini-pack; plastic	SO-16;SOT-109A

type number	description	package code
PC74HC/HCT139P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT139D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT139T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT147P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT147D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT147T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT151P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT151D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT151T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT153P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT153D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT153T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT154P	24-lead DIL; plastic	SOT-101A
PC54/74HC/HCT154D	24-lead DIL; ceramic (cerdip)	SOT-94
PC74HC/HCT154T	24-lead mini-pack; plastic	SO-24;SOT-137A
PC74HC/HCT157P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT157D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT157T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT158P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT158D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT158T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT160P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT160D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT160T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT161P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT161D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT161T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT162P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT162D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT162T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT163P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT163D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT163T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT164P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT164D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT164T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT165P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT165D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT165T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT166P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT166D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT166T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT173P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT173D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT173T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT174P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT174D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT174T	16-lead mini-pack; plastic	SO-16;SOT-109A

CROSS-REFERENCE LIST: ICs TO PACKAGE OUTLINES (continued)

type number	description	package code
PC74HC/HCT175P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT175D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT175T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT181P	24-lead DIL; plastic	SOT-101A
PC54/74HC/HCT181D	24-lead DIL; ceramic (cerdip)	SOT-94
PC74HC/HCT181T	24-lead mini-pack; plastic	SO-24;SOT-137A
PC74HC/HCT182P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT182D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT182T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT190P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT190D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT190T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT191P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT191D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT191T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT192P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT192D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT192T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT193P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT193D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT193T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT194P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT194D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT194T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT195P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT195D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT195T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT221P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT221D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT221T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT237P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT237D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT237T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT238P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT238D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT238T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT240P	20-lead DIL; plastic	SOT-146
PC74HC/HCT240T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT241P	20-lead DIL; plastic	SOT-146
PC74HC/HCT241T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT242P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT242D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT242T	14-lead mini-pack; plastic	SO-14;SOT-108A

type number	description	package code
PC74HC/HCT243P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT243D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT243T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT244P	20-lead DIL; plastic	SOT-146
PC74HC/HCT244T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT245P	20-lead DIL; plastic	SOT-146
PC74HC/HCT245T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT251P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT251D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT251T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT253P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT253D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT253T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT257P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT257D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT257T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT258P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT258D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT258T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT259P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT259D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT259T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC7266P	14-lead DIL; plastic	SOT-27
PC54/74HC7266D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC7266T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT273P	20-lead DIL; plastic	SOT-146
PC74HC/HCT273T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT280P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT280D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT280T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT283P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT283D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT283T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT297P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT297D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT297T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT299P	20-lead DIL; plastic	SOT-146
PC74HC/HCT299T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT354P	20-lead DIL; plastic	SOT-146
PC74HC/HCT354T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT356P	20-lead DIL; plastic	SOT-146
PC74HC/HCT356T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT365P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT365D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT365T	16-lead mini-pack; plastic	SO-16;SOT-109A

CROSS-REFERENCE LIST: ICs TO PACKAGE OUTLINES (continued)

type number	description	package code
PC74HC/HCT366P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT366D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT366T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT367P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT367D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT367T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT368P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT368D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT368T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT373P	20-lead DIL; plastic	SOT-146
PC74HC/HCT373T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT374P	20-lead DIL; plastic	SOT-146
PC74HC/HCT374T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT377P	20-lead DIL; plastic	SOT-146
PC74HC/HCT377T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT390P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT390D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT390T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT393P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT393D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT393T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT423P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT423D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT423T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT533P	20-lead DIL; plastic	SOT-146
PC74HC/HCT533T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT534P	20-lead DIL; plastic	SOT-146
PC74HC/HCT534T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT540P	20-lead DIL; plastic	SOT-146
PC74HC/HCT540T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT541P	20-lead DIL; plastic	SOT-146
PC74HC/HCT541T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT563P	20-lead DIL; plastic	SOT-146
PC74HC/HCT563T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT564P	20-lead DIL; plastic	SOT-146
PC74HC/HCT564T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT573P	20-lead DIL; plastic	SOT-146
PC74HC/HCT573T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT574P	20-lead DIL; plastic	SOT-146
PC74HC/HCT574T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT583P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT583D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT583T	16-lead mini-pack; plastic	SO-16;SOT-109A

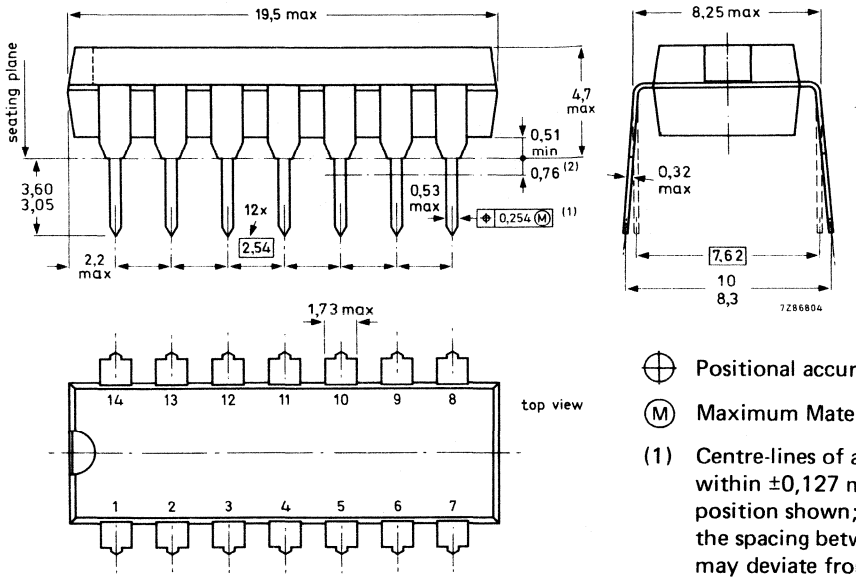
type number	description	package code
PC74HC/HCT597P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT597D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT597T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT640P	20-lead DIL; plastic	SOT-146
PC74HC/HCT640T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT643P	20-lead DIL; plastic	SOT-146
PC74HC/HCT643T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT646P	24-lead DIL; plastic	SOT-101A
PC54/74HC/HCT646D	24-lead DIL; ceramic (cerdip)	SOT-94
PC74HC/HCT646T	24-lead mini-pack; plastic	SO-24;SOT-137A
PC74HC/HCT648P	24-lead DIL; plastic	SOT-101A
PC54/74HC/HCT648D	24-lead DIL; ceramic (cerdip)	SOT-94
PC74HC/HCT648T	24-lead mini-pack; plastic	SO-24;SOT-137A
PC74HC/HCT670P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT670D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT670T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT688P	20-lead DIL; plastic	SOT-146
PC74HC/HCT688T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT4002P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT4002D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT4002T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT4015P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4015D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4015T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4016P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT4016D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT4016T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT4017P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4017D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4017T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4020P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4020D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4020T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4024P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT4024D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT4024T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT4040P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4040D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4040T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4046P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4046D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4046T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4046-1P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4046-1D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4046-1T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC4049P	16-lead DIL; plastic	SOT-38Z
PC54/74HC4049D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC4049T	16-lead mini-pack; plastic	SO-16;SOT-109A

CROSS-REFERENCE LIST: ICs TO PACKAGE OUTLINES (continued)

type number	description	package code
PC74HC4050P	16-lead DIL; plastic	SOT-38Z
PC54/74HC4050D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC4050T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4051P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4051D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4051T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4052P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4052D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4052T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4053P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4053D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4053T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4059P	24-lead DIL; plastic	SOT-101A
PC54/74HC/HCT4059D	24-lead DIL; ceramic (cerdip)	SOT-94
PC74HC/HCT4059T	24-lead mini-pack; plastic	SO-24;SOT-137A
PC74HC/HCT4060P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4060D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4060T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4066P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT4066D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT4066T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT4067P	24-lead DIL; plastic	SOT-101A
PC54/74HC/HCT4067D	24-lead DIL; ceramic (cerdip)	SOT-94
PC74HC/HCT4067T	24-lead mini-pack; plastic	SO-24;SOT-137A
PC74HC/HCT4075P	14-lead DIL; plastic	SOT-27
PC54/74HC/HCT4075D	14-lead DIL; ceramic (cerdip)	SOT-73
PC74HC/HCT4075T	14-lead mini-pack; plastic	SO-14;SOT-108A
PC74HC/HCT4094P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4094D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4094T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4316P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4316D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4316T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4351P	18-lead DIL; plastic	SOT-102A
PC54/74HC/HCT4351D	18-lead DIL; ceramic (cerdip)	SOT-133
PC74HC/HCT4351T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT4352P	18-lead DIL; plastic	SOT-102A
PC54/74HC/HCT4352D	18-lead DIL; ceramic (cerdip)	SOT-133
PC74HC/HCT4352T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT4353P	18-lead DIL; plastic	SOT-102A
PC54/74HC/HCT4353D	18-lead DIL; ceramic (cerdip)	SOT-133
PC74HC/HCT4353T	20-lead mini-pack; plastic	SO-20;SOT-163A
PC74HC/HCT4510P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4510D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4510T	16-lead mini-pack; plastic	SO-16;SOT-109A

type number	description	package code
PC74HC/HCT4511P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4511D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4511T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4514P	24-lead DIL; plastic	SOT-101A
PC54/74HC/HCT4514D	24-lead DIL; ceramic (cerdip)	SOT-94
PC74HC/HCT4514T	24-lead mini-pack; plastic	SO-24;SOT-137A
PC74HC/HCT4515P	24-lead DIL; plastic	SOT-101A
PC54/74HC/HCT4515D	24-lead DIL; ceramic (cerdip)	SOT-94
PC74HC/HCT4515T	24-lead mini-pack; plastic	SO-24;SOT-137A
PC74HC/HCT4516P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4516D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4516T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4518P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4518D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4518T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4520P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4520D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4520T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4538P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4538D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4538T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT4543P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT4543D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT4543T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT40102P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT40102D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT40102T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT40103P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT40103D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT40103T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT40104P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT40104D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT40104T	16-lead mini-pack; plastic	SO-16;SOT-109A
PC74HC/HCT40105P	16-lead DIL; plastic	SOT-38Z
PC54/74HC/HCT40105D	16-lead DIL; ceramic (cerdip)	SOT-74
PC74HC/HCT40105T	16-lead mini-pack; plastic	SO-16;SOT-109A

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27)



⊕ Positional accuracy.

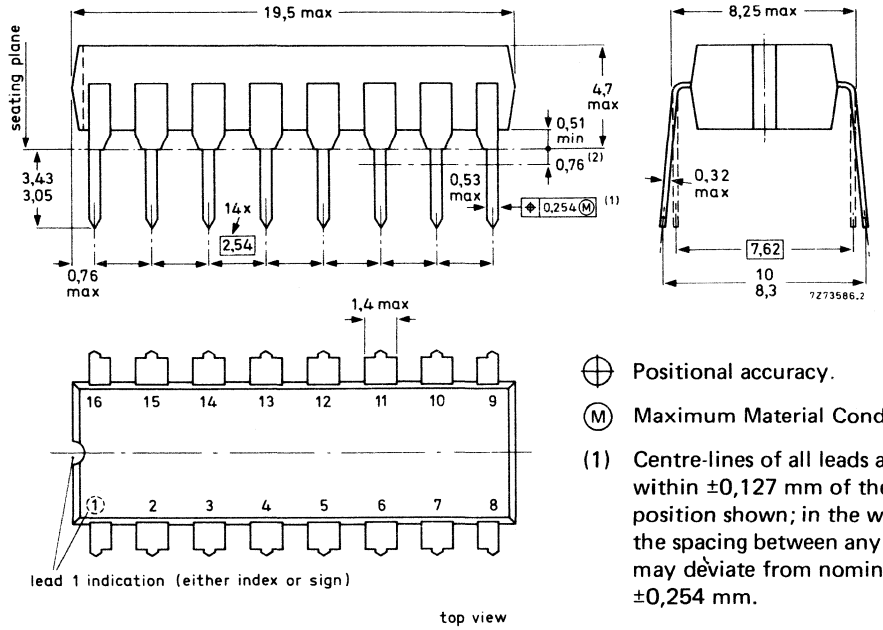
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



⊕ Positional accuracy.

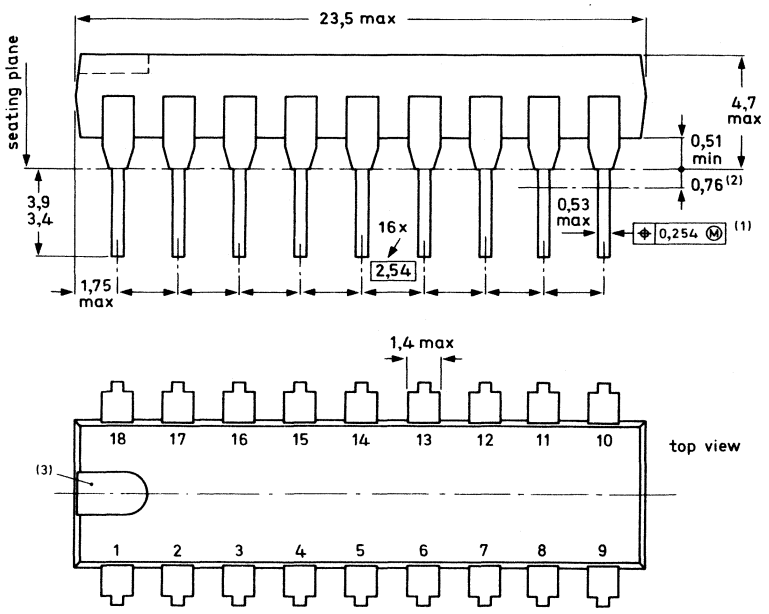
Ⓜ Maximum Material Condition.

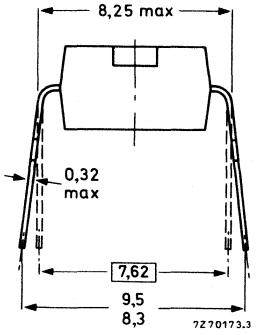
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





Dimensions in mm

⊕ Positional accuracy.

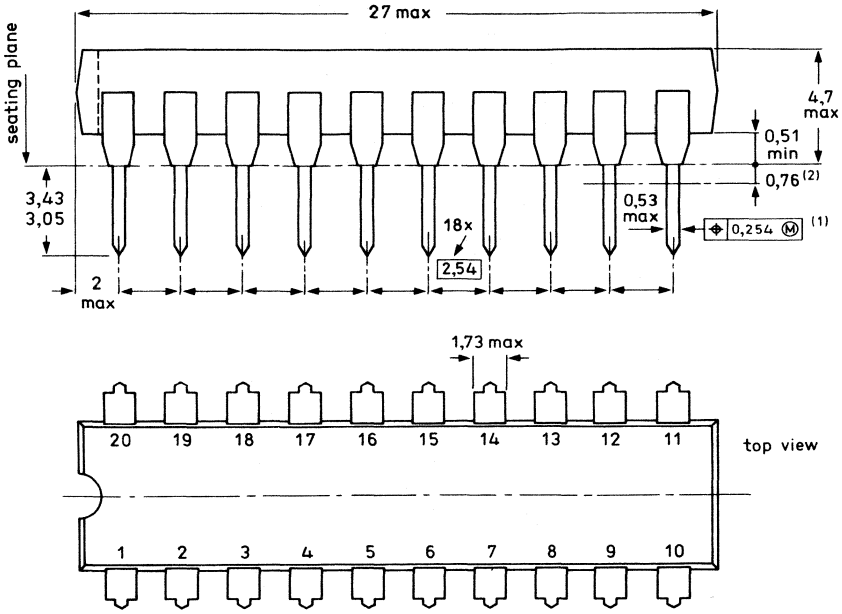
Ⓜ Maximum Material Condition.

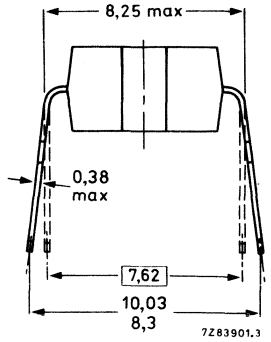
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

20-LEAD DUAL IN-LINE; PLASTIC (SOT-146)





Dimensions in mm

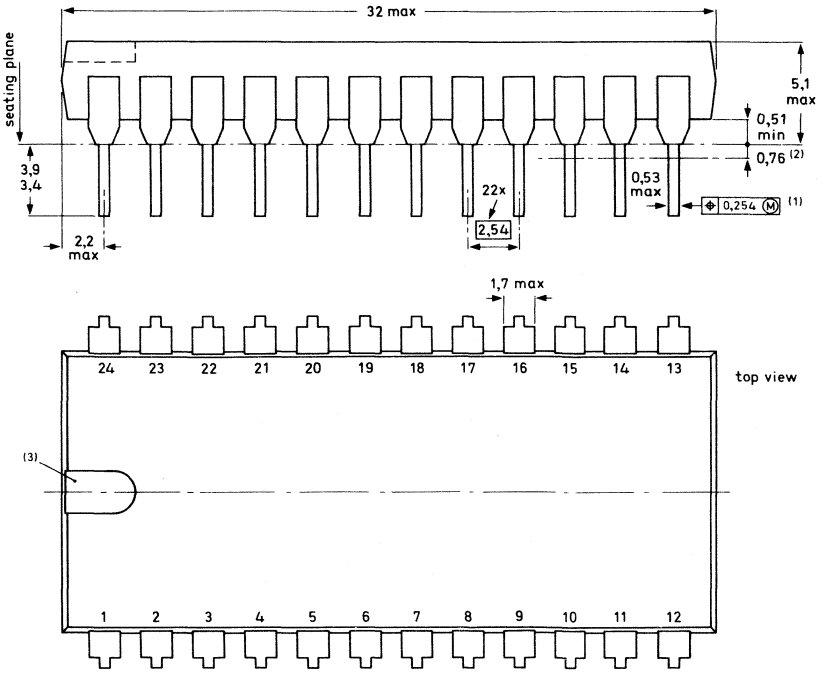
⊕ Positional accuracy.

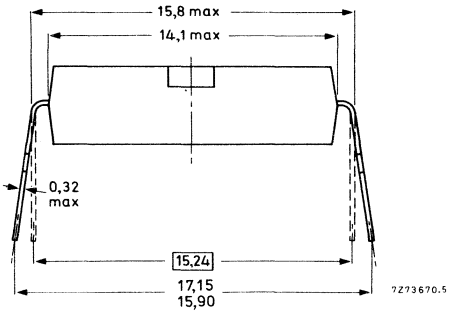
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





Dimensions in mm

⊕ Positional accuracy.

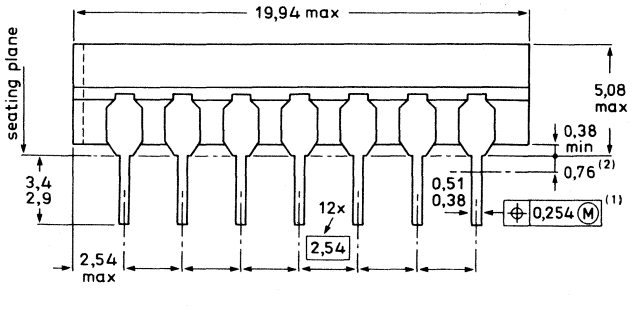
Ⓜ Maximum Material Condition.

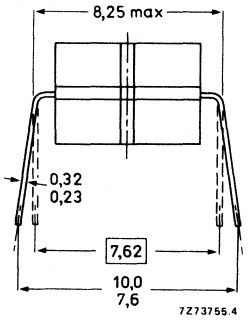
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

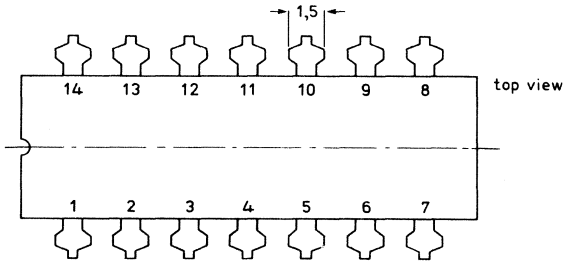
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

14-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-73)







⊕ Positional accuracy.

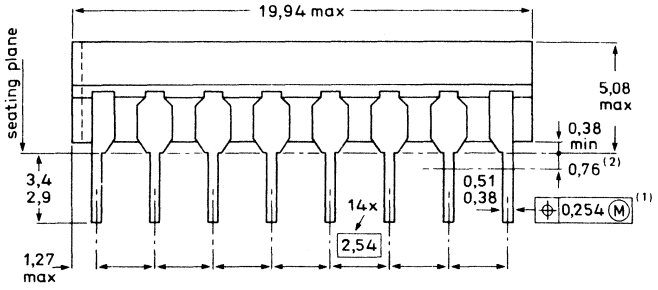
Ⓜ Maximum Material Condition.

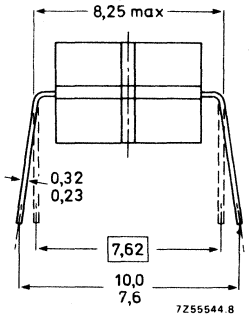
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

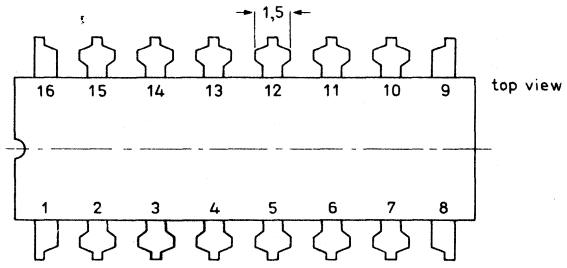
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-74)







⊕ Positional accuracy.

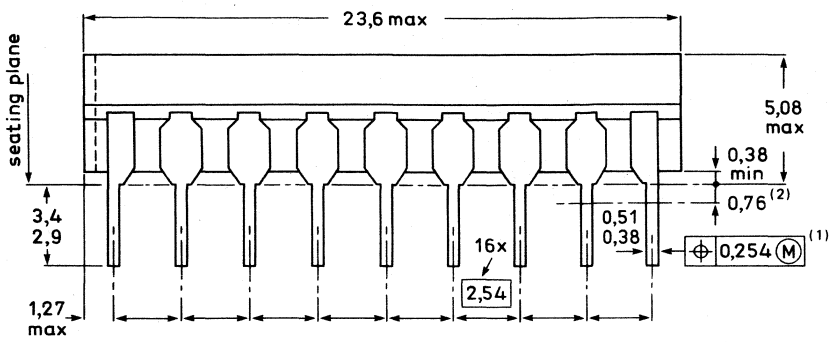
Ⓜ Maximum Material Condition.

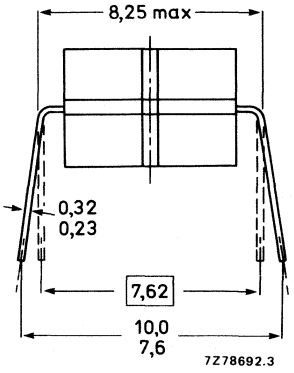
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

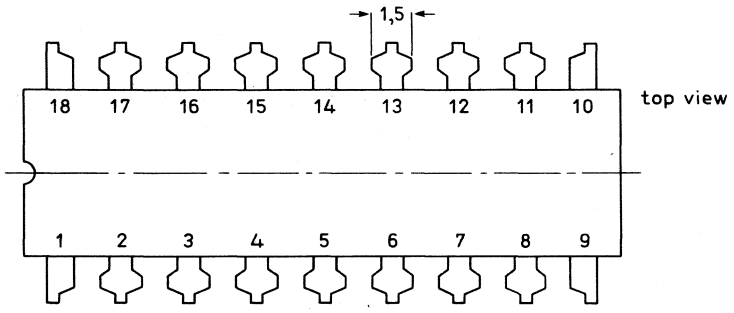
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133A,B)







⊕ Positional accuracy.

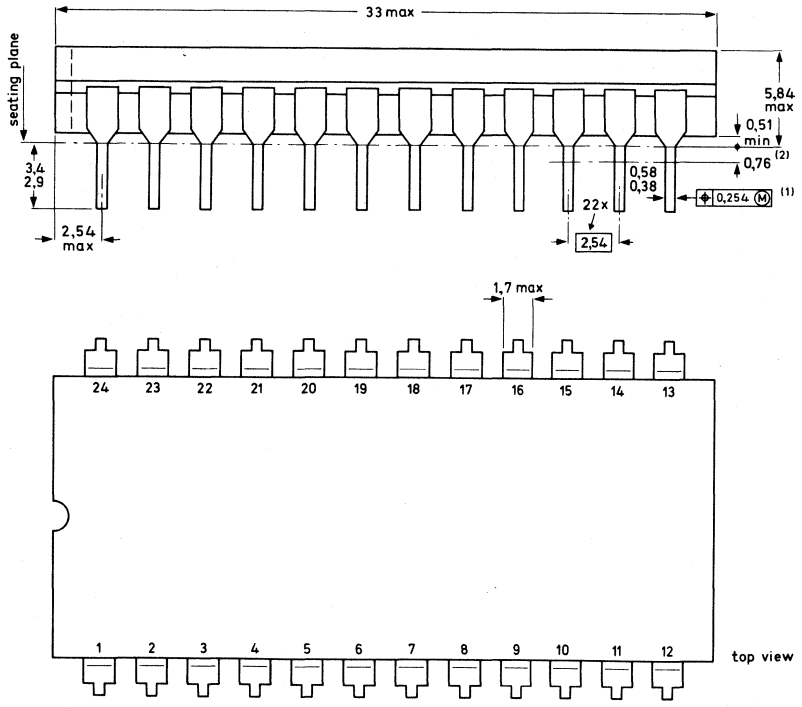
Ⓜ Maximum Material Condition.

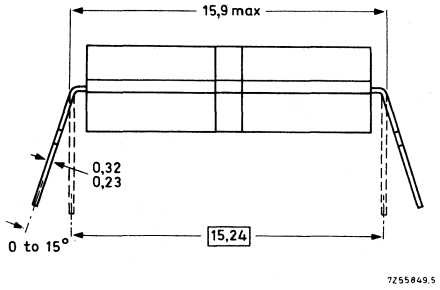
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

24-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-94)





⊕ Positional accuracy.

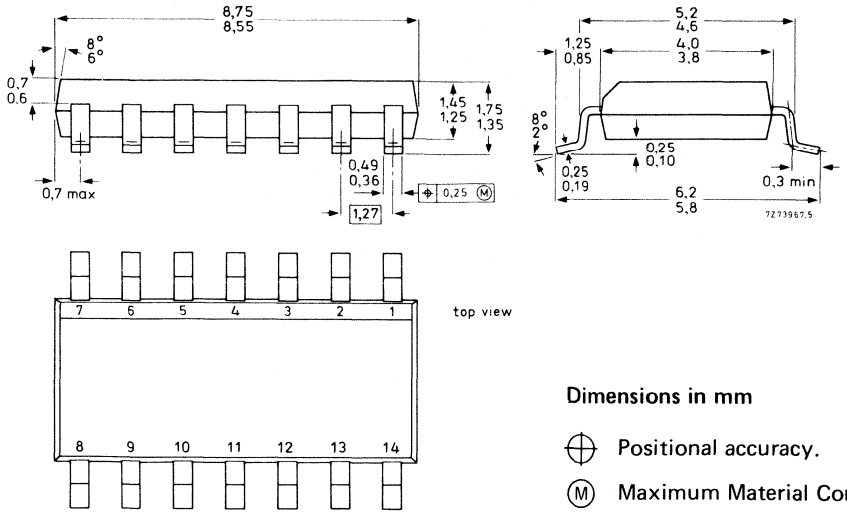
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

14-LEAD MINI-PACK; PLASTIC (SO-14; SOT-108A)

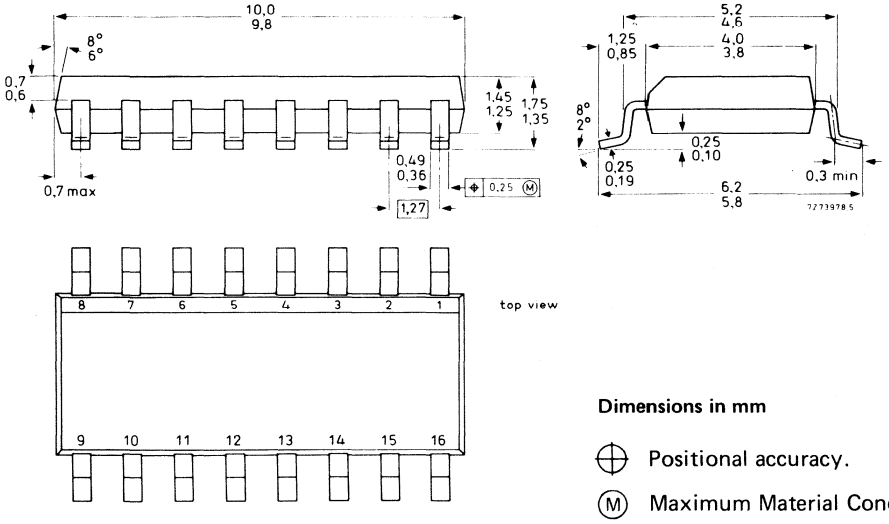


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

16-LEAD MINI-PACK; PLASTIC (SO-16; SOT-109A)

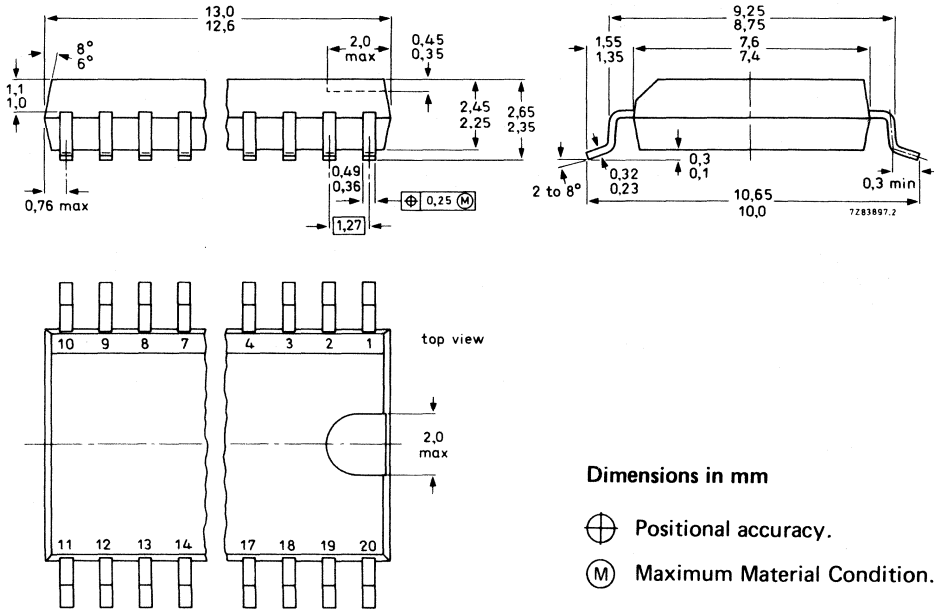


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)

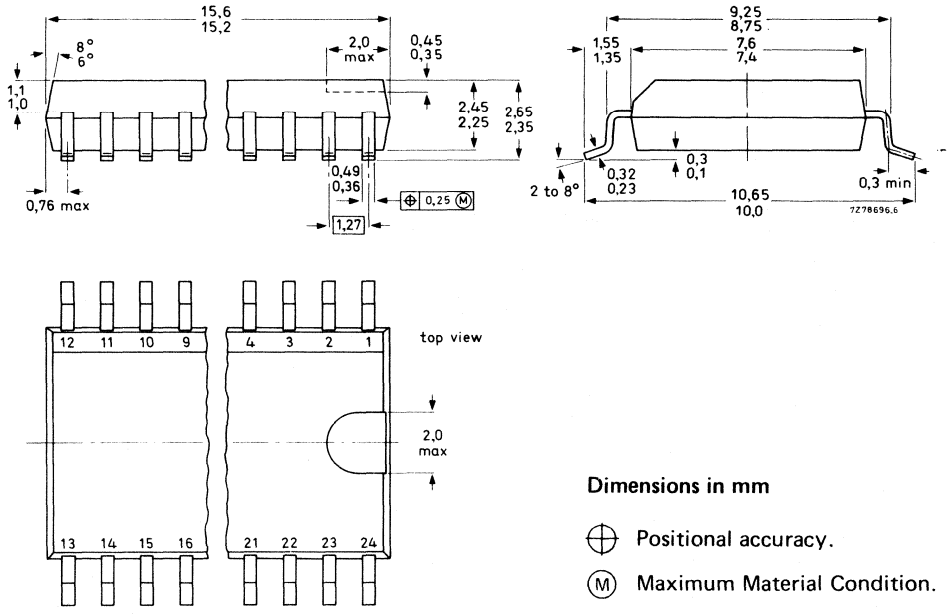


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

24-LEAD MINI-PACK; PLASTIC (SO-24; SOT-137A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

HCMOS FAMILY CHARACTERISTICS

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Data sheet specification guide 115

Definitions of symbols 117

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS PC54/74 family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The PC54 and PC74 high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 54/74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as PC54/74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as PC54/74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0,8 to 2,0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the PC54/74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.
However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "APPLICATION NOTES" section "HANDLING CMOS DEVICES").

RECOMMENDED OPERATING CONDITIONS FOR 54/74HC/HCT

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT/HCU
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT/HCU
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

RECOMMENDED OPERATING CONDITIONS FOR 54/74HC/HCT/HCU

SYMBOL	PARAMETER	54/74HC/HCU			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT/HCU
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT/HCU
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs and HCU devices		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > +0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > +0.5$ V
$\pm I_O$	DC output source or sink current — standard outputs — bus driver outputs		 25 35	 mA mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: — standard outputs — bus driver outputs		 50 70	 mA mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		 500	 mW	for standard temperature range; −40 to +85 °C; 74HC/HCT/HCU above +60 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60 °C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		 500	 mW	for extended temperature range; −55 to +125 °C; 54HC/HCT/HCU above +100 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage bus driver outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	6.0	V_{IH} or V_{IL}	$\|V_S\| = V_{CC}$ (note 1)
$\pm I_S$	analog switch ON-state leakage current			0.2		2.0		2.0	μA	6.0	V_{IH} or V_{IL}	$\|V_S\| = V_{CC}$ (note 1)
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current **SSI** **flip-flops** **MSI**			 2.0 4.0 8.0		 20.0 40.0 80.0		 40.0 80.0 160.0	 μA μA μA	 6.0 6.0 6.0	 V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$

Note

1. If applicable V_{EE} = GND.

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage all outputs	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage all outputs		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage bus driver outputs			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$\|V_S\| = V_{CC}$ (note 1)
$\pm I_S$	analog switch ON-state leakage current			0.2		2.0		2.0	μA	5.5	V_{IH} or V_{IL}	$\|V_S\| = V_{CC}$ (note 1)
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current **SSI** **flip-flops** **MSI**			 2.0 4.0 8.0		 20.0 40.0 80.0		 40.0 80.0 160.0	 μA μA μA	 6.0 6.0 6.0	 V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 2)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Notes

1. If applicable V_{EE} = GND.
2. The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2.4 V; V_{CC} = 5.5 V) specification is: ΔI_{CC} = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

DC CHARACTERISTICS FOR 54/74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCU			74HCU		54HCU			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5			1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage			0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current SSI			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 1 and 2
t_{THL}/ t_{TLH}	output transition time bus driver outputs			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 1 and 2

AC CHARACTERISTICS FOR 54/74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCU			74HCU		54HCU			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 1

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs			15		19		22	ns	4.5	Figs 1 and 2
t_{THL}/ t_{TLH}	output transition time bus driver outputs			12		15		18	ns	4.5	Figs 1 and 2

HCU TYPES

AC WAVEFORMS PC54HCU; PC74HCU

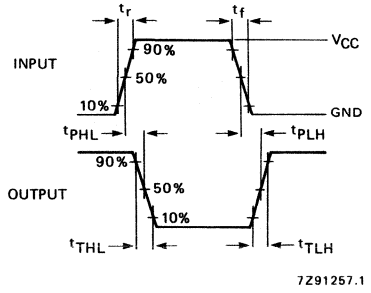


Fig. 1 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

TEST CIRCUIT FOR PC54HCU; PC74HCU

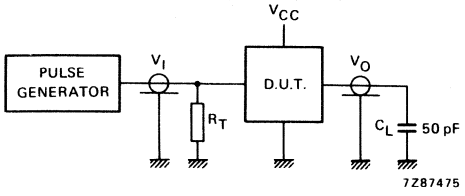


Fig. 2 Test circuit.

Definitions for Fig. 2:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HC TYPES

AC WAVEFORMS PC54HC; PC74HC

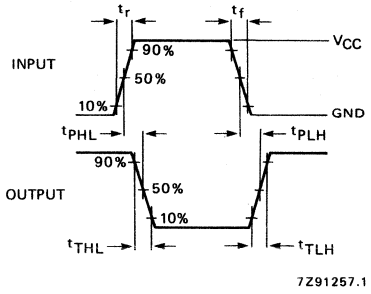


Fig. 3 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS PC54HC; PC74HC

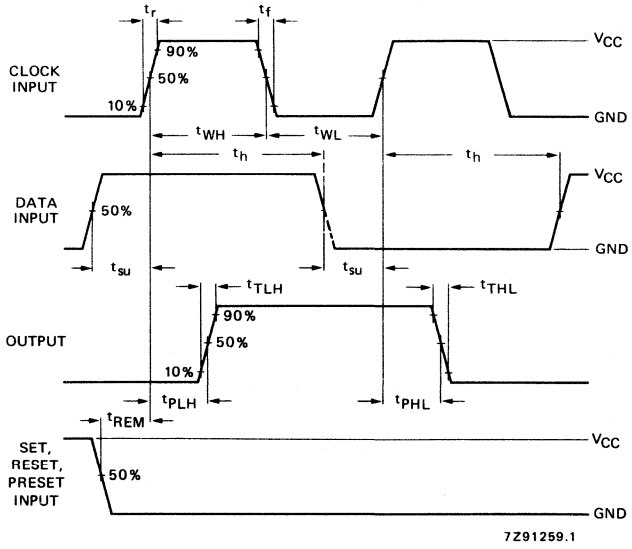


Fig. 4 Set-up times, hold times, removal times and propagation delays for sequential logic ICs.

Note to Fig. 4

In Fig. 4 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.

HC TYPES (continued)

TEST CIRCUIT FOR PC54HC; PC74HC

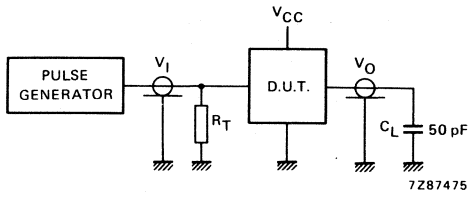


Fig. 5 Test circuit.

Definitions for Fig. 5:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

AC WAVEFORMS PC54HC; PC74HC (continued)

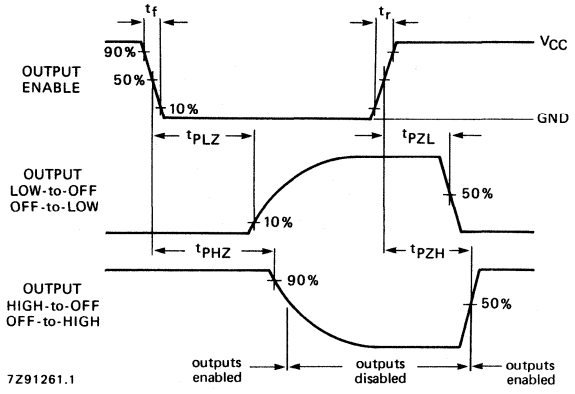
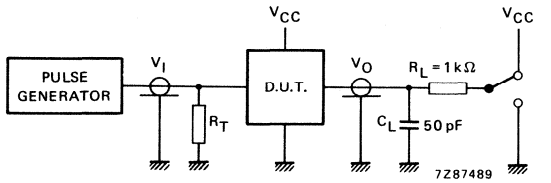


Fig. 6 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR PC54HC; PC74HC



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 7 Test circuit for 3-state outputs.

Definitions for Fig. 7:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HCT TYPES

AC WAVEFORMS PC54HCT; PC74HCT

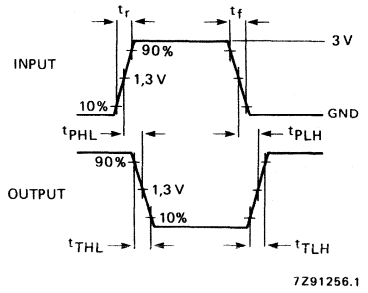


Fig. 8 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS PC54HCT; PC74HCT

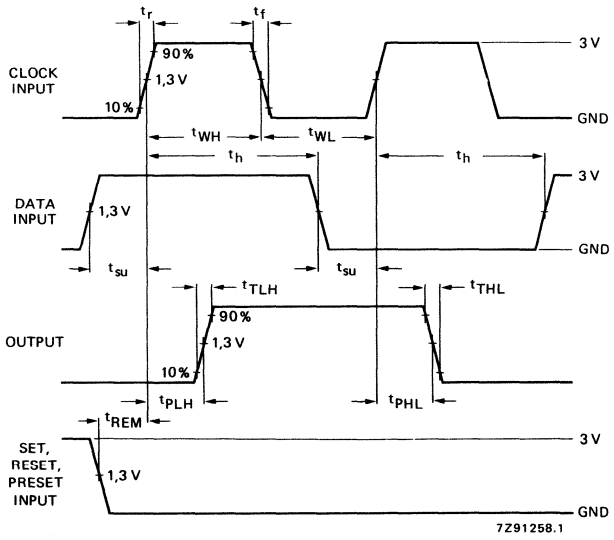


Fig. 9 Set-up times, hold times, removal times and propagation delays for sequential logic ICs.

Note to Fig. 9

In Fig. 9 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.

TEST CIRCUIT FOR PC54HCT; PC74HCT

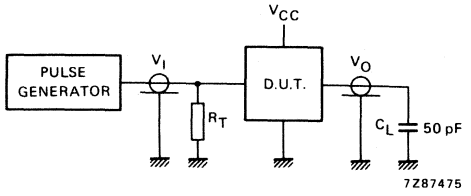


Fig. 10 Test circuit.

Definitions for Fig. 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HCT TYPES (continued)

AC WAVEFORMS PC54HCT; PC74HCT (continued)

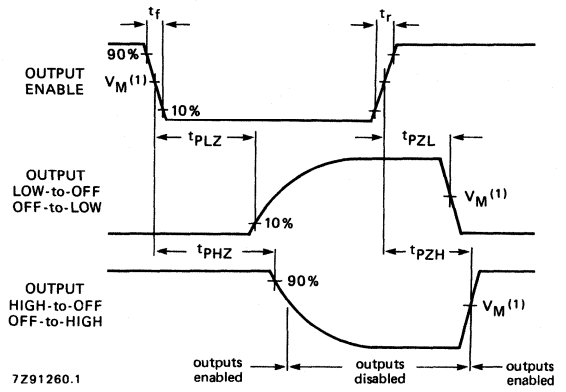
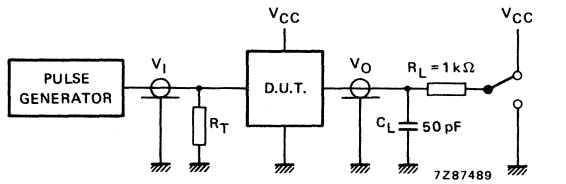


Fig. 11 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR PC54HCT; PC74HCT



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 12 Test circuit for 3-state outputs.

Definitions for Fig. 12:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

INTRODUCTION

The HCMOS HC/HCT/HCU data sheets have been configured for quick usability.

They are self-contained and should require minimum reference to other sections for amplifying information.

For examples of AC waveforms and test circuits see section "FAMILY CHARACTERISTICS".

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part with a 15 pF load.

In case of clocked products, this is sometimes the maximum frequency of operation. In any event, this number is under the operating conditions of V_{CC} = 5.0 V and T_{amb} = 25 °C.

For the typical operating frequency this is the maximum device operating frequency with 50% duty factor and no constraints on t_r and t_f.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol", explicitly shows the internal logic (except for complex logic). The other is "IEC Logic Symbol" as developed by the IEC (International Electrotechnical Commission).

IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that consolidates the original work started in the mid-1960's and published in 1972 (Publication 117-15), and the amendments and supplements that have been followed.

RATINGS

The "RATINGS" table (Limiting values in accordance with the Absolute Maximum System - IEC134) carries the maximum limits to which the device can be subjected without damaging it; there is no implication that the device will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than -0.5 V is applied to the output pin, after that voltage is removed, the device will still be functional and its useful life will not have been shortened. The maximum rated supply voltage of 7 V is well below the typical breakdown voltage of 18 V. The DC input and output diode currents are often referred to, that at these values no latch-up of the devices occur.

RECOMMENDED OPERATING CONDITIONS

The "RECOMMENDED OPERATING CONDITIONS" table has a dual purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the "DC CHARACTERISTICS" table and the "AC CHARACTERISTICS" table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by the manufacturer, but as the conditions used to test the parts and guarantee that they will then meet the limits set forth in the DC and AC CHARACTERISTICS tables.

DC CHARACTERISTICS

This table reflects the DC limits used during the testing operations. The input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment; if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the "DC CHARACTERISTICS" table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the device for functionality in a "function-table exercizer" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the device has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any HCMOS device type. For these types of tests, input voltages of V_{CC} and 0 V should be used for the HIGH and LOW states, respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" HIGHs and LOWs during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several one meter or more. The situation in a system on a PC-board is less severe than in a noisy production environment.

Compared to TTL no output HIGH short-circuit current is specified. The intention of this current, e.g., for calculating propagation delays under capacitive load conditions, is fully covered by the HCMOS output drive graphs and propagation delay increase versus load capacitance.

The quiescent supply current is the leakage current of all the reversed biased diodes and the OFF-state MOS transistors and is tested with the input at V_{CC} or GND. Its value is typically in the low nA region.

AC CHARACTERISTICS

The "AC CHARACTERISTICS" table contains the guaranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section.

TEST CIRCUITS AND WAVEFORMS

For CMOS no load resistor to V_{CC} or GND is applied, because CMOS inputs draw only a negligible amount of input leakage current. Also for HCT outputs, which reference level is the LSTTL established value of 1.3 V, a resistive load is not applied. In case of real TTL loads, the LOW-to- HIGH propagation delay is decreased marginally and the

HIGH-to-LOW propagation delay will increase marginally due to the active DC TTL input current.

The test circuit for 3-state outputs is self explanatory. Special attention needs the disable time definition in the waveforms.

As shown in Fig. 6 (section "FAMILY CHARACTERISTICS" - AC WAVEFORMS for PC54/74HC), the disable times are measured at the point where the output voltage has risen or fallen by 10% of the voltage swing.

Since the rising or falling waveform is RC-controlled, the 10% of change is more linear and is less susceptible to external and circuit influences.

TEST CIRCUIT AND WAVEFORMS (continued)

More importantly, from the system designer's point of view, 10% is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times. To study the break before make characteristic the user may substract the 10% RC-time, being 5 ns, from the values given in the data sheet, in order to know the real internal disable propagation delay.

Good, high-frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lenghts. Input signals should have rise and fall times of 6 ns, a signal swing of 0 V to V_{CC} for HC and 0 V to 3 V for HCT, 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as set-up time, hold time, removal time, ect. f_{max} is also tested with 6 ns input rise and fall times, and a repetition time, with a 50% duty factor, but for typical f_{max} as high as 60 MHz, there are no constraints on rise and fall times.

DEFINITIONS OF SYMBOLS AND TERMS USED IN HCMOS DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

I_{CC} Quiescent power supply current; the current flowing into the V_{CC} supply terminal.

ΔI_{CC} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-state device in the OFF-state, when the output is connected to V_{CC} or GND.

I_S Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels, when applying a positive and a negative-going input signal.

V_{IH} HIGH level input voltage ; the range of input voltages that represents a logic HIGH level in the system.

V_{IL} LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.

V_{OH} HIGH level output voltage ; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Analog terms

R_{ON} ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load.

ΔR_{ON} ΔON-resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.

C_S Switch capacitance; the capacitance of a terminal to a switch of an analog device.

AC switching parameters

f_i Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

f_o Output frequency; each output.

f_{max} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%V_{CC} to 90%V_{CC} in accordance with the device function table.

t_h Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_r, t_f Clock input rise and fall times; 10% and 90% values.

AC switching parameters (continued)

t_{PHL} Propagation delay; the time between the specified reference points, normally the 50% points for PC54/74HC and PC54/74HCU devices on the input and output waveforms and the 1,3 V point for the PC54/74HCT devices, with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH} Propagation delay; the time between the specified reference points, normally the 50% points for PC54/74HC and PC54/74HCU devices on the input and output waveforms and the 1,3 V point for the PC54/74HCT devices, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the PC54/74HC and PC54/74HCU devices and the 1,3 V points for the PC54/74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level (V_{OH}) to a high impedance OFF-state (Z).

t_{PLZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the PC54/74HC and PC54/74HCU devices and the 1,3 V points for the PC54/74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level (V_{OL}) to a high impedance OFF-state (Z).

t_{PZH} 3-state output enable time; the time between the specified reference points, normally the 50% points for the PC54/74HC devices and the 1,3 V points for the PC54/74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level (V_{OH}).

t_{PZL} 3-state output enable time; the time between the specified reference points, normally the 50% points for the PC54/74HC devices and the 1,3 V points for the PC54/74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level (V_{OL}).

t_{rem} Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for PC54/74HC and PC54/74HCU devices and the 1,3 V points for the PC54/74HCT devices on both input voltage waveforms.

t_{su} Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to- LOW.

t_{TLH} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to- HIGH.

t_w Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for PC54/74HC and PC54/74HCU devices and at the 1,3 V points for PC54/74HCT devices.

DEVICE DATA

QUAD 2-INPUT NAND GATE

FEATURES

- **Output capability; standard**

GENERAL DESCRIPTION

The 54/74HC/HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT00 provide the 2-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	8	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT00P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT00D; PC74HC/HCT00D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT00T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

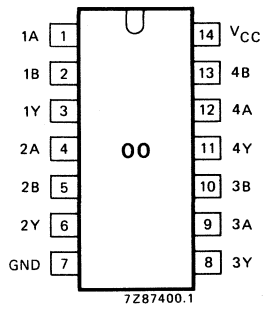


Fig. 1 Pin configuration.

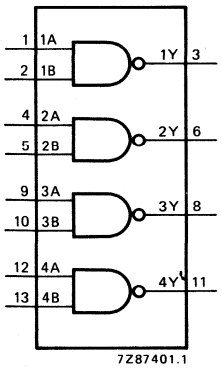


Fig. 2 Logic symbol.

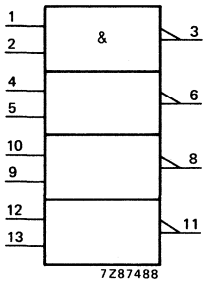


Fig. 3 IEC logic symbol.

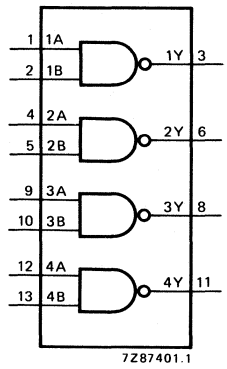


Fig. 4 Functional diagram.

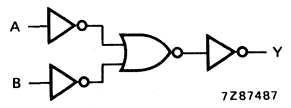


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB	2.20

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			20		25		30	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

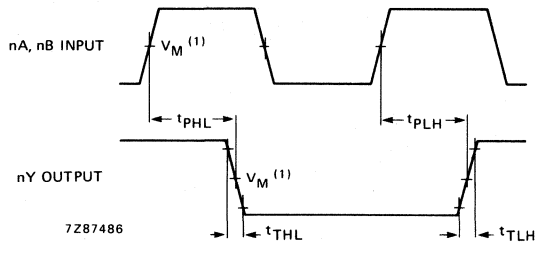


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

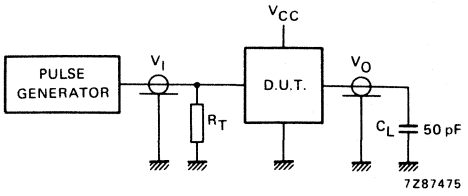


Fig. 7 Test circuit.

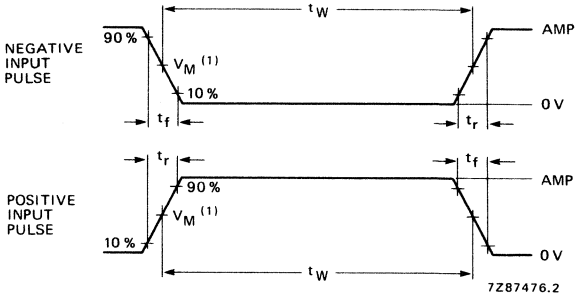


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD 2-INPUT NOR GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT02 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT02 provide the 2-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT02P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT02D; PC74HC/HCT02D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT02T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

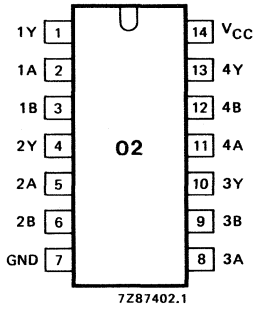


Fig. 1 Pin configuration.

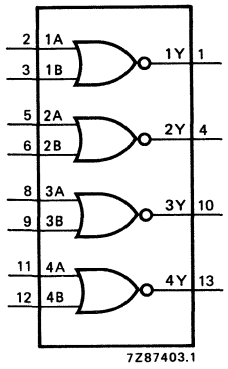


Fig. 2 Logic symbol.

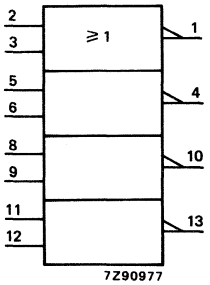


Fig. 3 IEC logic symbol.

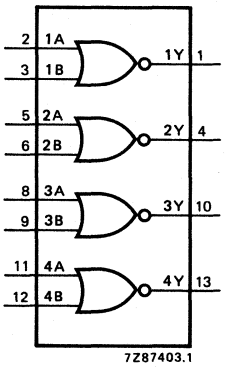


Fig. 4 Functional diagram.

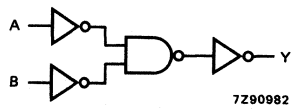


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB	1.50

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			22		28		33	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

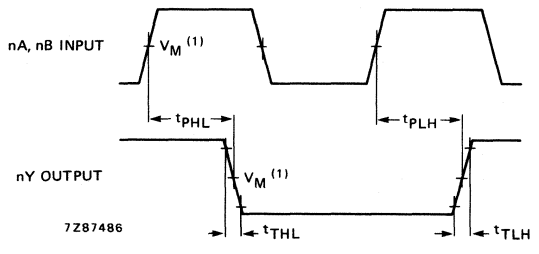


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

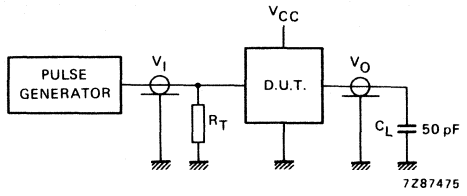


Fig. 7 Test circuit.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

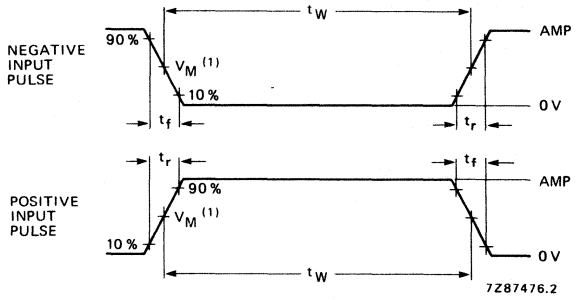


Fig. 8 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

QUAD 2-INPUT NAND GATE

FEATURES

- **Level shift capability**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT03 provide the 2-input NAND function.

The "03" have open-drain N-transistor outputs. For digital operation and OR-tied output applications these devices must have a pull-up resistor to establish a logic HIGH level.

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT03P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT03D; PC74HC/HCT03D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT03T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

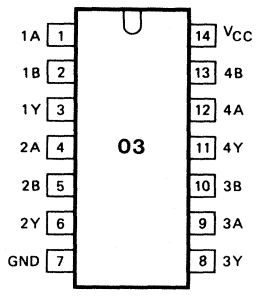


Fig. 1 Pin configuration.

HEX INVERTER

FEATURES

- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT04 provide six inverting buffers.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	6	8	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	21	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT04P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT04D; PC74HC/HCT04D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT04T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 4A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

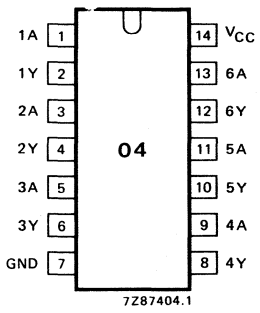


Fig. 1 Pin configuration.

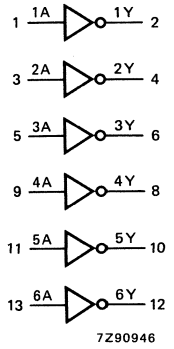


Fig. 2 Logic symbol.

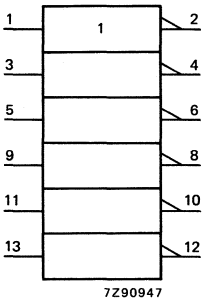


Fig. 3 IEC logic symbol.

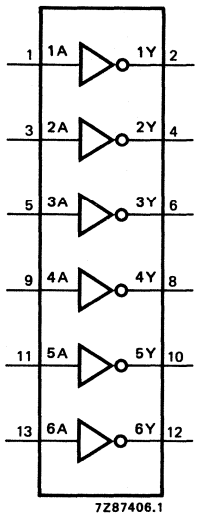


Fig. 4 Functional diagram.

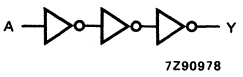


Fig. 5 Logic diagram (one inverter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA	1.20

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay nA to nY			80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 6
t_{PLH}	propagation delay nA to nY			85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY			20		25		30	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

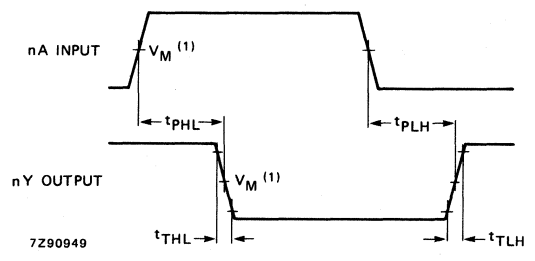


Fig. 6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

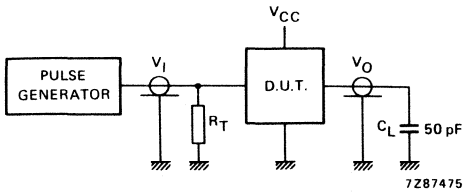


Fig. 7 Test circuit.

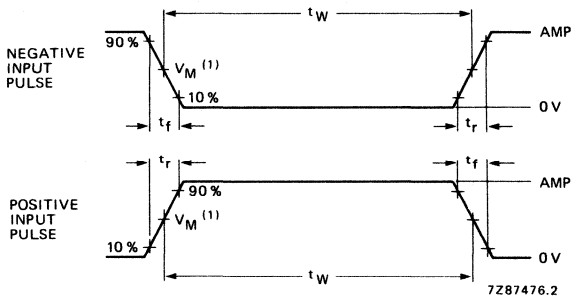


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

HEX INVERTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HCU is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7.

The PC54/74HCU04 is a general purpose hex inverter. Each of the six inverters is a single stage.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	5	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per inverter	notes 1 and 2	10	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. V_I = GND to V_{CC}

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HCU04P: 14-lead DIL; plastic (SOT-27).
PC54HCU04D; PC74HCU04D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HCU04T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

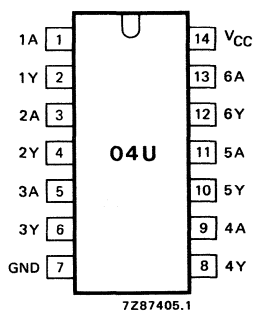


Fig. 1 Pin configuration.

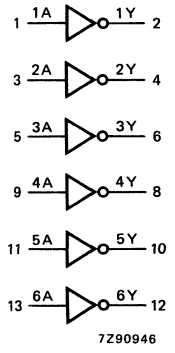


Fig. 2 Logic symbol.

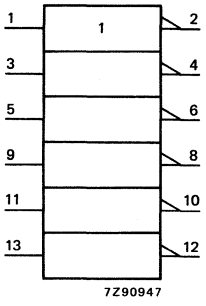


Fig. 3 IEC logic symbol.

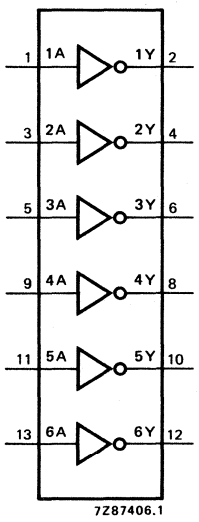


Fig. 4 Functional diagram.

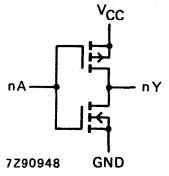


Fig. 5 Schematic diagram (one inverter).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HCU
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		200	mW	above +70°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HCU
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	V	
T_{amb}	operating ambient temperature range 74HCU	-40		+85	°C	
T_{amb}	operating ambient temperature range 54HCU	-55		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCU			74HCU		54HCU			V_{CC} V	V_I	OTHER
		+25			-40 to +85		-55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5			1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage			0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	I_O = 0

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCU			74HCU		54HCU			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY			70 14 12		90 18 15		105 21 18	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS

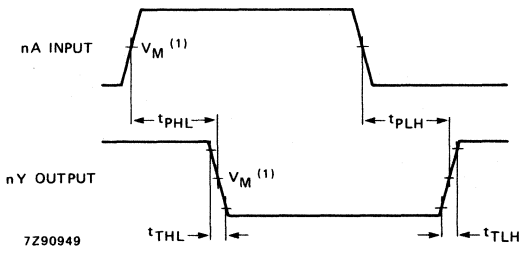


Fig. 6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

TYPICAL TRANSFER CHARACTERISTICS

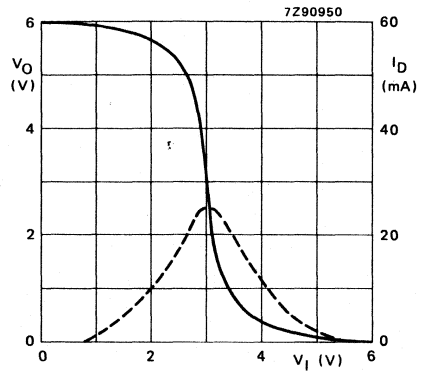


Fig. 7

——— V_O; – – – – I_D (drain current)
I_O = 0; V_{CC} = 6.0 V.

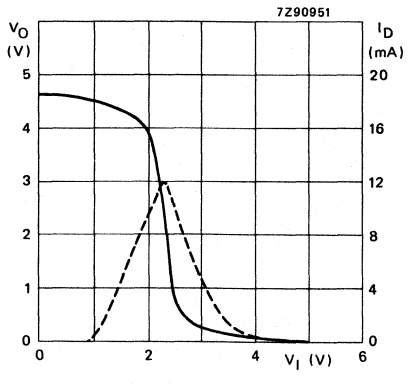


Fig. 8

——— V_O; – – – – I_D (drain current)
I_O = 0; V_{CC} = 4.5 V.

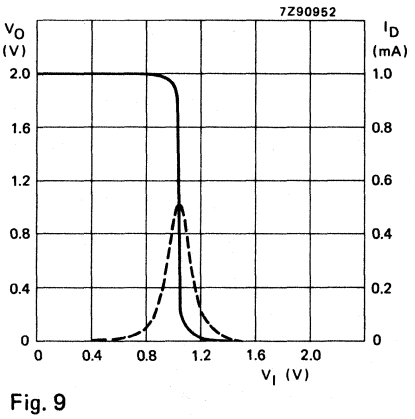


Fig. 9

——— V_O; – – – – I_D (drain current)
I_O = 0; V_{CC} = 2.0 V.

QUAD 2-INPUT AND GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT08 provide the 2-input AND function.

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT08P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT08D; PC74HC/HCT08D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT08T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

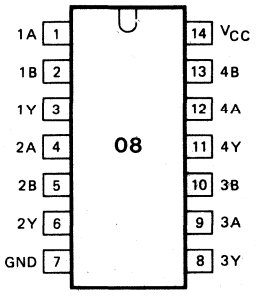


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

TRIPLE 3-INPUT NAND GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT10 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT10 provide the 3-input NAND function.

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT10P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT10D; PC74HC/HCT10D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT10T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
12, 6, 8	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

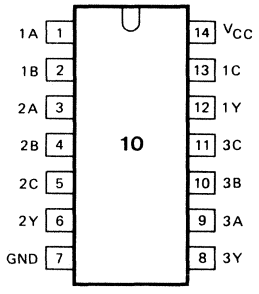


Fig. 1 Pin configuration.

TRIPLE 3-INPUT AND GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT11 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT11 provide the 3-input AND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 5 V	10	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	26	28	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT11P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT11D; PC74HC/HCT11D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT11T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
13, 5, 11	1C to 3C	data outputs
14	V_{CC}	positive supply voltage

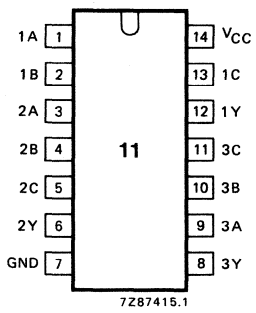


Fig. 1 Pin configuration.

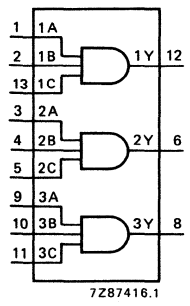


Fig. 2 Logic symbol.

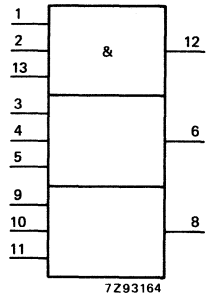


Fig. 3 IEC logic symbol.

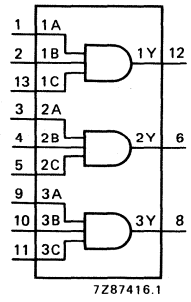


Fig. 4 Functional diagram.

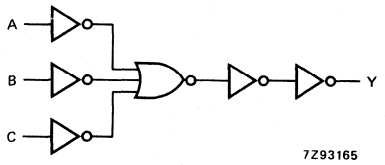


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	I_O = 0

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB, nC	0.5

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition times			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY			28		35		42	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition times			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

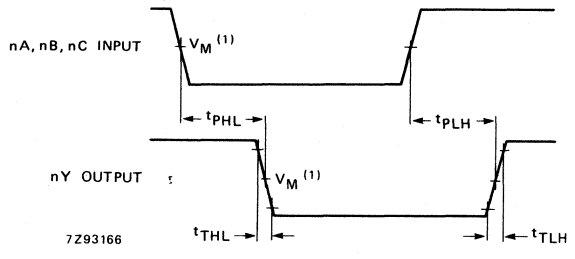


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

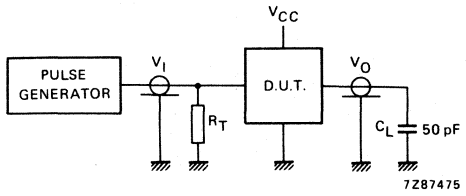


Fig. 7 Test circuit.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

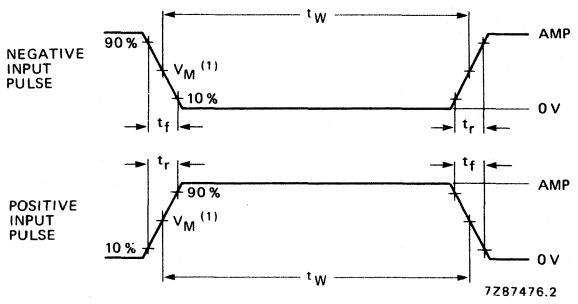


Fig. 8 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

HEX INVERTING SCHMITT TRIGGER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT14 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

APPLICATIONS

- **Wave and pulse shapers**
- **Astable multivibrators**
- **Monostable multivibrators**

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	10	12	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT14P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT14D; PC74HC/HCT14D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT14T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

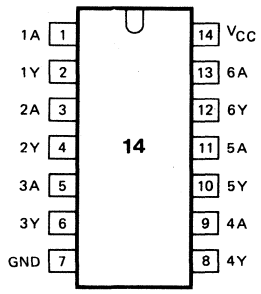


Fig. 1 Pin configuration.

DUAL 4-INPUT NAND GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT20 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT20 provide the 4-input NAND function.

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT20P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT20D; PC74HC/HCT20D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT20T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

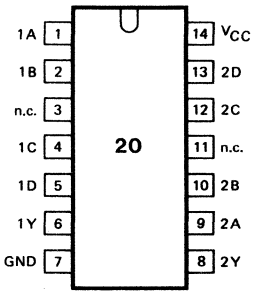


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

DUAL 4-INPUT AND GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT21 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT21 provide the 4-input AND function.

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT21P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT21D; PC74HC/HCT21D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT21T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

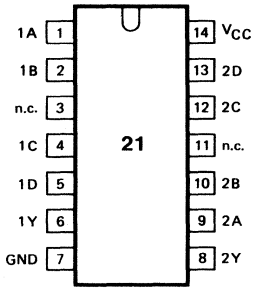


Fig. 1 Pin configuration.

TRIPLE 3-INPUT NOR GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT27 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT27 provide the 3-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 5 V	8	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	24	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT27P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT27D; PC74HC/HCT27D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT27T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
14	V_{CC}	positive supply voltage

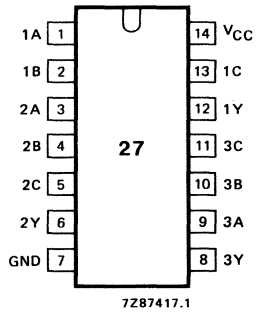


Fig. 1 Pin configuration.

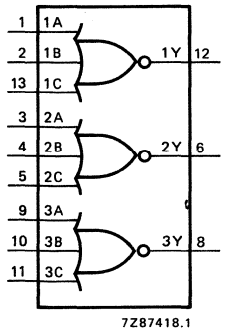


Fig. 2 Logic symbol.

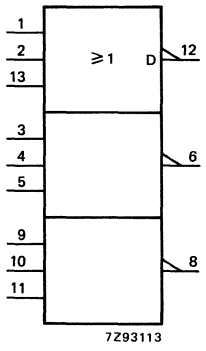


Fig. 3 IEC logic symbol.

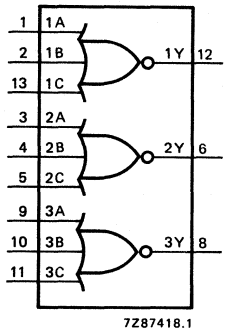


Fig. 4 Functional diagram.

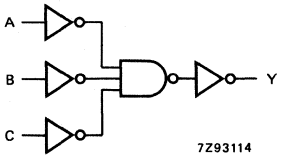


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB, nC	1.50

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY			24		30		36	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

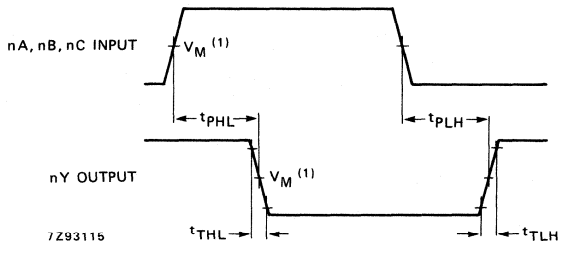


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

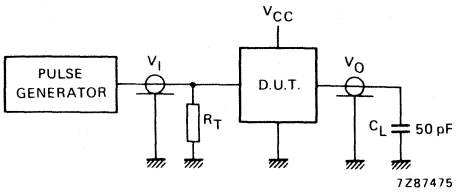


Fig. 7 Test circuit.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

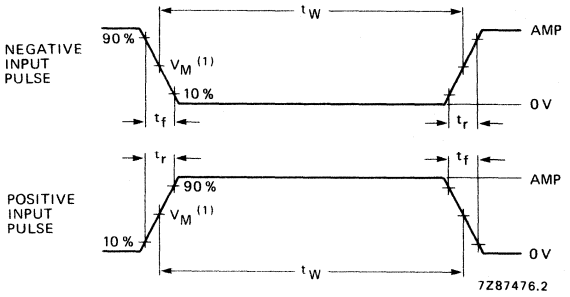


Fig. 8 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

8-INPUT NAND GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT30 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT30 provide the 8-input NAND function.

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A, B, C, D, E, F, G, H to Y	C_L = 15 pF; V_{CC} = 5 V	10	12	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT30P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT30D; PC74HC/HCT30D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT30T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	A	data input
2	B	data input
3	C	data input
4	D	data input
5	E	data input
6	F	data input
7	GND	ground (0 V)
8	Y	data output
9, 10, 13	n.c.	not connected
11	G	data input
12	H	data input
14	V_{CC}	positive supply voltage

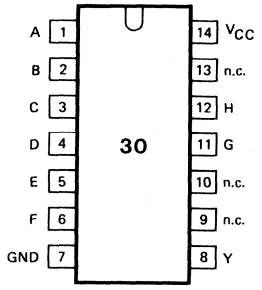


Fig. 1 Pin configuration.

QUAD 2-INPUT OR GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT32 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT32 provide the 2-input OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	6	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	28	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT32P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT32D; PC74HC/HCT32D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT32T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

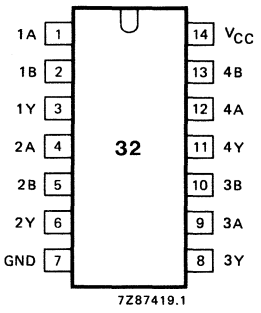


Fig. 1 Pin configuration.

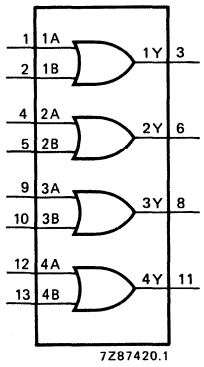


Fig. 2 Logic symbol.

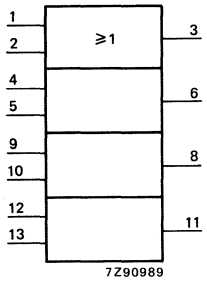


Fig. 3 IEC logic symbol.

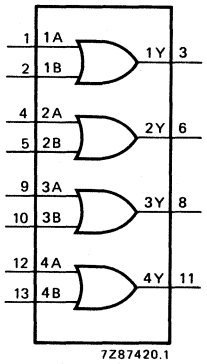


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

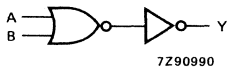


Fig. 5 Logic diagram PC54/74HC (one gate).

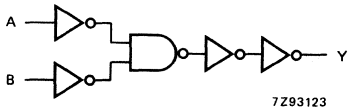


Fig. 6 Logic diagram PC54/74HCT (one gate).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		500	mW	for standard temperature range; −40 to +85 °C; 74HC/HCT above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		500	mW	for extended temperature range; −55 to +125°C; 54HC/HCT above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB	1.20

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay nA, nB to nY			22		28		33	ns	4.5	Fig. 7
t_{PLH}	propagation delay nA, nB to nY			18		23		27	ns	4.5	Fig. 7
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS

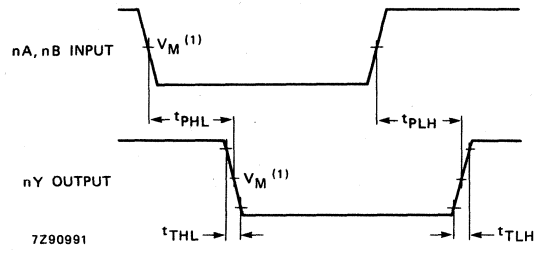


Fig. 7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

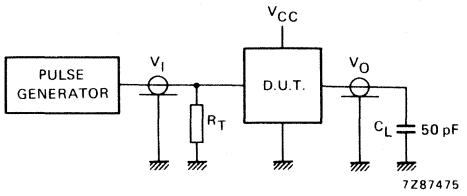


Fig. 8 Test circuit.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

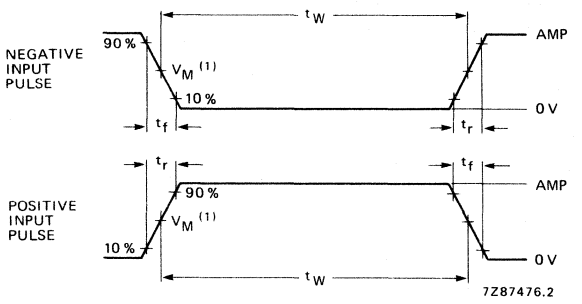


Fig. 9 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BCD TO DECIMAL DECODER (1-OF-10)

FEATURES

- Mutually exclusive outputs
- 1-of-8 demultiplexing capability
- Outputs disabled for input codes above nine
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT42 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT42 decoders accept four active HIGH BCD inputs and provide 10 mutually exclusive active LOW outputs. The active LOW outputs facilitate addressing other MSI circuits with active LOW input enables.

The logic design of the "42" ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input (A_3) produces a useful inhibit function when the "42" is used as a 1-of-8 decoder. The A_3 input can also be used as the data input in an 8-output demultiplexer application.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	14	16	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT42P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT42D; PC74HC/HCT42D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT42T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 9, 10, 11	$\overline{Y}_0$ to $\overline{Y}_6$	multiplexer outputs
8	GND	ground (0 V)
15, 14, 13, 12	A_0 to A_3	data inputs
16	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS									
A_3	A_2	A_1	A_0	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	$\overline{Y}_8$	$\overline{Y}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage level
L = LOW voltage level

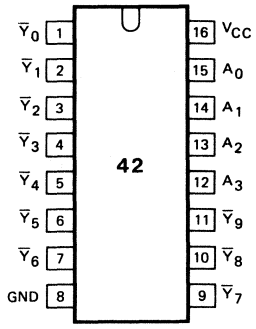


Fig. 1 Pin configuration.

DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT73 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT73 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ $n\overline{CP}$ to $n\overline{Q}$ $n\overline{R}$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 5 V	 16 14 14	 18 15 17	 ns ns ns
f_{max}	maximum clock frequency		58	40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT73P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT73D; PC74HC/HCT73D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT73T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5	$1\overline{CP}$, $2\overline{CP}$	clock input (LOW-to-HIGH, edge-triggered)
2, 6	$1\overline{R}$, $2\overline{R}$	asynchronous reset inputs (active LOW)
4	V_{CC}	positive supply voltage
11	GND	ground (0 V)
12, 9	1Q, 2Q	true flip-flop outputs
13, 8	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
14, 7, 3, 10	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2

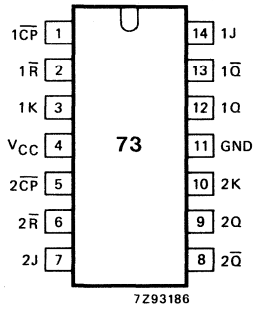


Fig. 1 Pin configuration.

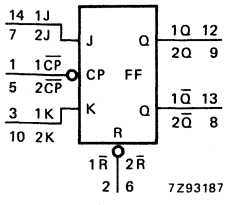


Fig. 2 Logic symbol.

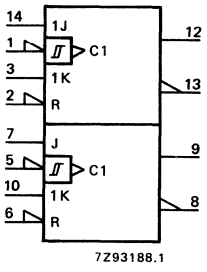


Fig. 3 IEC logic symbol.

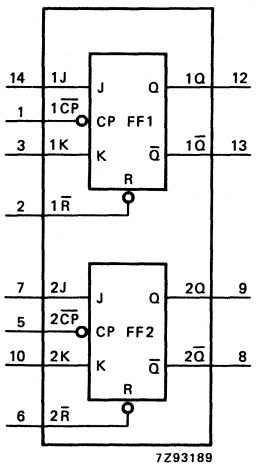


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$n\overline{R}$	$n\overline{CP}$	J	K	Q	$\overline{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	$\overline{q}$	q
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↓ = HIGH-to-LOW CP transition

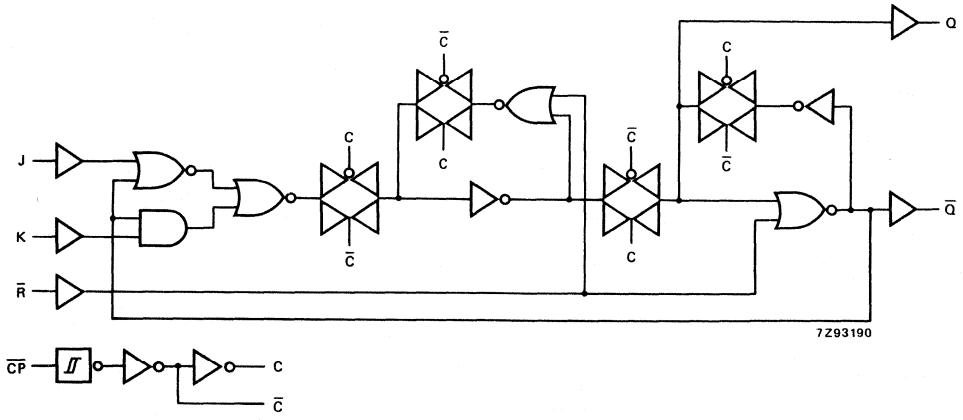


Fig. 5 Logic diagram (one flip-flop).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			4.0		40.0		80.0	μA	6.0	V_{CC} or GND	I_O = 0

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			4.0		40.0		80.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nJ, nK	0.35
$n\overline{R}$	0.35
$n\overline{CP}$	0.35

AC CHARACTERISTICS FOR 54/74HC

GND =0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	90 18 15			115 23 20		135 27 15		ns	2.0 4.5 6.0	Fig. 6
t_W	reset pulse width LOW	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	
t_{su}	set-up time nJ, nK to $n\overline{CP}$	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	4 4 4			4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum maximum clock pulse frequency	5 27 32			4 22 26		4 18 21		MHz	2.0 4.5 6.0	Fig. 6

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ			43		54		65	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$			36		45		54	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$			40		50		60	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	24			33		39		ns	4.5	Fig. 6
t_W	reset pulse width LOW	20			25		30		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	12			15		18		ns	4.5	
t_{su}	set-up time nJ, nK to $n\overline{CP}$	12			15		18		ns	4.5	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	6			8		9		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	22			18		15		MHz	4.5	Fig. 6

AC WAVEFORMS

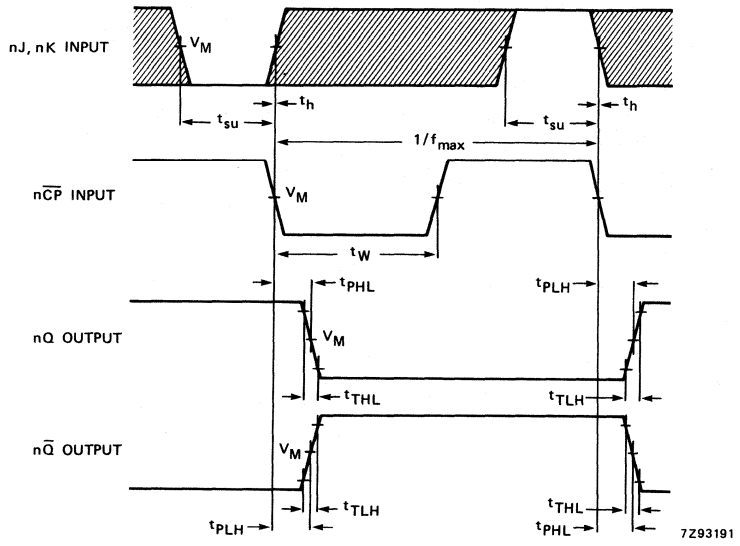


Fig. 6 Waveforms showing the clock (n$\overline{CP}$) to output (nQ, nQ̄) propagation delays, the clock pulse width, the J and K to n$\overline{CP}$ set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

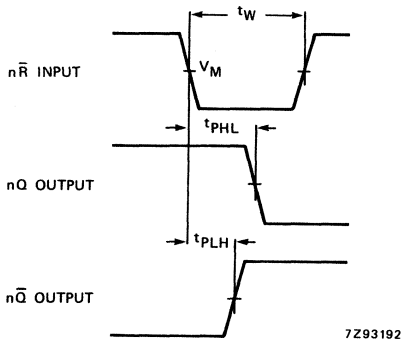


Fig. 7 Waveforms showing the reset (nR̄) input to output (nQ, nQ̄) propagation delays and the reset pulse width.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

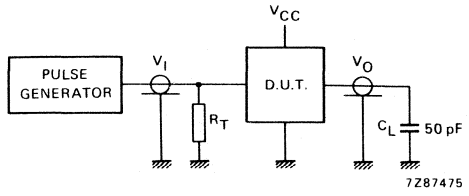


Fig. 8 Test circuit.

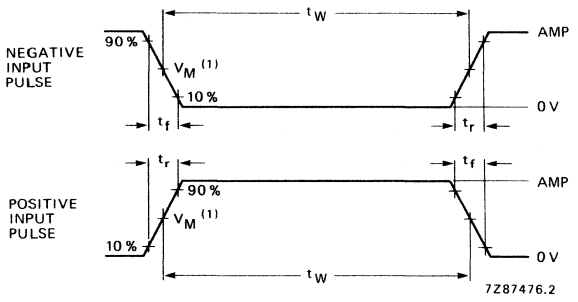


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT74 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT74 are dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 5 V	 14 17 17	 14 17 17	 ns ns ns
f_{max}	maximum clock frequency		60	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	24	29	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT74P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT74D; PC74HC/HCT74D 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT74T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{R}_D$, $2\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	data inputs
3, 11	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
4, 10	$1\overline{S}_D$, $2\overline{S}_D$	asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

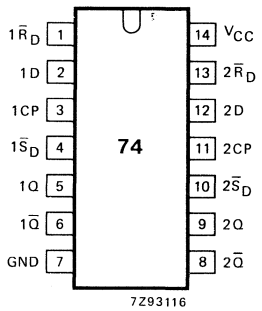


Fig. 1 Pin configuration.

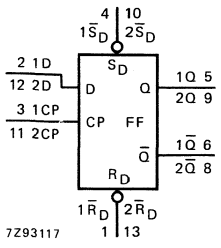


Fig. 2 Logic symbol.

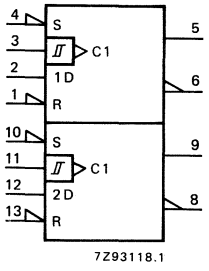


Fig. 3 IEC logic symbol.

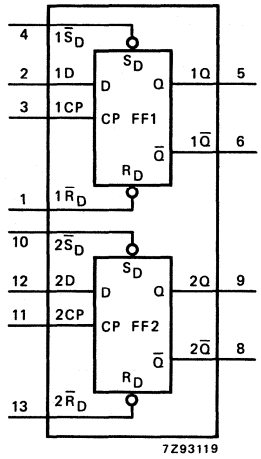


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	↑	L	L	H
L	L	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

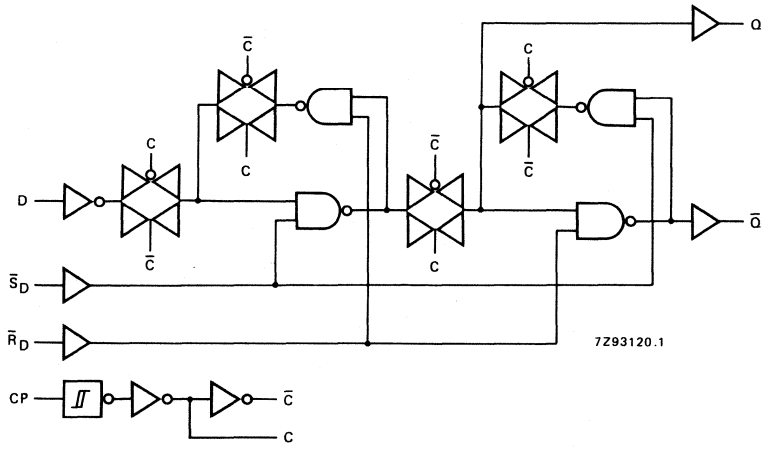


Fig. 5 Logic diagram (one flip-flop).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			4.0		40.0		80.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			4.0		40.0		80.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nD	0.70
$n\overline{R}_D$	0.70
$n\overline{S}_D$	0.80
nCP	0.80

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	set or reset pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time set or reset	30 6 5			40 8 7		45 9 8		ns	2.0 4.5 6.0	
t_{su}	set-up time nD to nCP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nCP to nD	3 3 3			3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$			35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$			40		50		60	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$			40		50		60	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 6
t_W	set or reset pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 7
t_{rem}	removal time set or reset	6			8		9		ns	4.5	
t_{su}	set-up time nD to nCP	20			25		30		ns	4.5	Fig. 6
t_h	hold time nCP to nD	3			3		3		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	25			20		17		ns	4.5	Fig. 6

AC WAVEFORMS

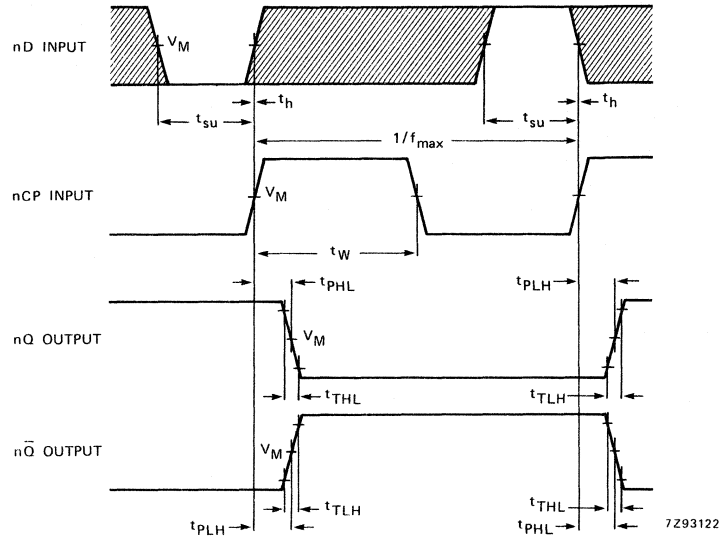


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

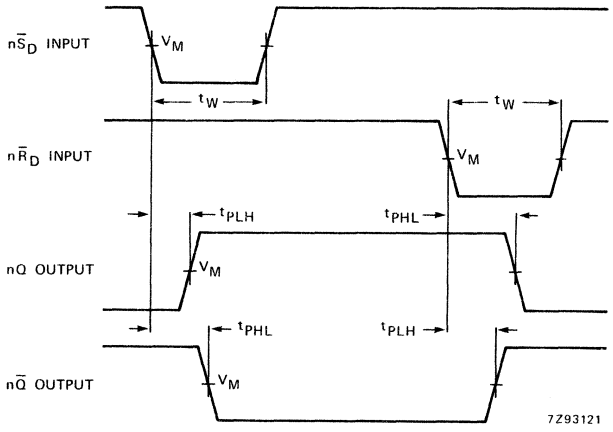


Fig. 7 Waveforms showing the set and reset input to output (nQ, nQ̄) propagation delays and the set and reset pulse width.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

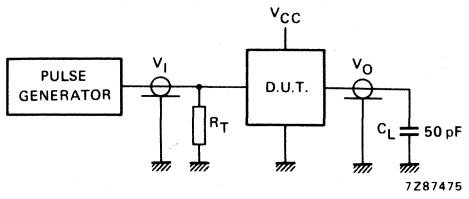


Fig. 8 Test circuit.

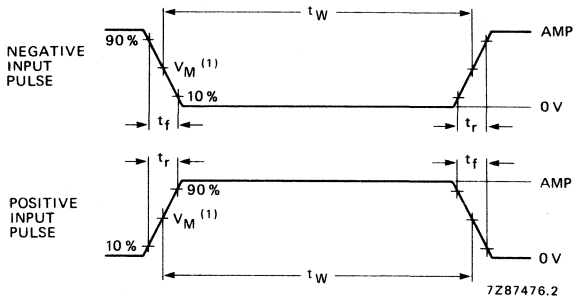


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

QUAD BISTABLE TRANSPARENT LATCH

FEATURES

- Complementary Q and $\overline{Q}$ outputs
- V_{CC} and GND on the centre pins
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT75 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT75 have four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs (LE_{1-2} and LE_{3-4}). When LE_{n-n} is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LE_{n-n} is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LE_{n-n} will be stored in the latches. The latched outputs remain stable as long as the LE_{n-n} is LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n, $\overline{Q}_n$ LE_{n-n} to Q_n, $\overline{Q}_n$	C_L = 15 pF V_{CC} = 5 V	9 11	11 12	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	42	42	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT75D;
PC74HC/HCT75P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT75D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT75T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 14, 11, 8	$1\overline{Q}$ to $4\overline{Q}$	complementary latch outputs
2, 3, 6, 7	1D to 4D	data inputs
4	LE_{3-4}	latch enable input, latches 3 and 4 (active HIGH)
5	V_{CC}	positive supply voltage
12	GND	ground (0 V)
13	LE_{1-2}	latch enable input, latches 1 and 2 (active HIGH)
16, 15, 10, 9	1Q to 4Q	latch outputs

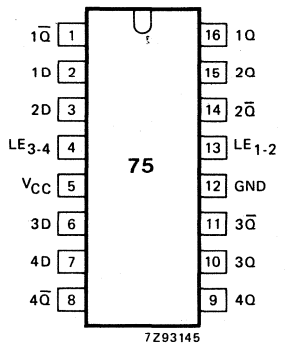


Fig. 1 Pin configuration.

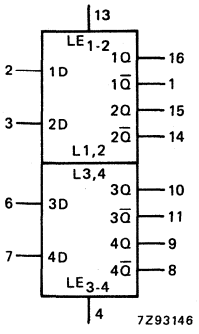


Fig. 2 Logic symbol.

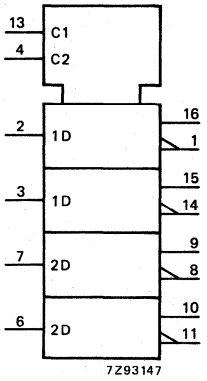


Fig. 3 IEC logic symbol.

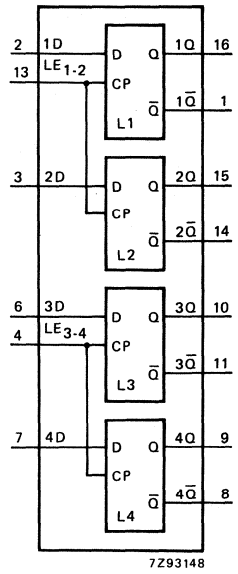


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS		OUTPUTS	
	$LE_{n\text{-}n}$	nD	nQ	$n\bar{Q}$
data enabled	H H	L H	L H	H L
data latched	L	X	q	$\bar{q}$

H = HIGH voltage level
L = LOW voltage level
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH $LE_{n\text{-}n}$ transition
X = don't care

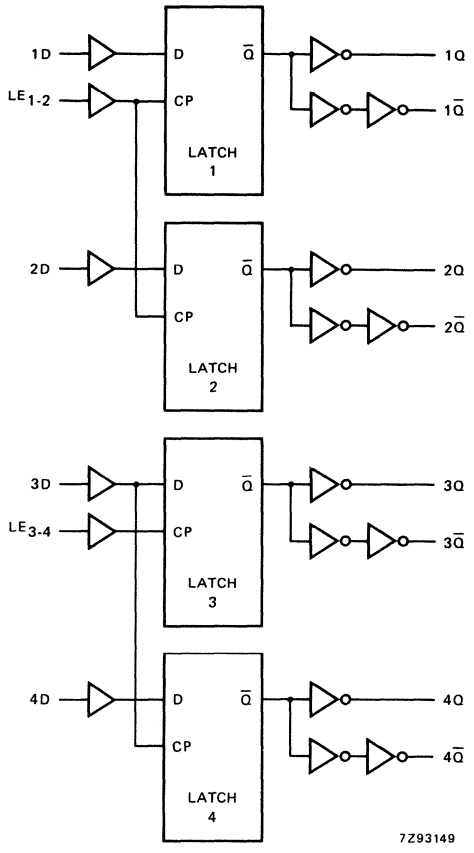


Fig. 5 Logic diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nD	0.75
$LE_{n\text{-}n}$	1.00

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nD to nQ			110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay nD to n$\overline{Q}$			120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $LE_{n\text{-}n}$ to nQ			120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $LE_{n\text{-}n}$ to n$\overline{Q}$			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t_W	enable pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time nD to $LE_{n\text{-}n}$	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time nD to $LE_{n\text{-}n}$	3 3 3			3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 9

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nD to nQ			28		35		42	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay nD to $n\overline{Q}$			28		35		42	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $LE_{n\text{-}n}$ to nQ			28		35		42	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $LE_{n\text{-}n}$ to $n\overline{Q}$			30		38		45	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7
t_W	enable pulse width HIGH	16			20		24		ns	4.5	Fig. 8
t_{su}	set-up time nD to $LE_{n\text{-}n}$	12			15		18		ns	4.5	Fig. 9
t_h	hold time nD to $LE_{n\text{-}n}$	3			3		3		ns	4.5	Fig. 9

AC WAVEFORMS

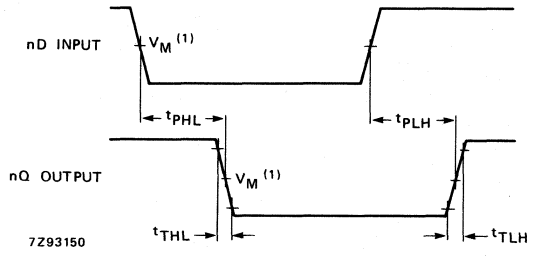


Fig. 6 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

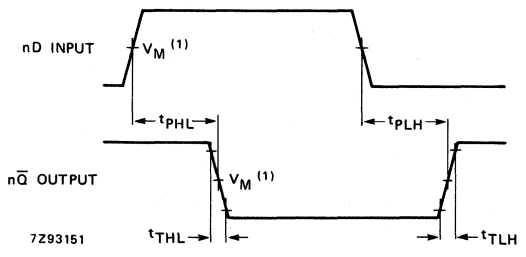


Fig. 7 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

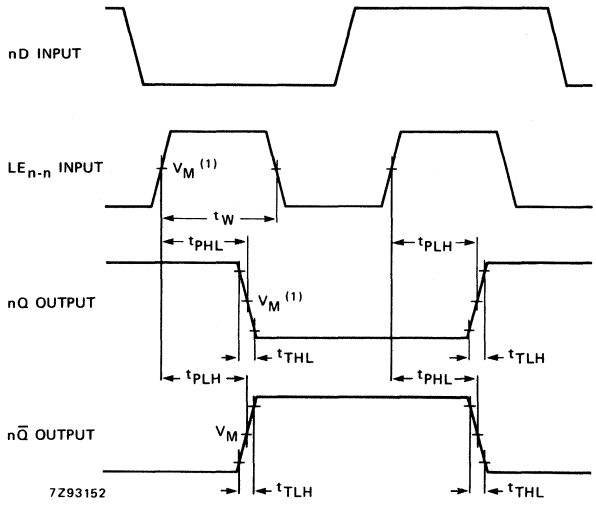


Fig. 8 Waveforms showing the latch enable input (LE_{n-n}) pulse width, the latch enable input to outputs (nQ, $n\overline{Q}$) propagation delays and the output transition times.

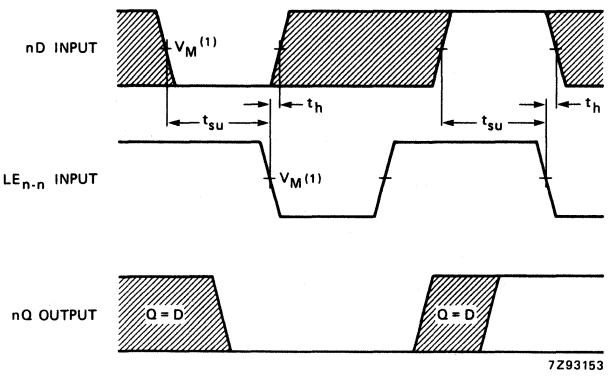


Fig. 9 Waveforms showing the data set-up and hold times for nD input to LE_{n-n} input.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

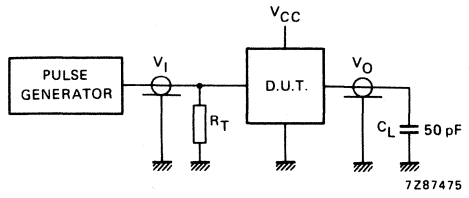


Fig. 10 Test circuit.

Definitions for Figs 10 and 11:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

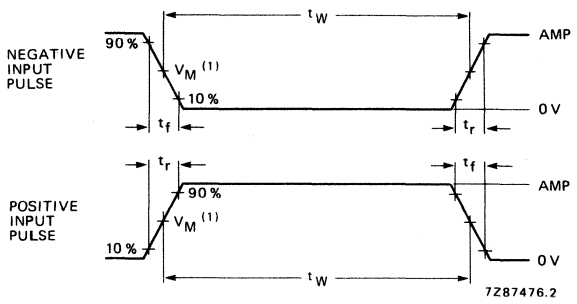


Fig. 11 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

4-BIT MAGNITUDE COMPARATOR

FEATURES

- **Serial or parallel expansion without extra gating**
- **Magnitude comparison of any binary words**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT85 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT85 are 4-bit magnitude comparators that can be expanded to almost any length. They perform comparison of two 4-bit binary, BCD or other monotonic codes and present the three possible magnitude results at the outputs ($Q_{A>B}$, $Q_{A=B}$ and $Q_{A<B}$). The 4-bit inputs are weighted (A_0 to A_3 and B_0 to B_3), where A_3 and B_3 are the most significant bits.

The operation of the "85" is described in the function table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed forward conditions that excist in the parallel expansion scheme.

For proper compare operation the expander inputs ($I_{A>B}$, $I_{A=B}$ and $I_{A<B}$) to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} =$ = LOW and $I_{A=B}$ = HIGH.
For words greater than 4-bits, units can be cascaded by connecting outputs $Q_{A<B}$, $Q_{A>B}$ and $Q_{A=B}$ to the corresponding inputs of the significant comparator.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A>B}$, $Q_{A<B}$ A_n, B_n to $Q_{A=B}$ $I_{A<B}$, $I_{A=B}$, $I_{A>B}$ to $Q_{A<B}$, $Q_{A>B}$ $I_{A=B}$ to $Q_{A=B}$	C_L = 15 pF V_{CC} = 5 V	 18 14 12 9	 18 20 15 15	 ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	18	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT85P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT85D; PC74HC/HCT85D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT85T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2	$I_{A<B}$	A < B expansion input
3	$I_{A=B}$	A = B expansion input
4	$I_{A>B}$	A > B expansion input
5	$Q_{A>B}$	A > B output
6	$Q_{A=B}$	A = B output
7	$Q_{A<B}$	A < B output
8	GND	ground (0 V)
9, 11, 14, 1,	B_0 to B_3	word B inputs
10, 12, 13, 15	A_0 to A_3	word A inputs
16	V_{CC}	positive supply voltage

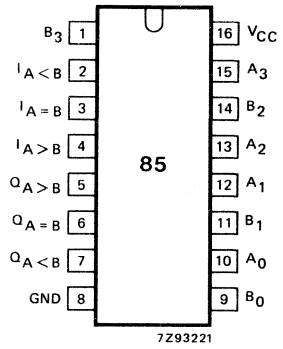


Fig. 1 Pin configuration.

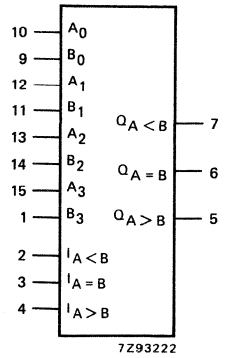


Fig. 2 Logic symbol.

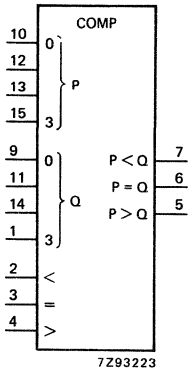


Fig. 3 IEC logic symbol.

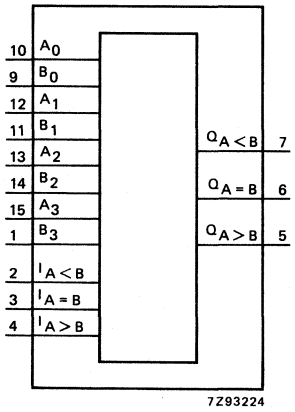


Fig. 4 Functional diagram.

APPLICATIONS

- Process controllers
- Servo-motor control

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$Q_{A>B}$	$Q_{A<B}$	$Q_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

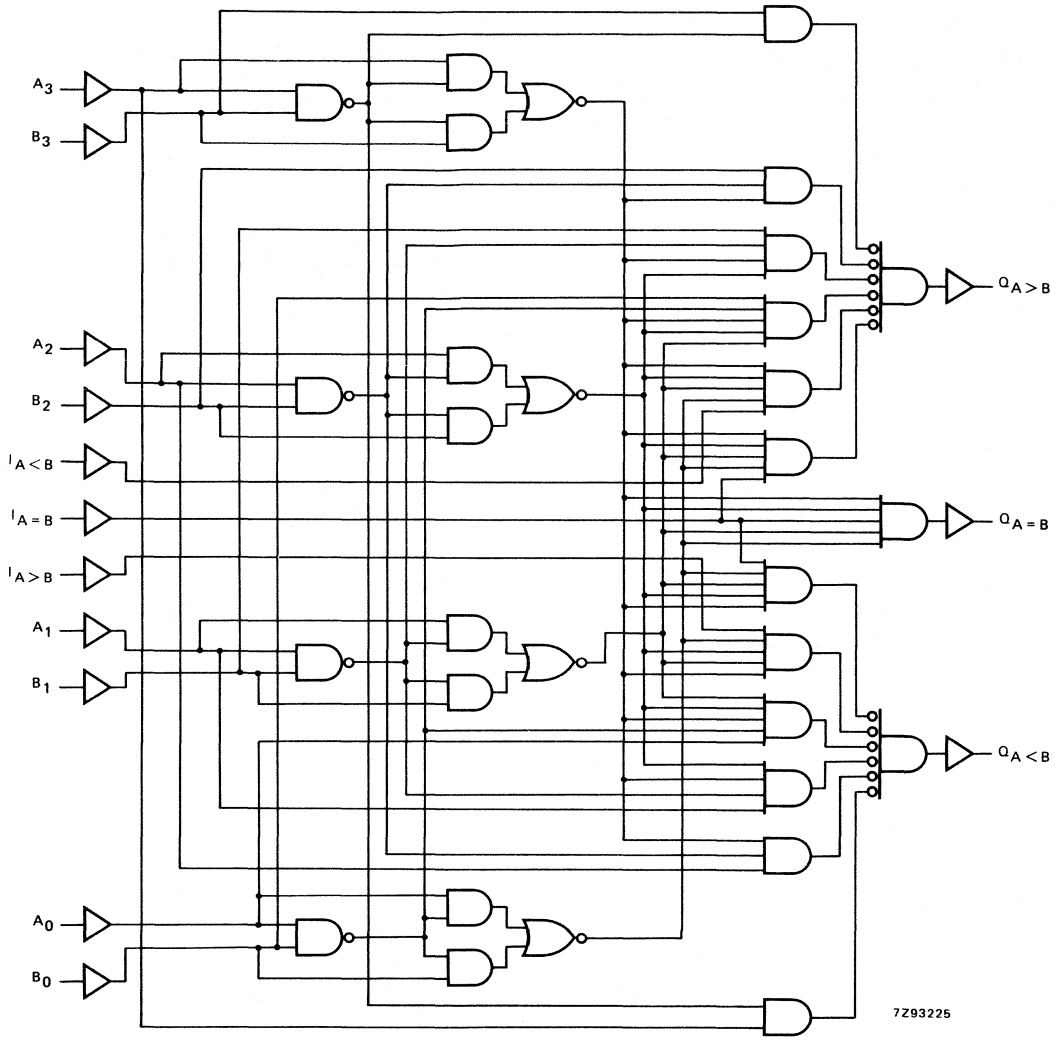


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$I_{A<B}$	1.00
$I_{A>B}$	1.00
$I_{A=B}$	1.50
A_n, B_n	1.50

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A>B}$ or $Q_{A<B}$			210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A=B}$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $I_{A<B}$, $I_{A=B}$, $I_{A>B}$ to $Q_{A<B}$, $Q_{A>B}$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $I_{A=B}$ to $Q_{A=B}$			120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A>B}$ or $Q_{A<B}$			44		55		66	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A=B}$			48		60		72	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $I_{A<B}$, $I_{A=B}$, $I_{A>B}$ to $Q_{A<B}$, $Q_{A>B}$			36		45		54	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $I_{A=B}$ to $Q_{A=B}$			36		45		54	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

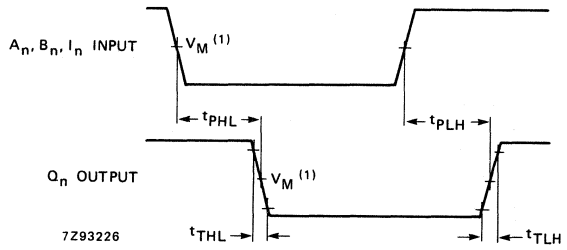


Fig. 6 Waveforms showing the word A inputs (A_n), word B inputs (B_n) and expansion inputs (I_n) to the outputs (Q_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

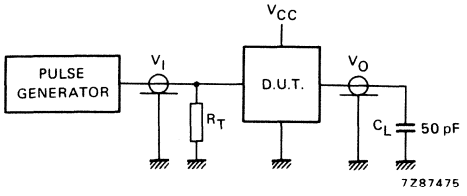


Fig. 7 Test circuit.

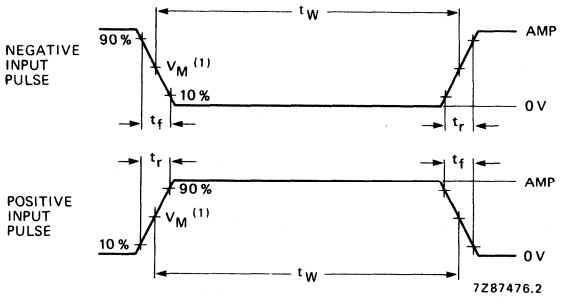


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD 2-INPUT EXCLUSIVE–OR GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT86 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT86 provide the EXCLUSIVE–OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	12	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT86D; PC74HC/HCT86P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT86D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT86T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

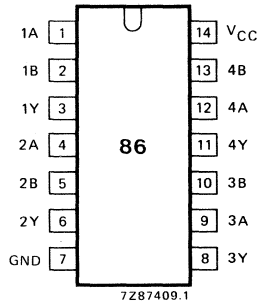


Fig. 1 Pin configuration.

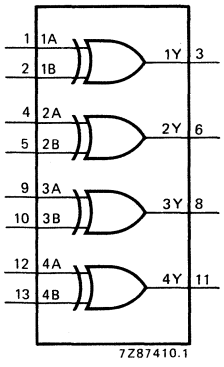


Fig. 2 Logic symbol.

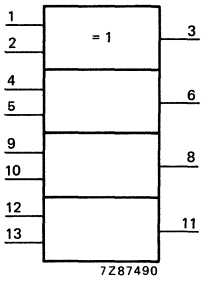


Fig. 3 IEC logic symbol.

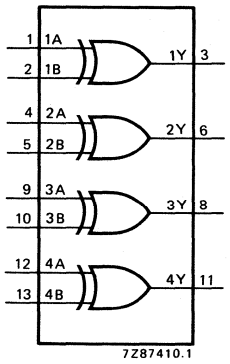


Fig. 4 Functional diagram.

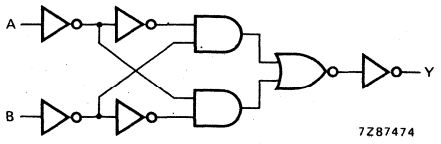


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; –40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; –55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	–40		+85	–40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	–55		+125	–55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB	1.0

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY			32		40		48	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

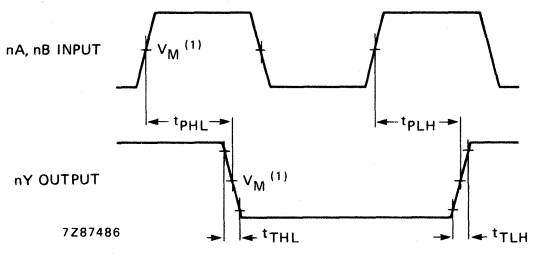


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

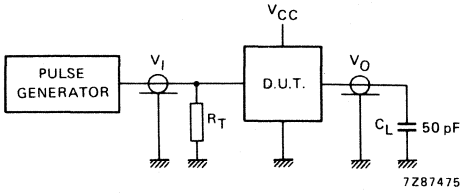


Fig. 7 Test circuit.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

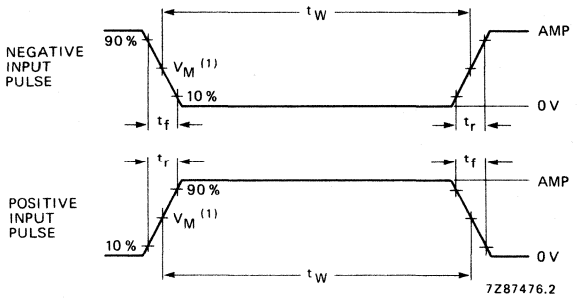


Fig. 8 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

4-BIT BINARY RIPPLE COUNTER

FEATURES

- Various counting modes
- Asynchronous master reset
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT93 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT93 are 4-bit binary ripple counters. The devices consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP}_0$ and $\overline{CP}_1$) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR_1 and MR_2) is provided which overrides both clocks and resets (clears) all flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.
In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to clock input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$.
Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

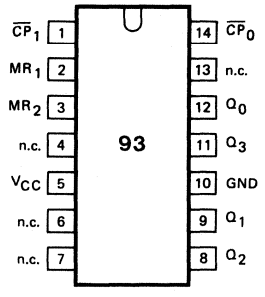


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_n$ to Q_n	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT93P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT93D; PC74HC/HCT93D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT93T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{CP}_1$	clock input 2nd, 3rd and 4th section (HIGH-to-LOW, edge-triggered)
2, 3	MR_1, MR_2	asynchronous master reset (active HIGH)
4, 6, 7, 13	n.c.	not connected
5	V_{CC}	positive supply voltage
10	GND	ground (0 V)
12, 9, 8, 11	Q_0 to Q_3	flip-flop outputs
14	$\overline{CP}_0$	clock input 1st section (HIGH-to-LOW, edge-triggered)

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	count			
H	L	count			
L	L	count			

Note to function table

Output Q_0 connected to $\overline{CP}_1$.

H = HIGH voltage level
L = LOW voltage level

DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT107 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT107 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ $n\overline{CP}$ to $n\overline{Q}$ $n\overline{R}$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 5 V	 17 14 14	 20 15 17	 ns ns ns
f_{max}	maximum clock frequency		54	39	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT107D; PC74HC/HCT107P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT107D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT107T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2
2, 6	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
3, 5	1Q, 2Q	true flip-flop outputs
7	GND	ground (0 V)
12, 9	$1\overline{CP}$, $2\overline{CP}$	clock input (LOW-to-HIGH, edge-triggered)
13, 10	$1\overline{R}$, $2\overline{R}$	asynchronous reset inputs (active LOW)
14	V_{CC}	positive supply voltage

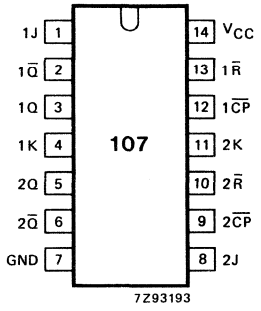


Fig. 1 Pin configuration.

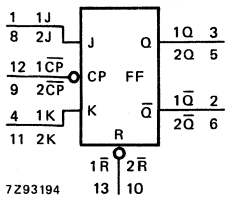


Fig. 2 Logic symbol.

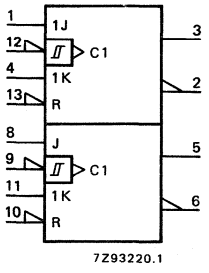


Fig. 3 IEC logic symbol.

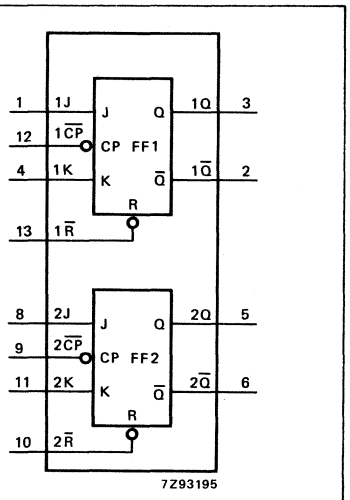


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$n\overline{R}$	$n\overline{CP}$	J	K	Q	$\overline{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	$\overline{q}$	q
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↓ = HIGH-to-LOW CP transition

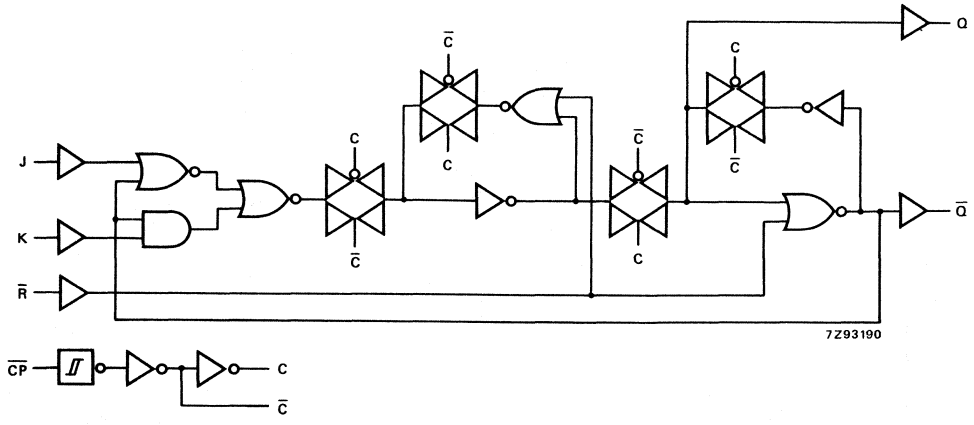


Fig. 5 Logic diagram (one flip-flop).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\ V < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			4.0		40.0		80.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			4.0		40.0		80.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nJ, nK	0.35
$n\overline{R}$	0.35
$n\overline{CP}$	0.35

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HC

GND =0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 6
t_W	reset pulse width LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	
t_{su}	set-up time nJ, nK to $n\overline{CP}$	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	5 25 30			4 20 24		3 17 20		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ			42		53		63	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$			36		45		54	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$			40		50		60	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	24			30		36		ns	4.5	Fig. 6
t_W	reset pulse width LOW	24			30		36		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	12			15		18		ns	4.5	
t_{su}	set-up time nJ, nK to $n\overline{CP}$	16			20		24		ns	4.5	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	5			5		5		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	21			17		14		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

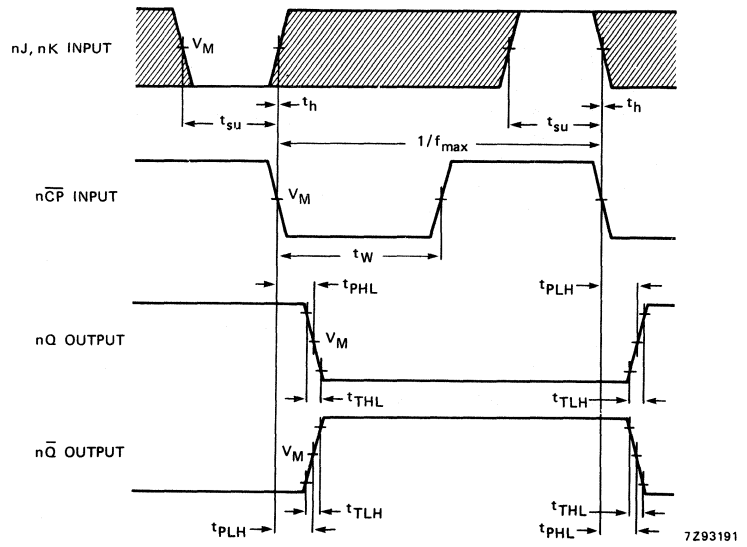


Fig. 6 Waveforms showing the clock (n$\overline{CP}$) to output (nQ, nQ̄) propagation delays, the clock pulse width, the J and K to n$\overline{CP}$ set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

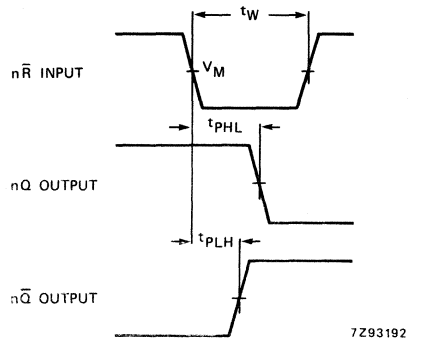


Fig. 7 Waveforms showing the reset (n$\overline{R}$) input to output (nQ, nQ̄) propagation delays and the reset pulse width.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

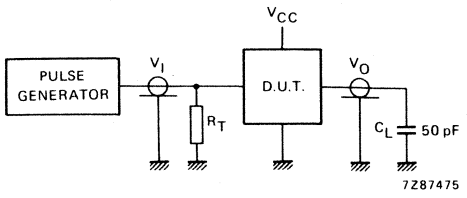


Fig. 8 Test circuit.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

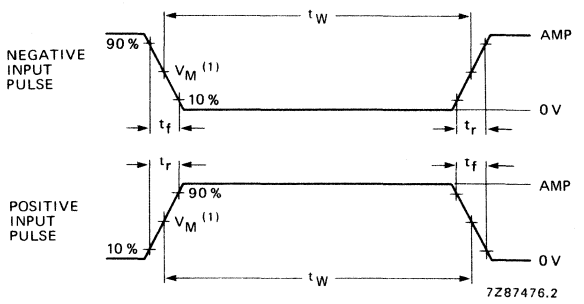


Fig. 9 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DUAL J$\overline{K}$ FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- J, $\overline{K}$ inputs for easy D-type flip-flop
- Toggle flip-flop or "do nothing" mode
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT109 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT109 are dual positive-edge triggered, J$\overline{K}$ flip-flops with individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the mode select function table.

The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The J$\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 5 V	 16 11 11	 17 14 14	 ns ns ns
f_{max}	maximum clock frequency		60	58	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT109P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT109D; PC74HC/HCT109D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT109T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{R}_D$, $2\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
5, 11	$1\overline{S}_D$, $2\overline{S}_D$	asynchronous set-direct input (active LOW)
6, 10	1Q, 2Q	true flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

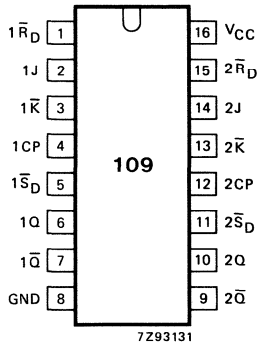


Fig. 1 Pin configuration.

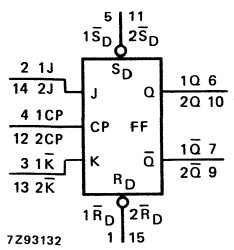


Fig. 2 Logic symbol.

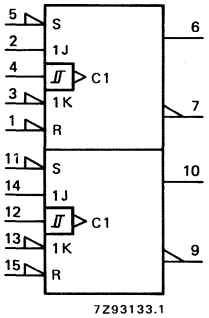


Fig. 3 IEC logic symbol.

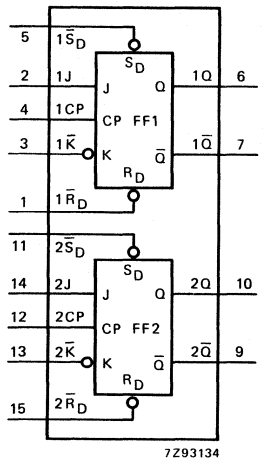


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	l	$\overline{q}$	q
load "0" (reset)	H	H	↑	l	l	L	H
load "1" (set)	H	H	↑	h	h	H	$\overline{L}$
hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

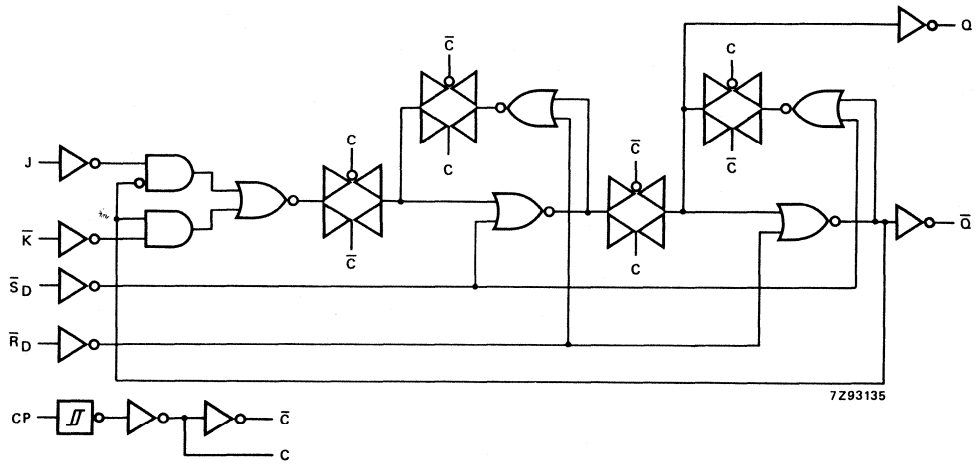


Fig. 5 Logic diagram (one flip-flop).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			4.0		40.0		80.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			4.0		40.0		80.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nJ, n$\overline{K}$	0.35
n$\overline{R}_D$	0.35
n$\overline{S}_D$	0.35
nCP	0.35

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$			190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay n$\overline{S}_D$ to nQ			110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 7
t_{PLH}	propagation delay n$\overline{S}_D$ to n$\overline{Q}$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay n$\overline{R}_D$ to nQ			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{PLH}	propagation delay n$\overline{R}_D$ to n$\overline{Q}$			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	set or reset pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time n$\overline{S}_D$, n$\overline{R}_D$ to nCP	70 14 12			90 18 15		105 21 18		ns	2.0 4.5 6.0	
t_{su}	set-up time nJ, n$\overline{K}$ to nCP	70 14 12			90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, n$\overline{K}$ to nCP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$			40		50		60	ns	4.5	Fig. 6
t_{PHL}	propagation delay n$\overline{S}_D$ to nQ			26		33		39	ns	4.5	Fig. 7
t_{PLH}	propagation delay n$\overline{S}_D$ to n$\overline{Q}$			38		48		57	ns	4.5	Fig. 7
t_{PHL}	propagation delay n$\overline{R}_D$ to nQ			40		50		60	ns	4.5	Fig. 7
t_{PLH}	propagation delay n$\overline{R}_D$ to n$\overline{Q}$			32		40		48	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	18			23		27		ns	4.5	Fig. 6
t_W	set or reset pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 7
t_{rem}	removal time n$\overline{S}_D$, n$\overline{R}_D$ to nCP	16			20		24		ns	4.5	
t_{su}	set-up time nJ, n$\overline{K}$ to nCP	18			23		27		ns	4.5	Fig. 6
t_h	hold time nJ, n$\overline{K}$ to nCP	3			3		3		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	27			22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

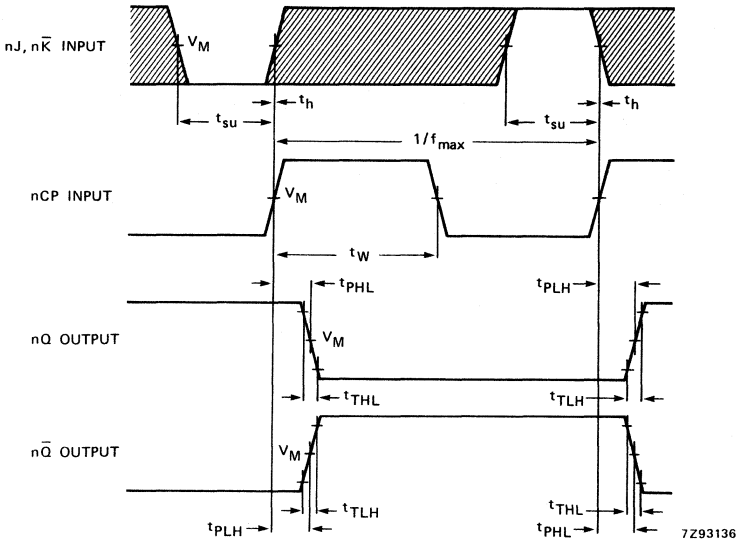


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

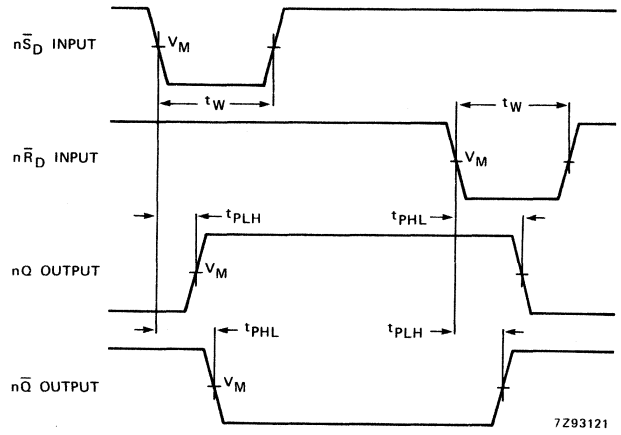


Fig. 7 Waveforms showing the set and reset input to output (nQ, nQ̄) propagation delays and the set and reset pulse width.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

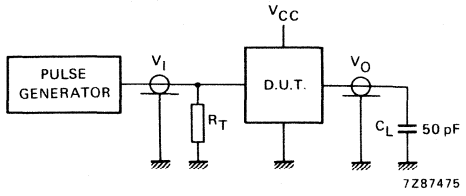


Fig. 8 Test circuit.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

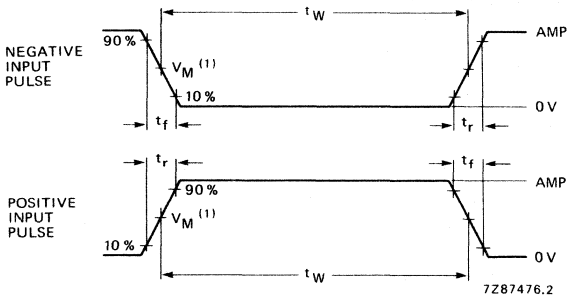


Fig. 9 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

DUAL JK FLIP-FLOP WITH SET AND RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Asynchronous set and reset
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT112 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT112 are dual negative-edge triggered JK-type flip-flops featuring individual nJ, nK, clock ($n\overline{CP}$), set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) inputs. The set and reset inputs, when LOW, set or reset the outputs as shown in the function table regardless of the levels at the other inputs.

A HIGH level at the clock ($n\overline{CP}$) input enables the nJ and nK inputs and data will be accepted. The logic levels at the nJ and nK inputs may be allowed to change while the $n\overline{CP}$ is HIGH and the flip-flop will perform according to the function table as long as minimum set-up and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $n\overline{CP}$.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT112P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT112D; PC74HC/HCT112D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT112T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge triggered)
2, 12	1K, 2K	data inputs; flip-flops 1 and 2
3, 11	1J, 2J	data inputs; flip-flops 1 and 2
4, 10	$1\overline{S}_D$, $2\overline{S}_D$	set inputs (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 7	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
14, 15	$1\overline{R}_D$, $2\overline{R}_D$	reset inputs (active LOW)
16	V_{CC}	positive supply voltage

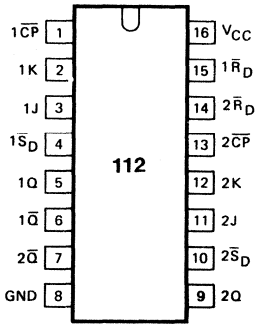


Fig. 1 Pin configuration.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	$n\overline{CP}$	nJ	nK	nQ	$n\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↓	h	h	$\overline{q}$	q
load "0" (reset)	H	H	↓	l	h	L	H
load "1" (set)	H	H	↓	h	l	H	L
hold "no change"	H	H	↓	l	l	q	$\overline{q}$

Note to function table

Both outputs will be HIGH while both $n\overline{S}_D$ and $n\overline{R}_D$ are LOW, but the output states are unpredictable if $n\overline{S}_D$ and $n\overline{R}_D$ go HIGH simultaneously.

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
X = don't care
↓ = HIGH-to-LOW CP transition

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})

GENERAL DESCRIPTION

The 54/74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown in Fig. 6.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}_D$, which also inhibits the triggering.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$ $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 5 V R_{EXT} = 5 kΩ C_{EXT} = 0 pF	26 19	26 19	ns ns
C_I	input capacitance		3.5	3.5	pF
t_W	minimum output pulse width nQ, $n\overline{Q}$		75	75	ns

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT123P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT123D; PC74HC/HCT123D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT123T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset LOW and trigger action at positive edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

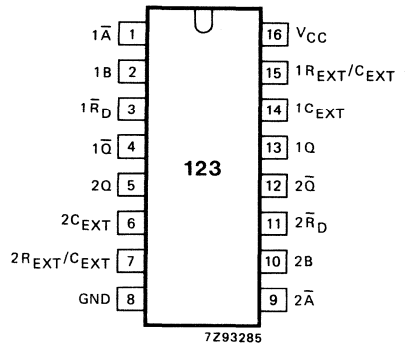


Fig. 1 Pin configuration.

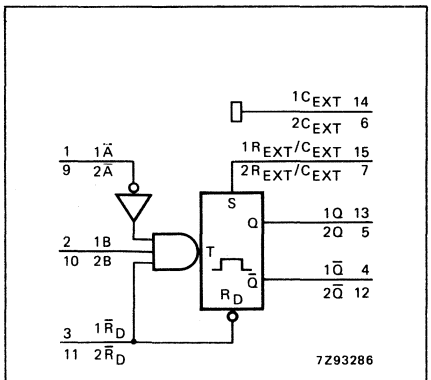


Fig. 2 Logic symbol.

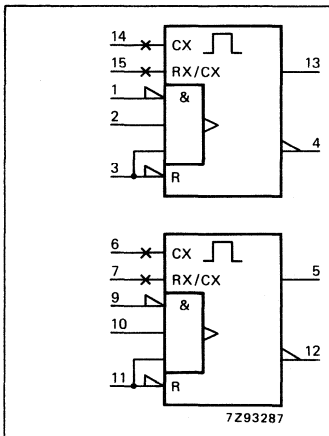


Fig. 3 IEC logic symbol.

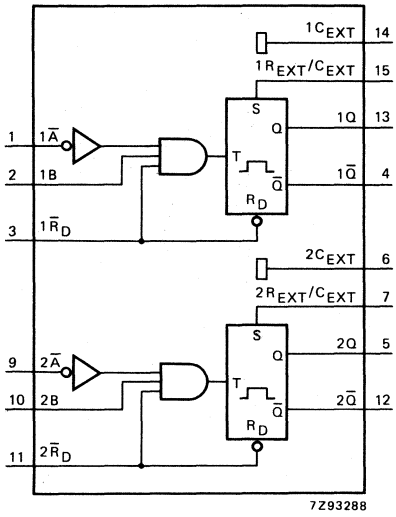


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd)

An internal connection from $n\overline{R}_D$ to the input gates makes it possible to trigger the circuit by a positive-going signal at input $n\overline{R}_D$ as shown in the function table. Figures 7 and 8 illustrate pulse control by retriggering and early reset. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}. For pulse widths, when $C_{EXT} < 10\,000$ pF, see Fig. 9.

When $C_{EXT} > 10\,000$ pF, the typical output pulse width is defined as:

$t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.),

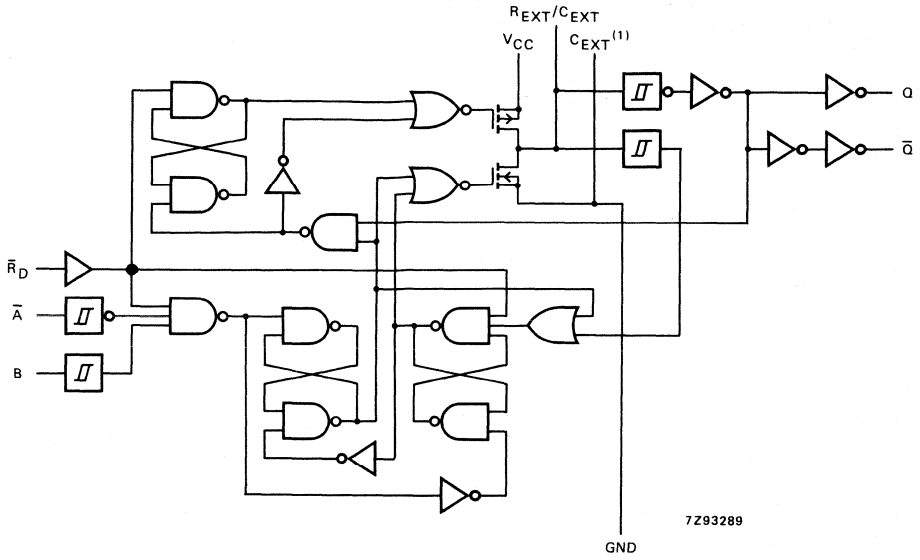
where, t_W = pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF.

Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎎ = one LOW level output pulse



(1) It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

Fig. 5 Logic diagram.

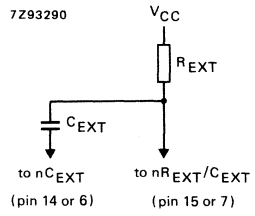


Fig. 6 Timing component connections.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$n\overline{A}$, nB	0.35
$n\overline{R}_D$	0.35

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS/NOTES
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay $n\overline{A}$, nB to $n\overline{Q}$			350 70 60		440 88 75		525 105 89	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{A}$, nB to nQ			330 66 56		415 83 71		495 99 84	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ			230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	
t_W	trigger pulse width $n\overline{A}$ = LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width nB = HIGH	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_W	output pulse width nQ, $n\overline{Q}$ = HIGH		45		–		–		μs	5.0	C_{EXT} = 10 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ, $n\overline{Q}$ = HIGH		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		50		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 8
R_{EXT}	external timing resistor	2		100	–		–		kΩ	5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 9

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS/NOTES
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay $n\overline{A}$, nB to $n\overline{Q}$			70		88		105	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{A}$, nB to nQ			66		83		99	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ			46		58		69	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$			50		63		75	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	
t_W	trigger pulse width $n\overline{A}$ = LOW	20			25		30		ns	4.5	Fig. 7
t_W	trigger pulse width nB = HIGH	20			25		30		ns	4.5	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	20			25		30		ns	4.5	Fig. 8
t_W	output pulse width nQ, $n\overline{Q}$ = HIGH		45		–		–		μs	5.0	C_{EXT} = 10 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ, $n\overline{Q}$ = HIGH		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		50		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 8
R_{EXT}	external timing resistor	2		100	–		–		kΩ	5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 9

Notes to AC characteristics

1. For other R_{EXT} and C_{EXT} combinations see Fig. 9.

   If $C_{EXT} > 10$ nF, the next formula is valid:

   $$t_W = K \times R_{EXT} \times C_{EXT} \text{ (typ.)}$$

   where, t_W = output pulse width in ns;
   R_{EXT} = external resistor in kΩ; C_{EXT} = external capacitor in pF;
   K = constant = 0.45 for V_{CC} = 5.0 V and 0.48 for V_{CC} = 2.0 V.

   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

2. The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}.

   The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

   If $C_{EXT} > 10$ nF, the next formula (at V_{CC} = 5.0 V) for the set-up time of a retrigger pulse is valid:

   $$t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT}) \text{ (typ.)}$$

   where, t_{rt} = retrigger time in ns;
   C_{EXT} = external capacitor in pF;
   R_{EXT} = external resistor in kΩ.

   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

AC WAVEFORMS

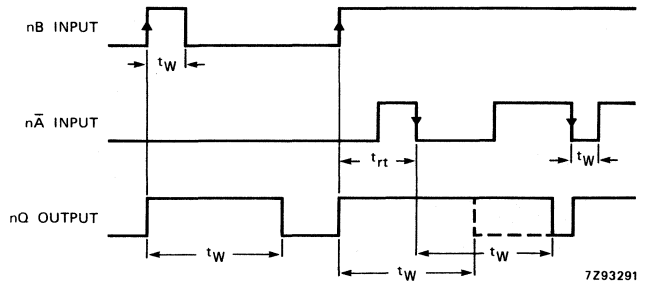


Fig. 7 Output pulse control using retrigger pulse; $n\overline{R}_D$ = HIGH.

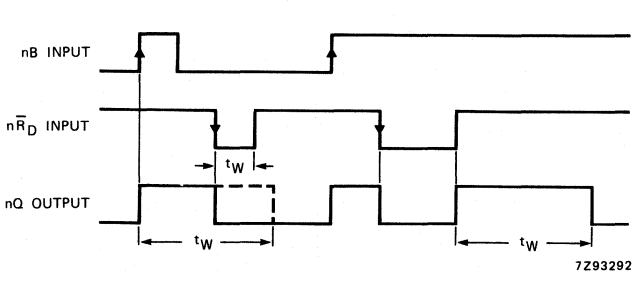


Fig. 8 Output pulse control using reset input $n\overline{R}_D$; $n\overline{A}$ = LOW.

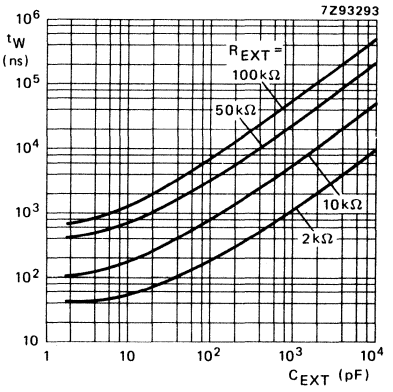


Fig. 9 Typical output pulse width as a function of the external capacitor values at V_{CC} = 5.0 V and T_{amb} = 25 °C.

TEST CIRCUIT AND WAVEFORMS

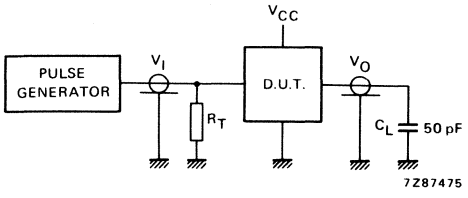


Fig. 10 Test circuit.

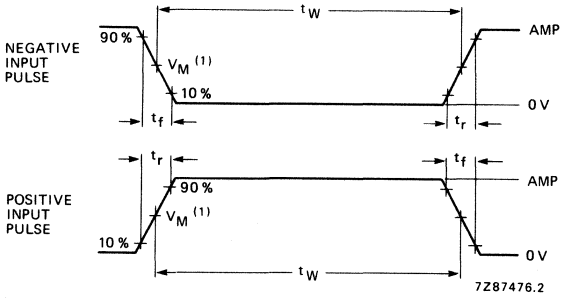


Fig. 11 Input pulse definitions.

Definitions for Figs 10 and 11:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT125P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT125D; PC74HC/HCT125D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT125T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

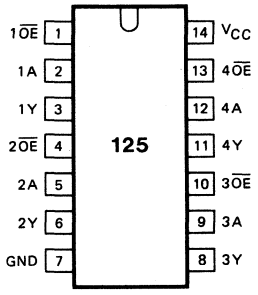


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT126 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT126 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "126" is identical to the "125" but has active HIGH enable inputs.

FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT126P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT126D; PC74HC/HCT126D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT126T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1OE to 4OE	output enable inputs (active HIGH)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

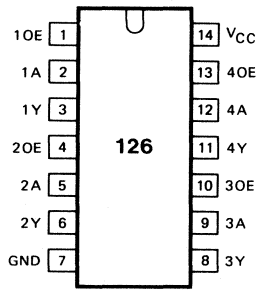


Fig. 1 Pin configuration.

QUAD 2-INPUT NAND SCHMITT TRIGGER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT132 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	10	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	24	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT132P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT132D; PC74HC/HCT132D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT132T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

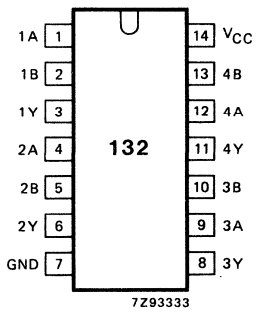


Fig. 1 Pin configuration.

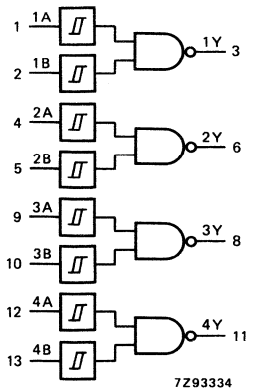


Fig. 2 Logic symbol.

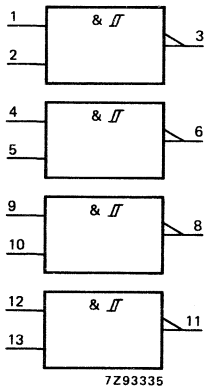


Fig. 3 IEC logic symbol.

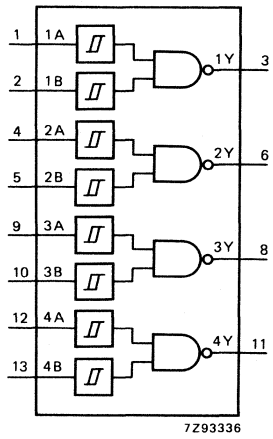


Fig. 4 Functional diagram.

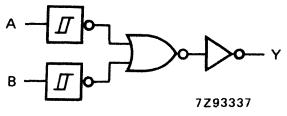


Fig. 5 Logic diagram (one Schmitt trigger).

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB	0,3

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	OTHERS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going treshold	0.7 1.7 2.1		1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V	2.0 4.5 6.0	
V_{T-}	negative-going treshold	0.3 0.9 1.2		1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	V	2.0 4.5 6.0	
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.6		1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	OTHERS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going treshold	1.2 1.4		1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V	4.5 5.5	
V_{T-}	negative-going treshold	0.5 0.6		1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5	
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.4 0.4		– –	0.4 0.4	– –	0.4 0.4	– –	V	4.5 5.5	

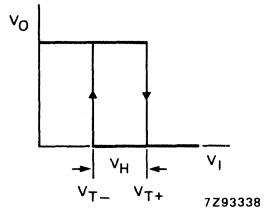


Fig. 6 Transfer characteristic.

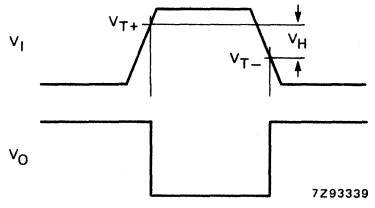


Fig. 7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			30		38		45	ns	4.5	Fig. 8
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 8

DEVELOPMENT DATA

AC WAVEFORMS

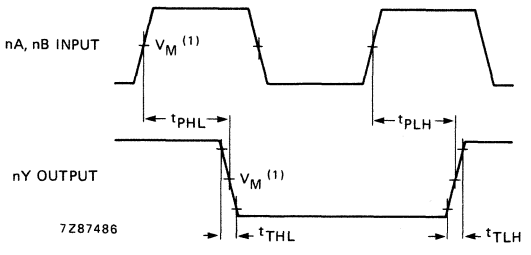


Fig. 8 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

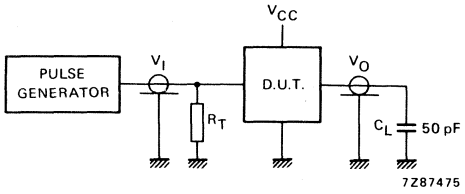


Fig. 9 Test circuit.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

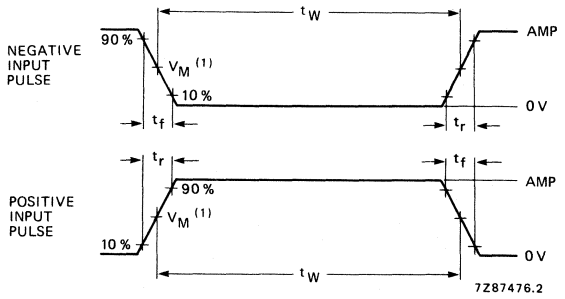


Fig. 10 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

1-TO-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

FEATURES

- **Combines 1-of-8 decoder with 3-bit latch**
- **Multiple input enable for easy expansion or independent controls**
- **Active LOW mutually exclusive outputs**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT137 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT137 are 1-of-8 decoder/demultiplexers with latches at the three address inputs (A_n). The "137" essentially combines the 1-of-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the "137" acts as a 1-of-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs, before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable input ($\overline{E}_1$ and E_2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E}_1$ is LOW and E_2 is HIGH.

The "137" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

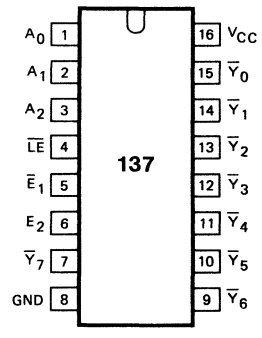


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT137P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT137D; PC74HC/HCT137D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT137T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	data inputs
4	$\overline{LE}$	latch enable input (active LOW)
5	$\overline{E}_1$	data enable input (active LOW)
6	E_2	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	multiplexer outputs
16	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E_2	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

3-TO-8 LINE DECODER/DEMULTIPLEXER; INVERTING

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT138 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).
The "138" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "138" to a 1-of-32 (5 lines to 32 lines) decoder with just four "138" ICs and one inverter.

The "138" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	12	14	ns
t_{PHL}/t_{PLH}	E_3 to $\overline{Y}_n$; $\overline{E}_n$ to $\overline{Y}_n$		14	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	67	67	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT138P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT138D; PC74HC/HCT138D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT138T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

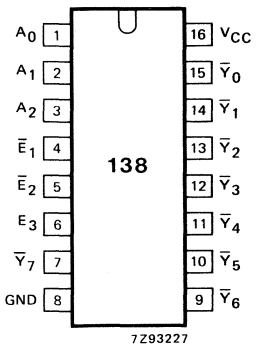


Fig. 1 Pin configuration.

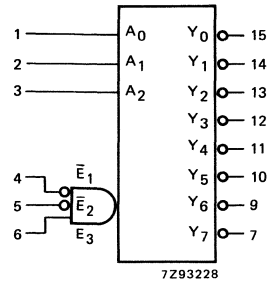


Fig. 2 Logic symbol.

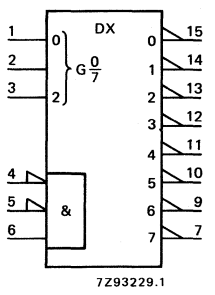


Fig. 3 IEC logic symbol.

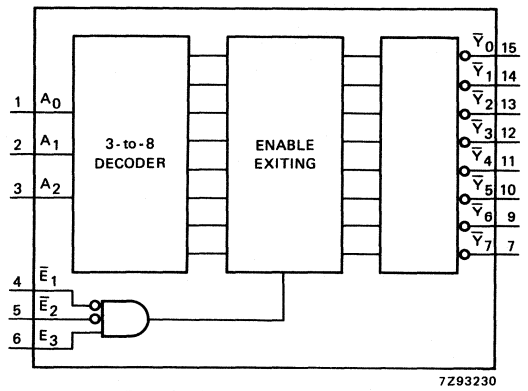


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

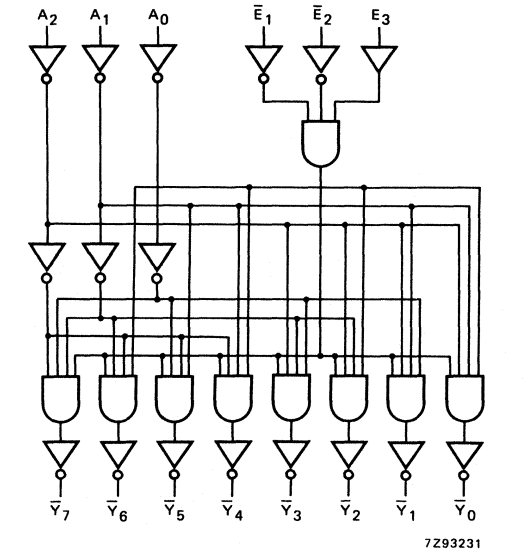


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
A_n	0.70
$\overline{E}_n$	0.40
E_3	1.50

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay E_3 to $\overline{Y}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$			35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay E_3 to $\overline{Y}_n$			40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$			40		50		60	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

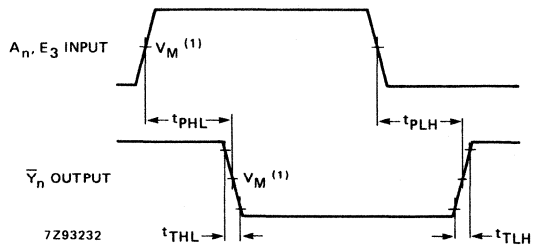


Fig. 6 Waveforms showing the address input (A_n) and enable input (E_3) to output ($\overline{Y}_n$) propagation delays and the output transition times.

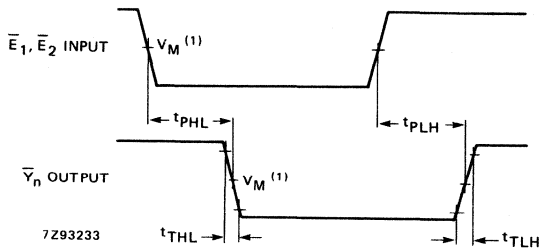


Fig. 7 Waveforms showing the enable input ($\overline{E}_n$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

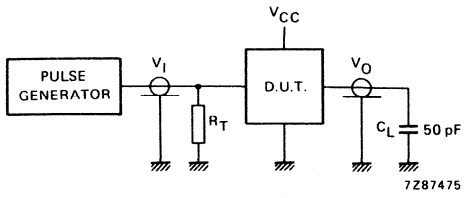


Fig. 8 Test circuit.

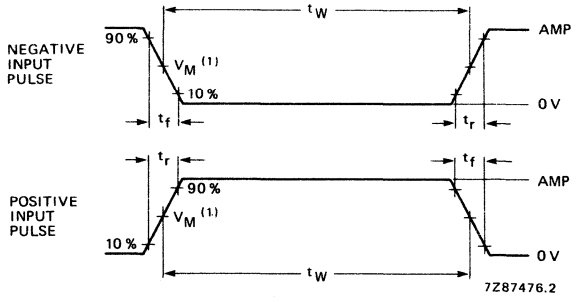


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER

FEATURES

- **Demultiplexing capability**
- **Two independent 2-to-4 decoders**
- **Multifunction capability**
- **Active LOW mutually exclusive outputs**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT139 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT139 are high-speed, dual 2-to-4 line decoder/demultiplexers. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_4$). Each decoder has an active LOW enable input ($n\overline{E}$).

When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

The "139" is identical to the HEF4556 of the HE4000B family.

APPLICATIONS

- **Memory decoding or data-routing**
- **Code conversion**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA_n to $n\overline{Y}_n$ $n\overline{E}$ to $n\overline{Y}_n$	C_L = 15 pF V_{CC} = 5 V	11 9	14 14	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	42	44	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT139P: 16-lead DIL; plastic (SOT-38).
PC54HC/HCT139D; PC74HC/HCT139D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT139T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	outputs (active LOW)
14, 13	$2A_0$, $2A_1$	address inputs
16	V_{CC}	positive supply voltage

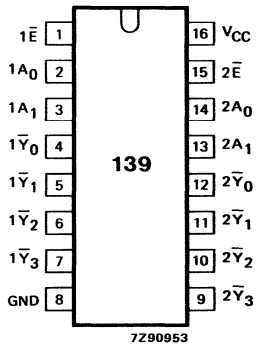


Fig. 1 Pin configuration.

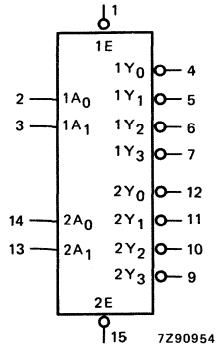


Fig. 2 Logic symbol.

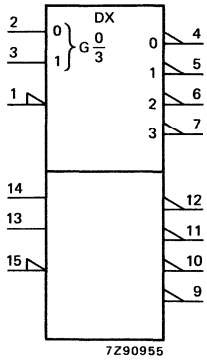


Fig. 3 IEC logic symbol.

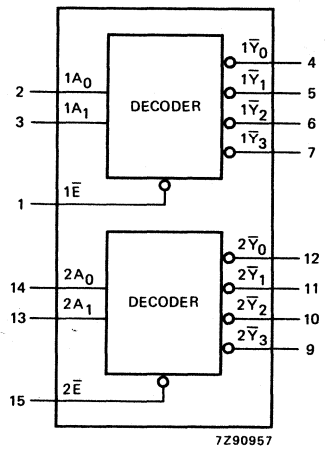


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\bar{E}$	nA_0	nA_1	$n\bar{Y}_0$	$n\bar{Y}_1$	$n\bar{Y}_2$	$n\bar{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

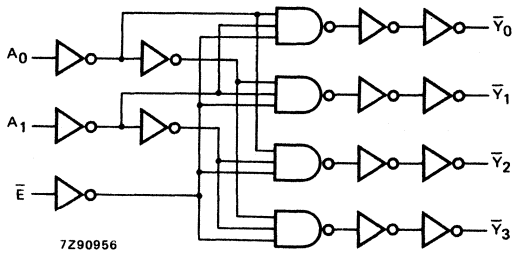


Fig. 5 Logic diagram (one decoder/demultiplexer).

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$1A_n$	0.70
$2A_n$	0.70
$n\overline{E}$	0.70

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA_n to $\overline{Y}_n$			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{E}$ to $n\overline{Y}_n$			120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA_n to $\overline{Y}_n$			34		43		51	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{E}$ to $n\overline{Y}_n$			34		43		51	ns	4.5	Fig. 7
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

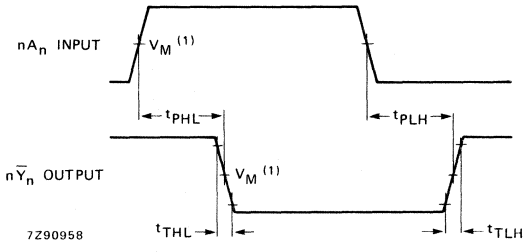


Fig. 6 Waveforms showing the address input (nA_n) to output ($n\overline{Y}_n$) propagation delays and the output transition times.

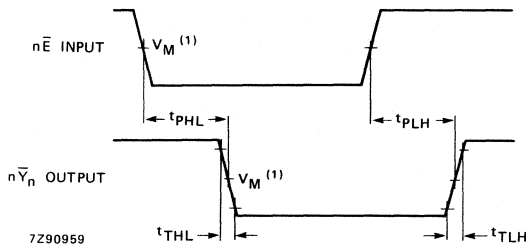


Fig. 7 Waveforms showing the enable input ($n\overline{E}$) to output ($n\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

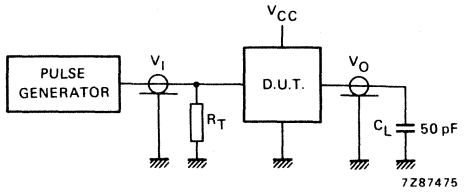


Fig. 8 Test circuit.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

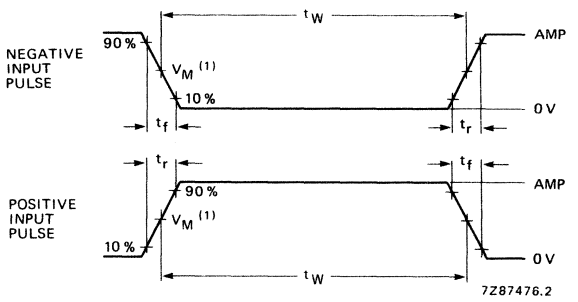


Fig. 9 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

10-TO-4 LINE PRIORITY ENCODER

FEATURES

- Encodes 10-line decimal to 4-line BCD
- Useful for 10-position switch encoding
- Used in code converters and generators
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT147 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT147 9-input priority encoders accept data from nine active LOW inputs ($\overline{A}_0$ to $\overline{A}_8$) and provide a binary representation on the four active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_3$). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{A}_8$ having the highest priority.

The devices provide the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	15	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	30	33	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT147P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT147D; PC74HC/HCT147D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT147T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 14	$\overline{Y}_0$ to $\overline{Y}_3$	BCD address outputs (active LOW)
11, 12, 13, 1, 2, 3, 4, 5, 10	$\overline{A}_0$ to $\overline{A}_8$	decimal data inputs (active LOW)
15	n.c.	not connected
16	V_{CC}	positive supply voltage

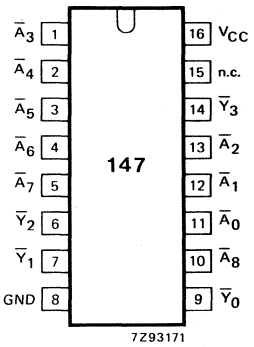


Fig. 1 Pin configuration.

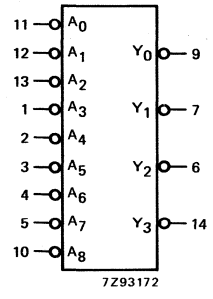


Fig. 2 Logic symbol.

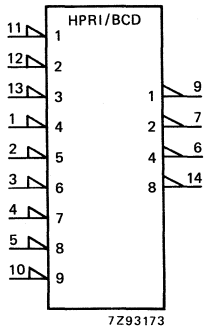


Fig. 3 IEC logic symbol.

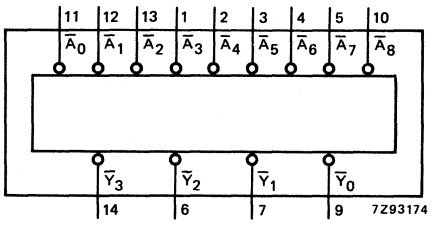


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS									OUTPUTS			
$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	$\overline{A}_8$	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

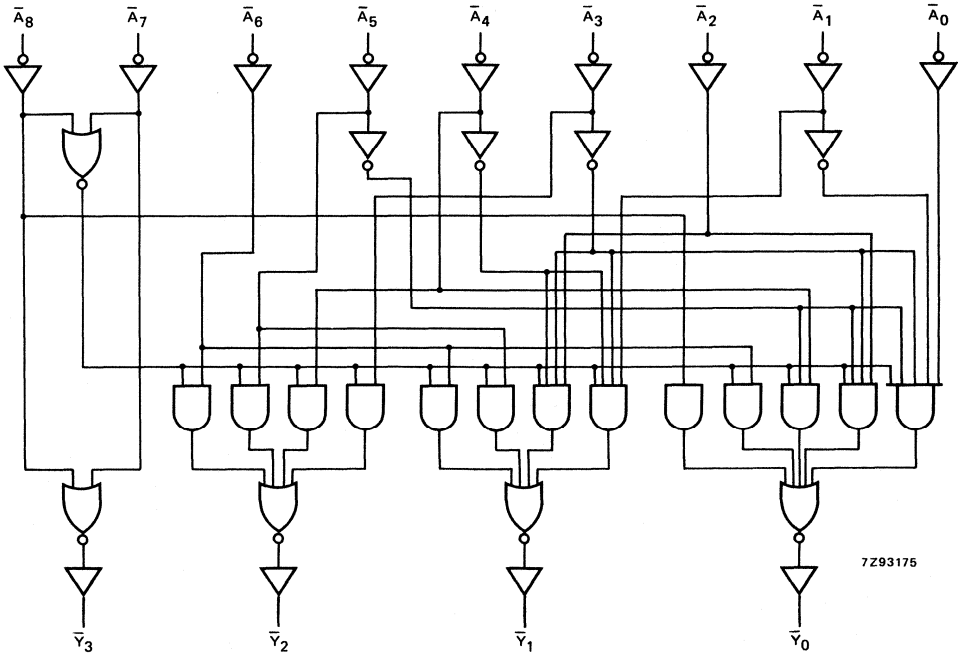


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$\overline{A}_3$, $\overline{A}_4$, $\overline{A}_7$, $\overline{A}_8$	1.50
$\overline{A}_5$, $\overline{A}_6$, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$	1.10

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{Y}_n$			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 6		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{Y}_n$			40		50		60	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

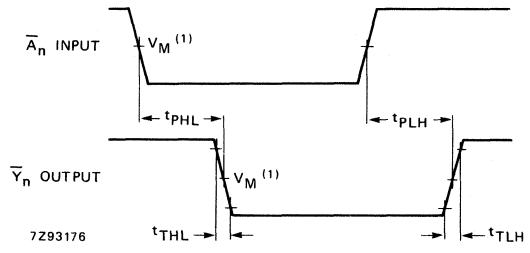


Fig. 6 Waveforms showing the decimal data inputs ($\overline{A}_n$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

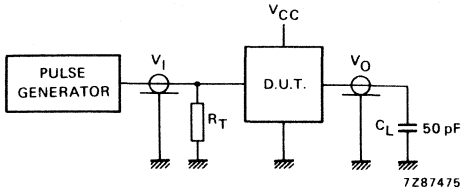


Fig. 7 Test circuit.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

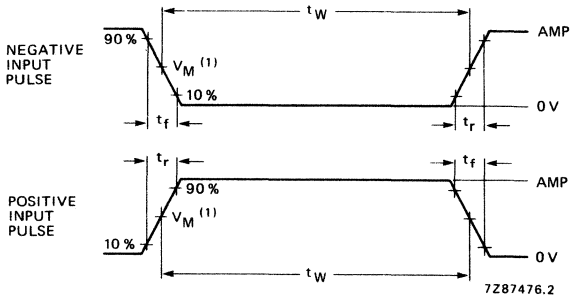


Fig. 8 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

8-INPUT MULTIPLEXER

FEATURES

- **True and complement outputs**
- **Multifunction capability**
- **Permits multiplexing from n lines to 1 line**
- **Non-inverting data path**
- **See the "251" for the 3-state version**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT151 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT151 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S_0, S_1, S_2) controlling the switch positions.
Assertion (Y) and negation ($\overline{Y}$) outputs are both provided.
The enable input ($\overline{E}$) is active LOW.
When $\overline{E}$ is HIGH, the $\overline{Y}$ output is HIGH and the Y output is LOW, regardless of all inputs.
The logic function provided at the output, when activated, is:

$$Y = \overline{E}.(I_0.\overline{S}_0.\overline{S}_1.\overline{S}_2 + I_1.S_0.\overline{S}_1.\overline{S}_2 + I_2.\overline{S}_0.S_1.\overline{S}_2 + I_3.S_0.S_1.\overline{S}_2 + I_4.\overline{S}_0.\overline{S}_1.S_2 + I_5.S_0.\overline{S}_1.S_2 + I_6.\overline{S}_0.S_1.S_2 + I_7.S_0.S_1.S_2)$$

The "151" provides in one package the ability to select from eight sources of data or control information. The "151" can provide any logic function of four variables and its negation with correct manipulations.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to Y, $\overline{Y}$ S_n to Y, $\overline{Y}$ $\overline{E}$ to Y $\overline{E}$ to $\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	 16 17 11 13	 17 19 12 16	 ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT151P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT151D; PC74HC/HCT151D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT151T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	$\overline{Y}$	complementary multiplexer output
7	$\overline{E}$	enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage

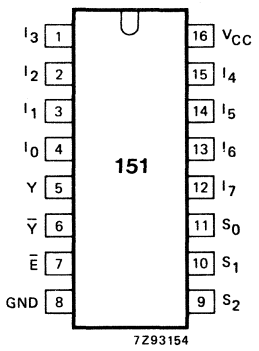


Fig. 1 Pin configuration.

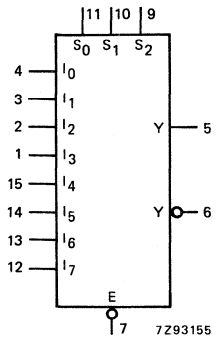


Fig. 2 Logic symbol.

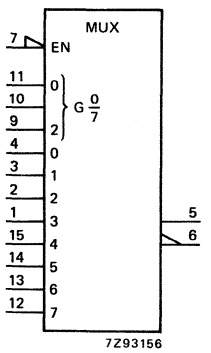


Fig. 3 IEC logic symbol.

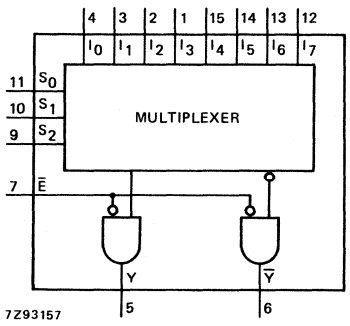


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS												OUTPUTS	
$\bar{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\bar{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

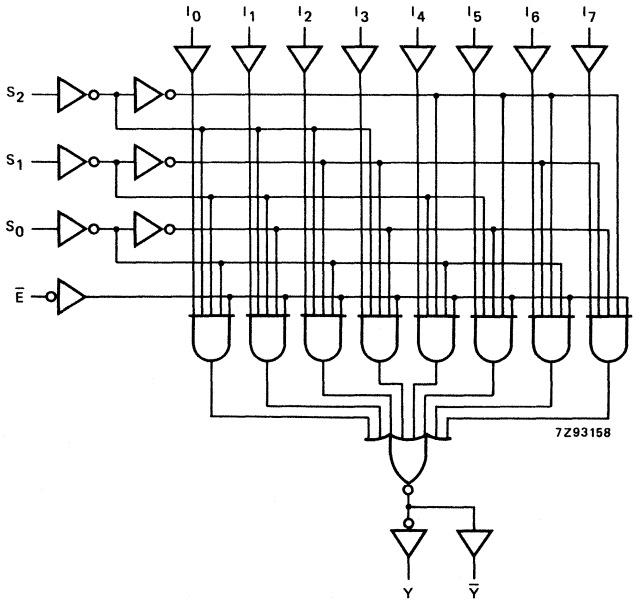


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
I_n	0.45
S_n	1.50
$\overline{E}$	0.30

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Y			190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to $\overline{Y}$			185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to Y			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_n to $\overline{Y}$			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to Y			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{Y}$			155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Y			40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to $\overline{Y}$			40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to Y			41		51		62	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_n to $\overline{Y}$			46		58		69	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to Y			29		36		44	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{Y}$			38		48		57	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

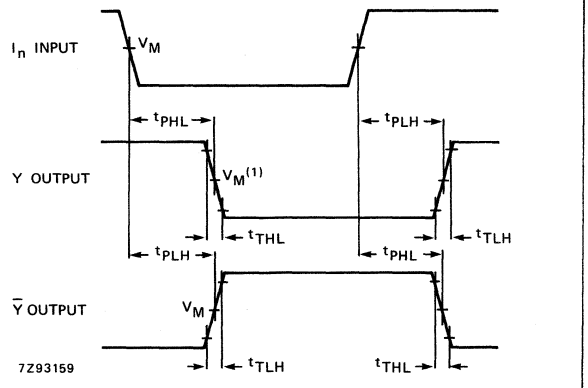


Fig. 6 Waveforms showing the multiplexer input (I_n) to outputs (Y and $\overline{Y}$) propagation delays and the output transition times.

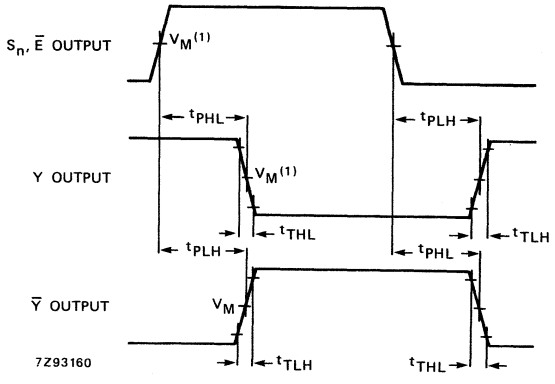


Fig. 7 Waveforms showing the select input (S_n) and enable input ($\overline{E}$) to outputs (Y and $\overline{Y}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

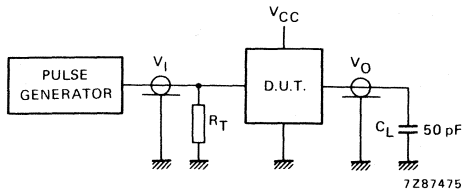


Fig. 8 Test circuit.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

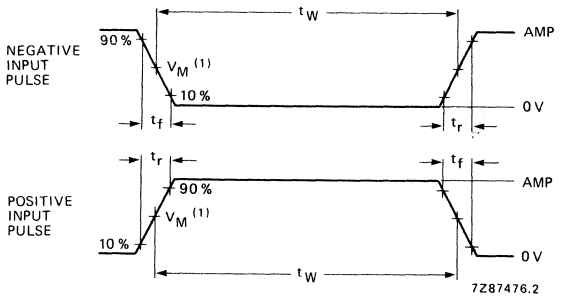


Fig. 9 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DUAL 4-INPUT MULTIPLEXER

FEATURES

- Non-inverting outputs
- Separate enable for each output
- Common select inputs
- See '253" for 3-state version
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT153 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT153 have two identical 4-input multiplexers which select two bits of data from up to four sources selected by common data select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW output enable inputs ($1\overline{E}$, $2\overline{E}$) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH.

The "153" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S_0 and S_1.

The logic equations for the outputs are:

$$1Y = 1\overline{E}.(1I_0.\overline{S}_1.\overline{S}_0 + 1I_1.\overline{S}_1.S_0 + 1I_2.S_1.\overline{S}_0 + 1I_3.S_1.S_0)$$

$$2Y = 2\overline{E}.(2I_0.\overline{S}_1.\overline{S}_0 + 2I_1.\overline{S}_1.S_0 + 2I_2.S_1.\overline{S}_0 + 2I_3.S_1.S_0)$$

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1I_n$, $2I_n$ to nY S_n to nY $n\overline{E}$ to nY	C_L = 15 pF V_{CC} = 5 V	12 14 9	13 13 9	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT153P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT153D; PC74HC/HCT153D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT153T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
7	1Y	multiplexer output from source 1
8	GND	ground (0 V)
9	2Y	multiplexer output from source 2
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage

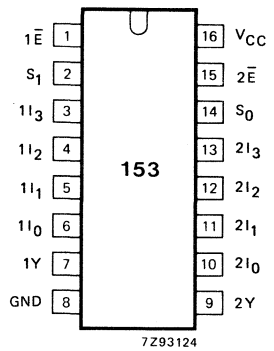


Fig. 1 Pin configuration.

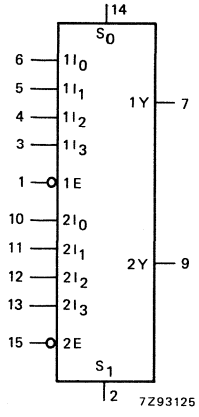


Fig. 2 Logic symbol.

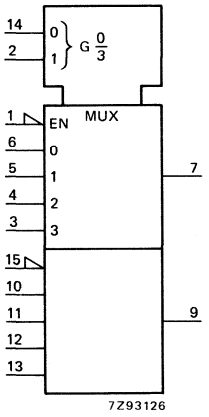


Fig. 3 IEC logic symbol.

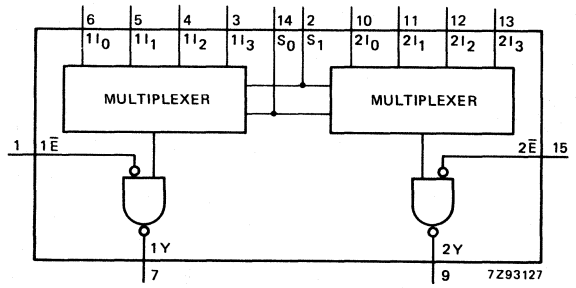


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (cont.'ed)

The "153" can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	nI_0	nI_1	nI_2	nI_3	$n\bar{E}$	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

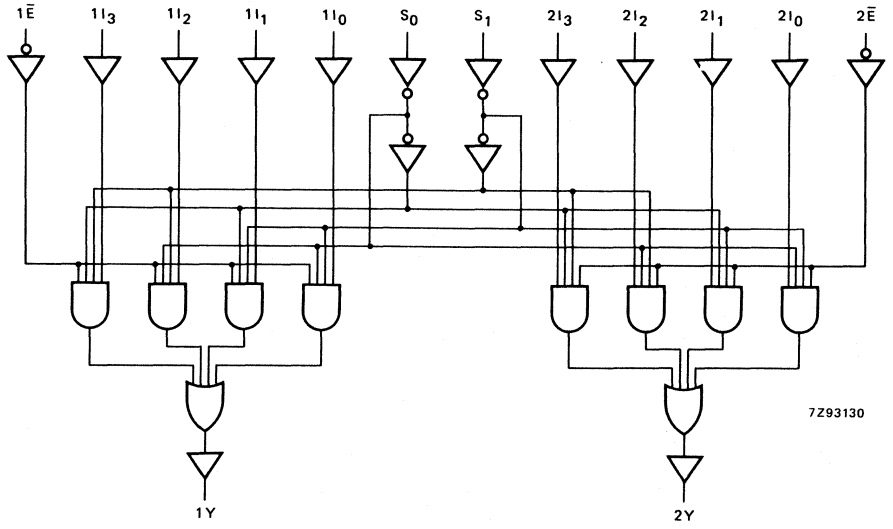


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		500	mW	for standard temperature range; −40 to +85 °C; 74HC/HCT above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		500	mW	for extended temperature range; −55 to +125°C; 54HC/HCT above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$1I_n$, $2I_n$	0.45
$\overline{nE}$	0.60
S_n	1.35

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY			145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to nY			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $n\overline{E}$ to nY			110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay $1I_n$ to nY; $2I_n$ to nY			33		41		50	ns	4.5	Fig. 6
t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY			26		33		39	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to nY			33		41		50	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $n\overline{E}$ to nY			24		30		36	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

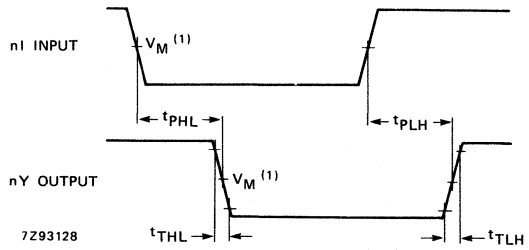


Fig. 6 Waveforms showing the input ($1I_n$, $2I_n$) to output (1Y, 2Y) propagation delays and the output transition times.

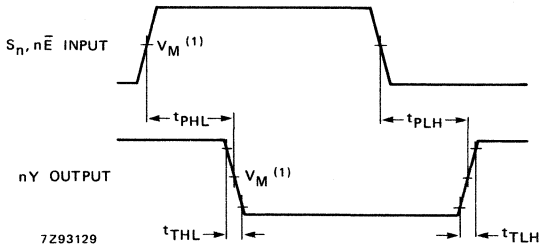


Fig. 7 Waveforms showing the select input (S_0, S_1) and the output enable input ($\bar{E}$) to output (1Y, 2Y) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

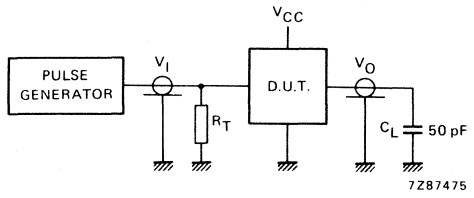


Fig. 8 Test circuit.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

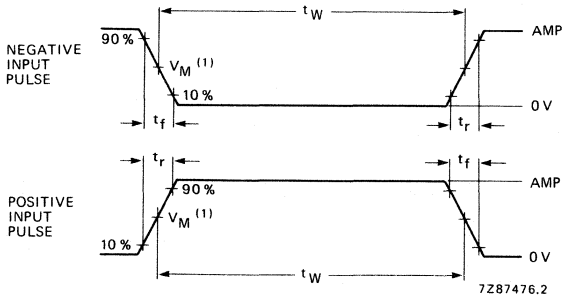


Fig. 9 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

4-TO-16 LINE DECODER/DEMULTIPLEXER

FEATURES

- **16-line demultiplexing capability**
- **Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs.

The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for the expansion of the decoder.

The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The "154" can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable is LOW, the addressed output will follow the state of the applied data.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n, $\overline{E}_n$ to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	12	14	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	60	60	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT154P: 24-lead DIL; plastic (SOT-101A).
PC54HC/HCT154D; PC74HC/HCT154D: 24-lead DIL; ceramic (cerdip) (SOT-94).
PC74HC/HCT154T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	$\overline{Y}_0$ to $\overline{Y}_{15}$	outputs (active LOW)
18, 19	$\overline{E}_0$, $\overline{E}_1$	enable inputs (active LOW)
12	GND	ground (0 V)
23, 22, 21, 20	A_0 to A_3	address inputs
24	V_{CC}	positive supply voltage

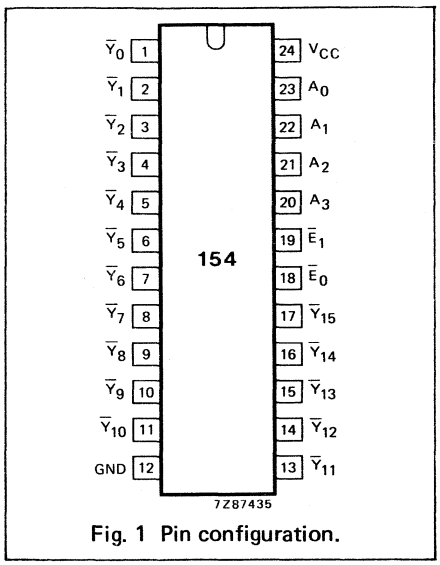


Fig. 1 Pin configuration.

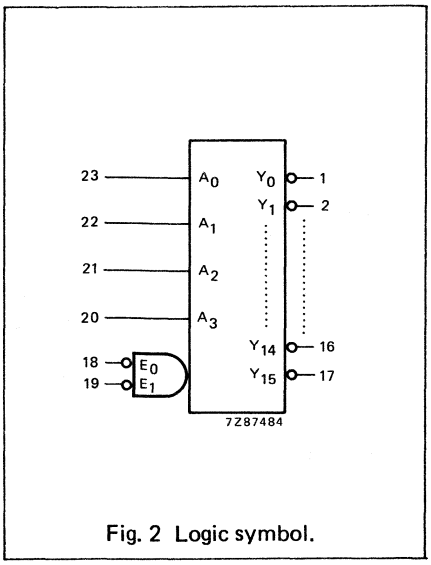


Fig. 2 Logic symbol.

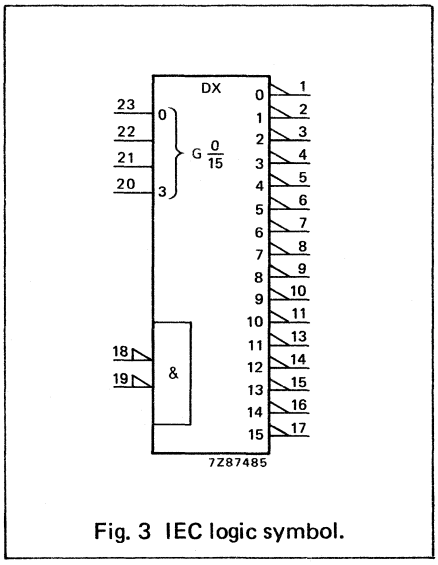


Fig. 3 IEC logic symbol.

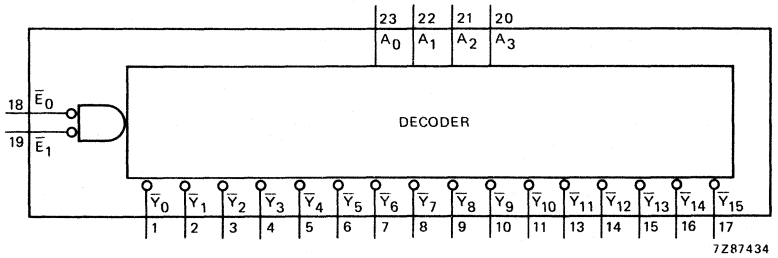


Fig. 4 Functional diagram.

FUNCTION TABLE

		INPUTS				OUTPUTS														
$\bar{E}_0$	$\bar{E}_1$	A_0	A_1	A_2	A_3	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$	$\bar{Y}_8$	$\bar{Y}_9$	$\bar{Y}_{10}$	$\bar{Y}_{11}$	$\bar{Y}_{12}$	$\bar{Y}_{13}$	$\bar{Y}_{14}$	$\bar{Y}_{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level L = LOW voltage level X = don't care

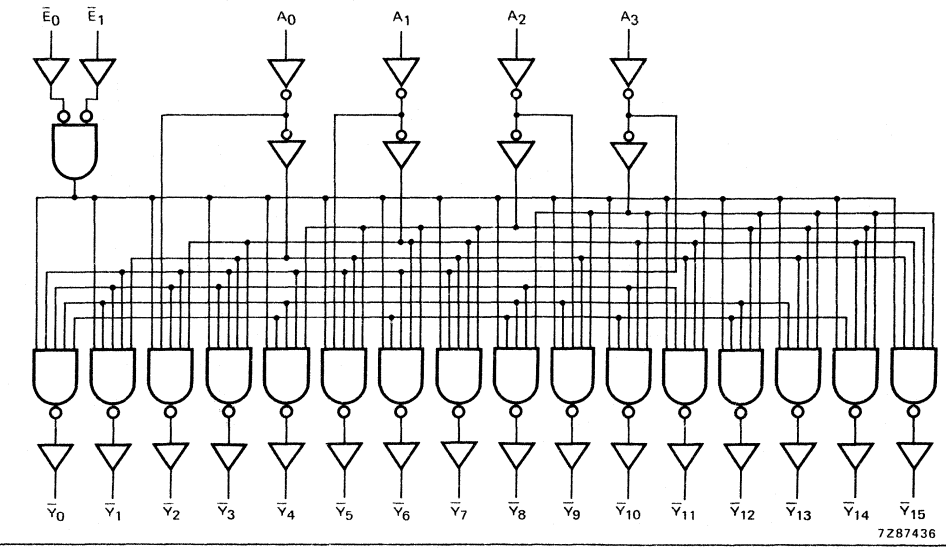


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
A_n	1.0
$\overline{E}_n$	1.0

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 6		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$			35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$			35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

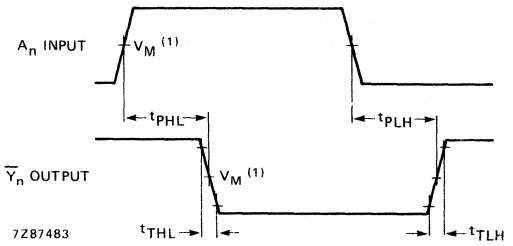


Fig. 6 Waveforms showing the address input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.

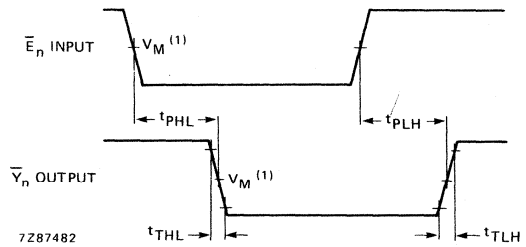


Fig. 7 Waveforms showing the enable input ($\overline{E}_n$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

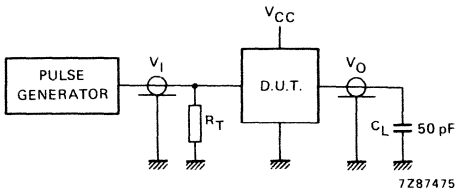


Fig. 8 Test circuit.

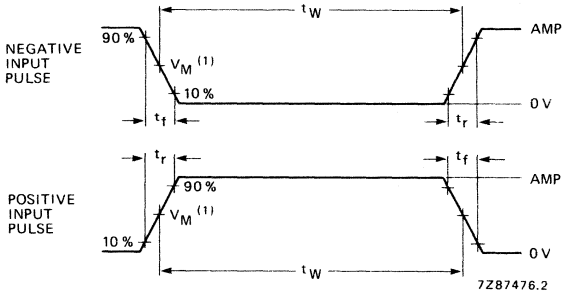


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

QUAD 2-INPUT MULTIPLEXER

FEATURES

- **Non-inverting data path**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT157 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT157 are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "157". The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is usefull for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "157" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

$1Y = \overline{E}.(1I_1.S + 1I_0.\overline{S})$

$2Y = \overline{E}.(2I_1.S + 2I_0.\overline{S})$

$3Y = \overline{E}.(3I_1.S + 3I_0.\overline{S})$

$4Y = \overline{E}.(4I_1.S + 4I_0.\overline{S})$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY $\overline{E}$ to nY S to nY	C_L = 15 pF V_{CC} = 5 V	11 11 13	13 12 17	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	76	70	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT157P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT157D; PC74HC/HCT157D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT157T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	multiplexer outputs
8	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	positive supply voltage

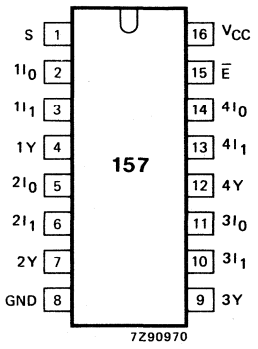


Fig. 1 Pin configuration.

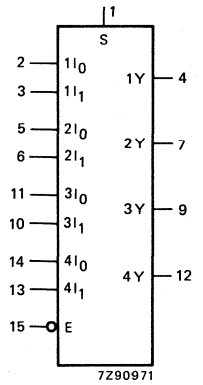


Fig. 2 Logic symbol.

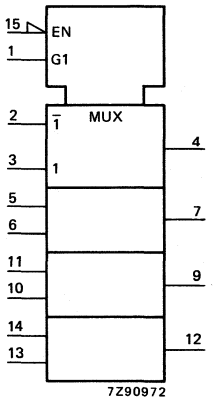


Fig. 3 IEC logic symbol.

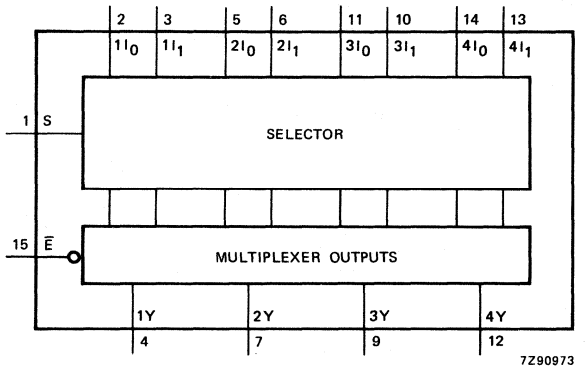


Fig. 4 Functional diagram.

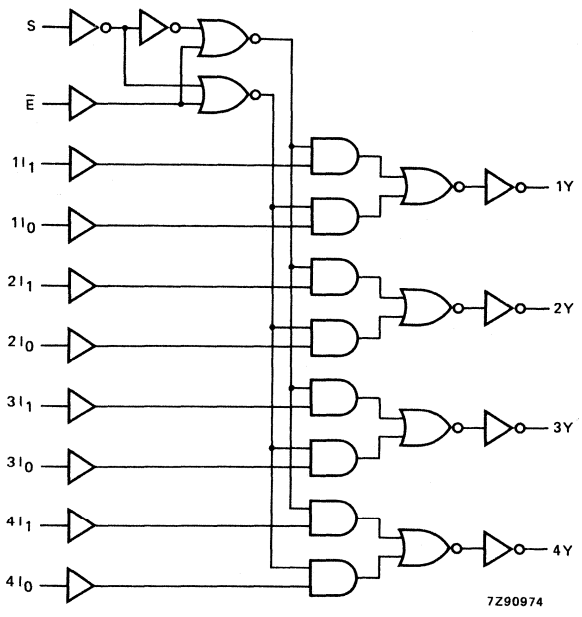


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		500	mW	for standard temperature range; −40 to +85 °C; 74HC/HCT above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		500	mW	for extended temperature range; −55 to +125°C; 54HC/HCT above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nI_0	1.00
nI_1	1.00
$\overline{E}$	0.60
S	3.00

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to nY			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to nY			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY			32		40		48	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to nY			30		38		45	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to nY			40		50		60	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

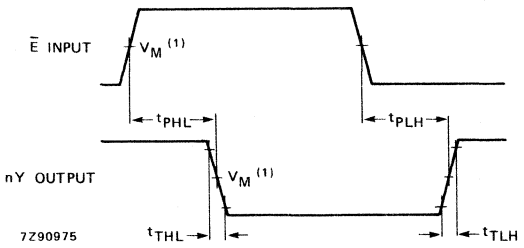


Fig. 6 Waveforms showing the enable input ($\overline{E}$) to output (nY) propagation delays and the output transition times.

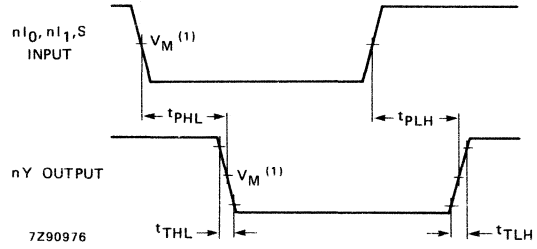


Fig. 7 Waveforms showing the data inputs (nI_n) and common data select input (S) to output (nY) propagation delays.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

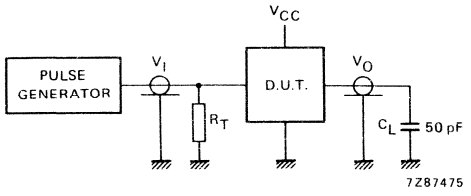


Fig. 8 Test circuit.

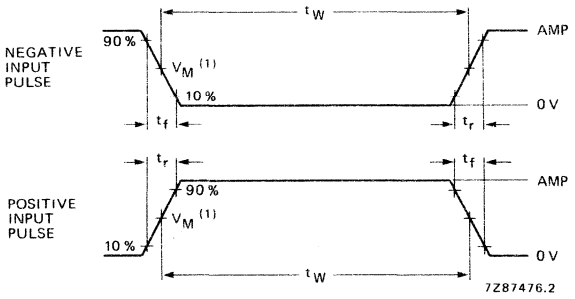


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD 2-INPUT MULTIPLEXER; INVERTING

FEATURES

- Inverting data path
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT158 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT158 are quad 2-input multiplexers which select 4 bits of data from two sources and are controlled by a common data select input (S). The four outputs present the selected data in the inverted form. The enable input ($\overline{E}$) is active LOW.

When $\overline{E}$ is HIGH, all the outputs ($1\overline{Y}$ to $4\overline{Y}$) are forced HIGH regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "158". The state of S determines the particular register from which the data comes. It can also be used as a function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "158" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations for the output are:

$1\overline{Y} = \overline{E}.(1I_1.S + 1I_0.\overline{S})$

$2\overline{Y} = \overline{E}.(2I_1.S + 2I_0.\overline{S})$

$3\overline{Y} = \overline{E}.(3I_1.S + 3I_0.\overline{S})$

$4\overline{Y} = \overline{E}.(4I_1.S + 4I_0.\overline{S})$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$ $\overline{E}$ to $n\overline{Y}$ S to $n\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	12 14 14	13 15 16	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT158P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT158D; PC74HC/HCT158D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT158T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	$1\overline{Y}$ to $4\overline{Y}$	multiplexer outputs
8	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	positive supply voltage

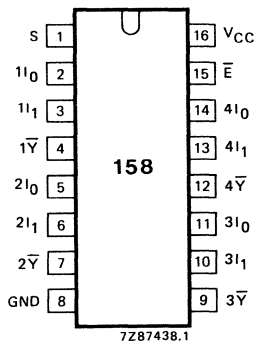


Fig. 1 Pin configuration.

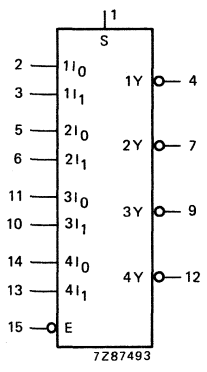


Fig. 2 Logic symbol.

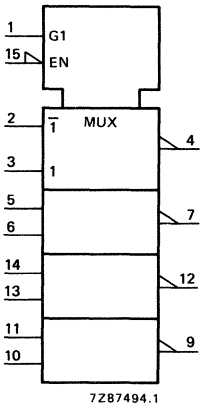


Fig. 3 IEC logic symbol.

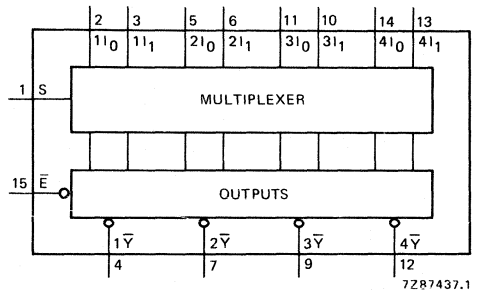


Fig. 4 Functional diagram.

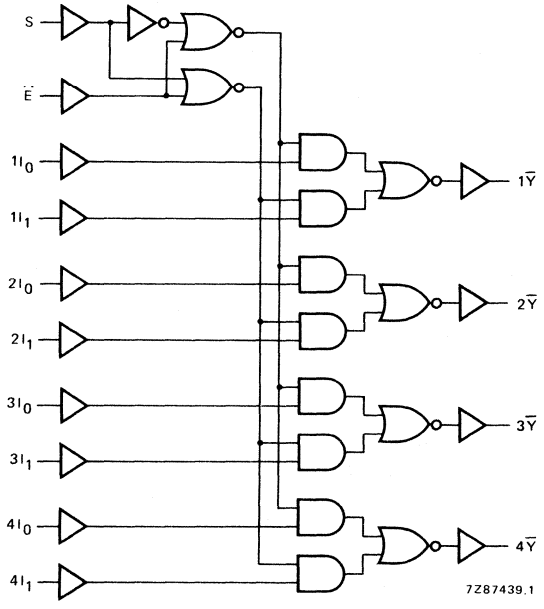


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{E}$	S	nI_0	nI_1	$n\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nI_0	0.40
nI_1	0.40
S	2.20
$\overline{E}$	0.60

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $n\overline{Y}$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to $n\overline{Y}$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$			32		40		48	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $n\overline{Y}$			37		46		56	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to $n\overline{Y}$			38		48		57	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

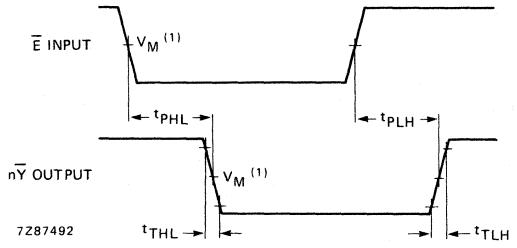


Fig. 6 Waveforms showing the enable input ($\overline{E}$) to output ($n\overline{Y}$) propagation delays and the output transition times.

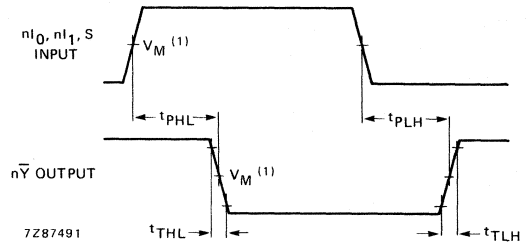


Fig. 7 Waveforms showing the data input (nI_0, nI_1) to output ($n\overline{Y}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

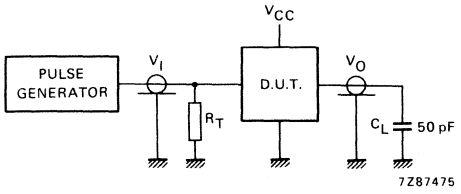


Fig. 8 Test circuit.

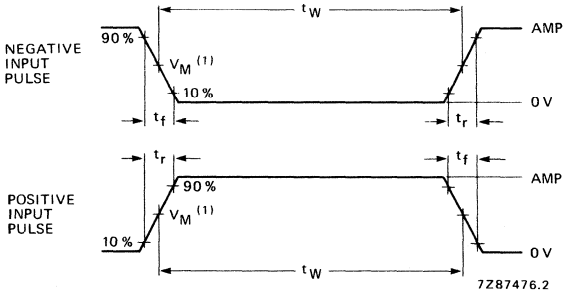


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; ASYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT160 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT160 are synchronous presettable decade counters which feature an internal carry look-ahead and can be used for high-speed counting.
Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW levels regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The carry look-ahead simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

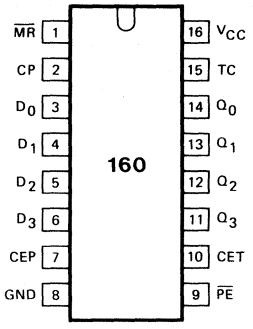


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT160P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT160D; PC74HC/HCT160D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT160T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H	X	l	X	h	X	q_n	*
	H	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; ASYNCHRONOUS RESET

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive-edge triggered clock**
- **Asynchronous reset**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT161 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT161 are synchronous presettable binary counters which feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW levels regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The carry look-ahead simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

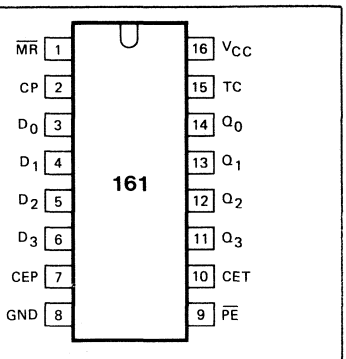


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT161P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT161D; PC74HC/HCT161D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT161T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H	X	l	X	h	X	q_n	*
	H	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; SYNCHRONOUS RESET

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive-edge triggered clock**
- **Synchronous reset**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT162 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT162 are synchronous presettable decade counters which feature an internal carry look-ahead and can be used for high-speed counting.
Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "162" the clear function is synchronous.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT162P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT162D; PC74HC/HCT162D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT162T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW levels after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.
This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The carry look-ahead simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

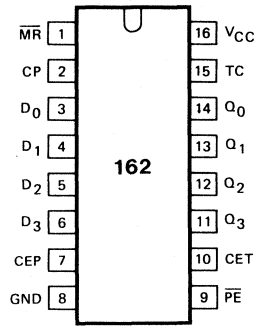


Fig. 1 Pin configuration.

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L *
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h h	X X	l X	X l	h h	X X	q_n q_n	* L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; SYNCHRONOUS RESET

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive-edge triggered clock**
- **Synchronous reset**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT163 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT163 are synchronous presettable binary counters which feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "163" the clear function is synchronous.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT163P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT163D; PC74HC/HCT163D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT163T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

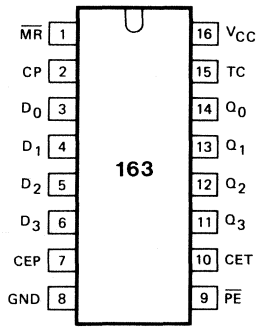


Fig. 1 Pin configuration.

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW levels after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.
This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The carry look-ahead simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L *
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h h	X X	l X	X l	h h	X X	q_n q_n	* L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

DEVELOPMENT DATA

8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

- Gated serial data inputs
- Asynchronous master reset
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT164 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages.

Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q_0, which is the logical AND of the two data inputs (D_{sa}, D_{sb}) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	14 11	17 16	ns ns
f_{max}	maximum clock frequency		60	58	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT164P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT164D; PC74HC/HCT164D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT164T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	D_{sa}, D_{sb}	data inputs
3, 4, 5, 6, 10, 11, 12, 13	Q_0 to Q_7	outputs
7	GND	ground (0 V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	master reset input (active LOW)
14	V_{CC}	positive supply voltage

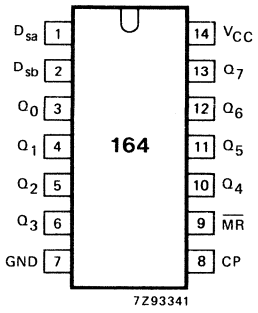


Fig. 1 Pin configuration.

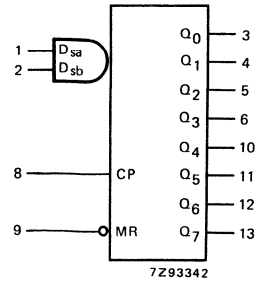


Fig. 2 Logic symbol.

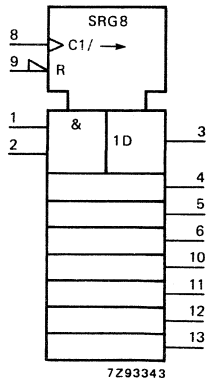


Fig. 3 IEC logic symbol.

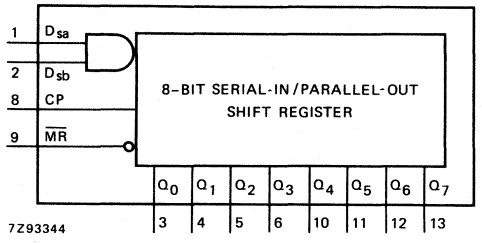


Fig. 4 Functional diagram.

APPLICATIONS

- **Serial data transfer**

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	$Q_1 - Q_7$
reset (clear)	L	X	X	X	L	L — L
shift	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

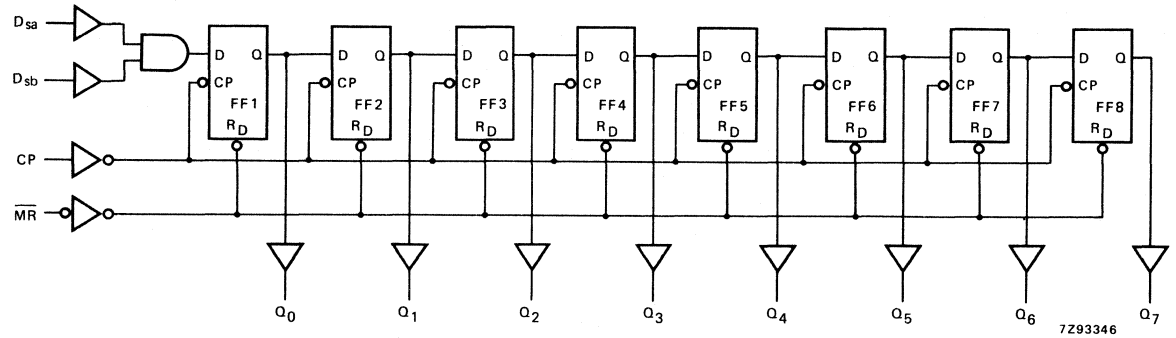


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_{sa}, D_{sb}	0.25
CP	0.60
$\overline{MR}$	0.90

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; LOW	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_{sa}, D_{sb} to CP	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_{sa}, D_{sb} to CP	4 4 4			4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 9
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			40		50		60	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			38		48		57	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	18			23		27		ns	4.5	Fig. 6
t_W	master reset pulse width; LOW	18			23		27		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	16			20		24		ns	4.5	Fig. 7
t_{su}	set-up time D_{sa}, D_{sb} to CP	12			15		18		ns	4.5	Fig. 9
t_h	hold time D_{sa}, D_{sb} to CP	4			4		4		ns	4.5	Fig. 9
f_{max}	maximum clock pulse frequency	27			22		18		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

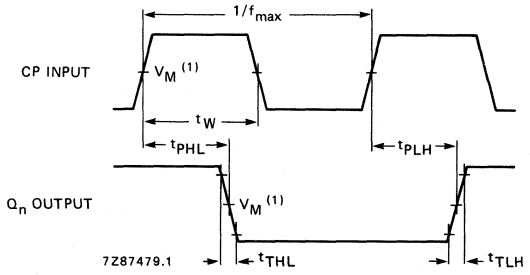


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

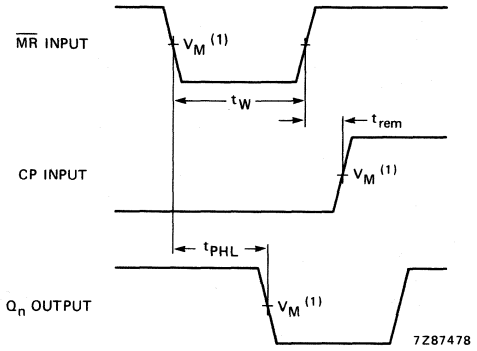


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

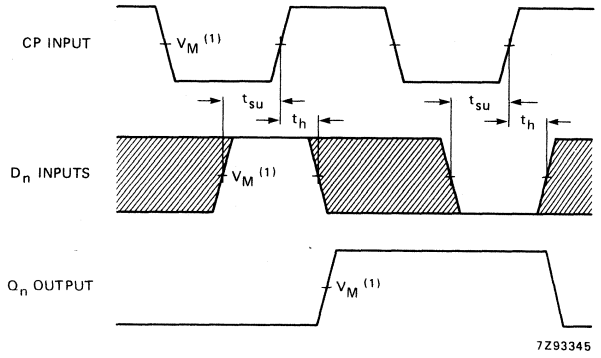


Fig. 8 Waveforms showing the data set-up and hold times for D_n inputs.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

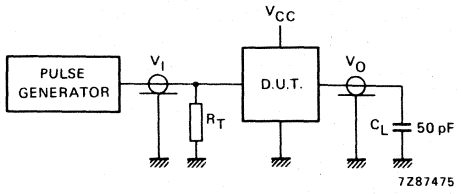


Fig. 9 Test circuit.

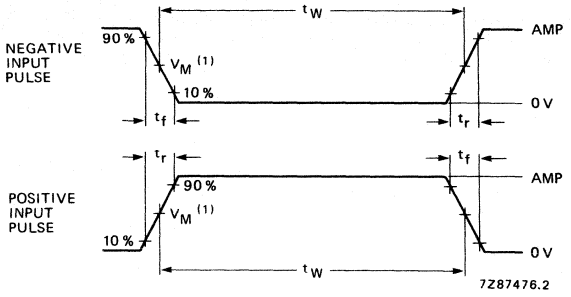


Fig. 10 Input pulse definitions.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

FEATURES

- **Asynchronous 8-bit parallel load**
- **Synchronous serial input**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT165 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT165 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs (Q_7 and $\overline{Q}_7$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D_0 to D_7 inputs are loaded into the register asynchronously.

When $\overline{PL}$ is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input $\overline{CE}$ should only take place while CP HIGH for predictable operation. Also, the CP and $\overline{CE}$ should be LOW before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is released.

APPLICATIONS

- **Parallel-to-serial data conversion**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_7, $\overline{Q}_7$ $\overline{PL}$ to Q_7, $\overline{Q}_7$ D_7 to Q_7, $\overline{Q}_7$	C_L = 15 pF V_{CC} = 5 V	 14 14 9	 14 17 11	 ns ns ns
f_{max}	maximum clock frequency		60	60	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	35	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT165P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT165D; PC74HC/HCT165D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT165T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{PL}$	asynchronous parallel load input (active LOW)
7	$\overline{Q}_7$	complementary output from the last stage
9	Q_7	serial output from the last stage
2	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
10	D_S	serial data input
11, 12, 13, 14, 3, 4, 5, 6	D_0 to D_7	parallel data inputs
15	$\overline{CE}$	clock enable input (active LOW)
16	V_{CC}	positive supply voltage

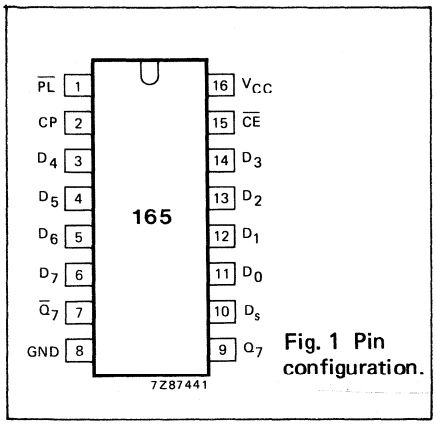


Fig. 1 Pin configuration.

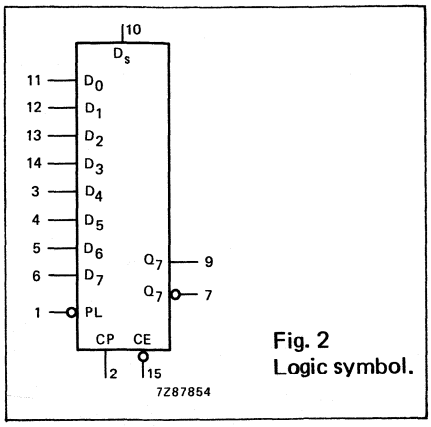


Fig. 2 Logic symbol.

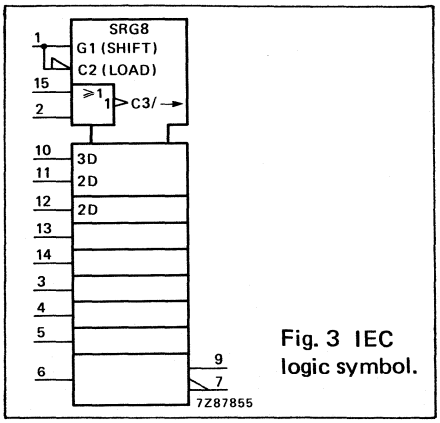


Fig. 3 IEC logic symbol.

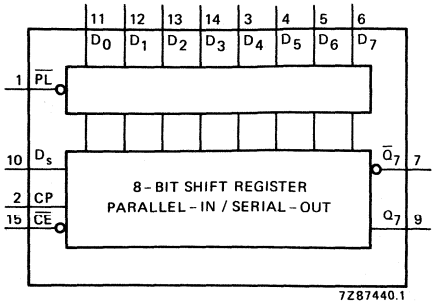


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTERS		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_s	D_0-D_7	Q_0	Q_1-Q_6	Q_7	$\overline{Q}_7$
parallel load	L L	X X	X X	X X	L H	L H	L - L H - H	L H	H L
serial shift	H H	L L	↑ ↑	l h	X X	L H	q_0-q_5 q_0-q_5	q_6 q_6	$\overline{q}_6$ $\overline{q}_6$
hold "do nothing"	H	H	X	X	X	q_0	q_1-q_6	q_7	q_7

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

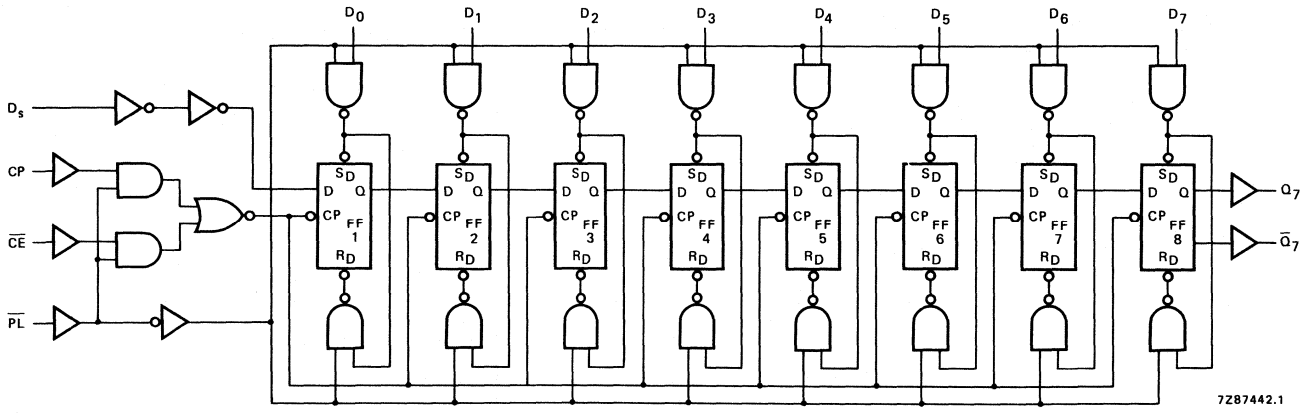


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_0 to D_7	0.35
D_S	0.35
$\overline{CP}$	0.65
$\overline{CE}$	0.65
$\overline{PL}$	0.65

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
			+25		−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_7, $\overline{Q}_7$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay D_7 to Q_7, $\overline{Q}_7$			120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	parallel load pulse width; LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_s to CP, $\overline{CE}$	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time $\overline{PL}$ to CP, $\overline{CE}$	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
$t_{su(L)}$	set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to $\overline{PL}$	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D_s to CP, $\overline{CE}$ D_n to $\overline{PL}$	35 7 6			45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time $\overline{PL}$, $\overline{CE}$ to CP $\overline{PL}$, CP to $\overline{CE}$	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$			34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_7, $\overline{Q}_7$			40		50		60	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay D_7 to Q_7, $\overline{Q}_7$			28		35		42	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 6
t_W	parallel load pulse width; LOW	20			25		30		ns	4.5	Fig. 7
t_{su}	set-up time D_s to CP, $\overline{CE}$	20			25		30		ns	4.5	Fig. 9
t_{su}	set-up time $\overline{PL}$ to CP, $\overline{CE}$	20			25		30		ns	4.5	Fig. 7
$t_{su(L)}$	set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	20			25		30		ns	4.5	Fig. 9
t_{su}	set-up time D_n to $\overline{PL}$	20			25		30		ns	4.5	Fig. 10
t_h	hold time D_s to CP, $\overline{CE}$; D_n to $\overline{PL}$	7			9		11		ns	4.5	Fig. 9
t_h	hold time $\overline{PL}$, $\overline{CE}$ to CP; $\overline{PL}$, CP to $\overline{CE}$	0			0		0		ns	4.5	Fig. 9
f_{max}	maximum clock pulse frequency	30			24		20		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

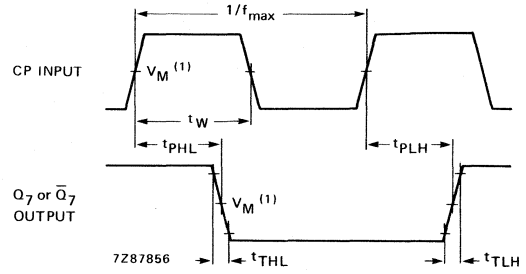


Fig. 6 Waveforms showing the clock (CP) to output (Q_7 or $\overline{Q}_7$) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

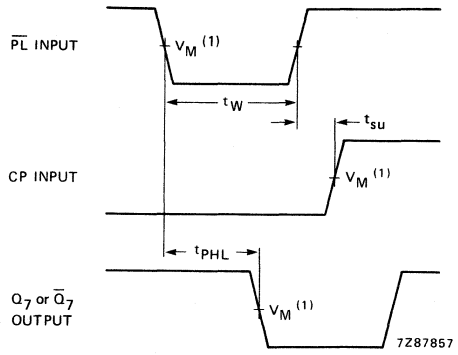


Fig. 7 Waveforms showing the parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q_7 or $\overline{Q}_7$) propagation delays and the parallel load to clock (CP) set-up time.

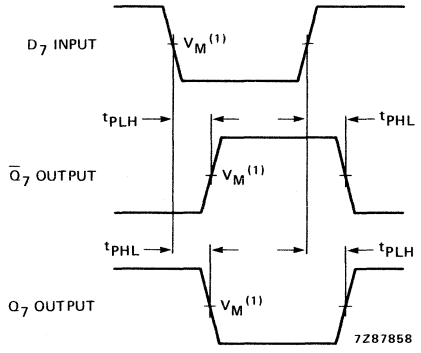


Fig. 8 Waveforms showing the data input (D_n) to output (Q_7 or $\overline{Q}_7$) propagation delays when $\overline{PL}$ is LOW.

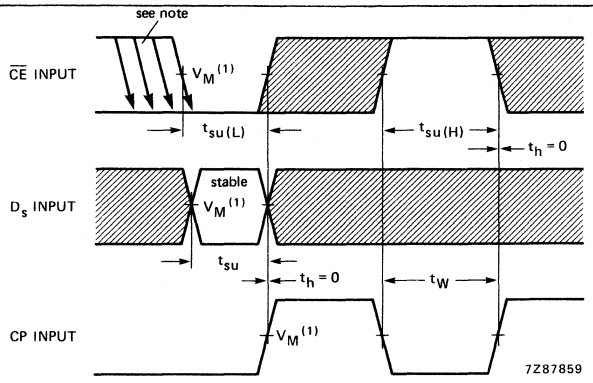


Fig. 9 Waveforms showing the set-up and hold times from the serial data input (D_s) to the clock (CP), from the clock enable input (LOW $\overline{CE}$) to the clock (CP) and from the clock enable input $\overline{CE}$ to the clock (CP).

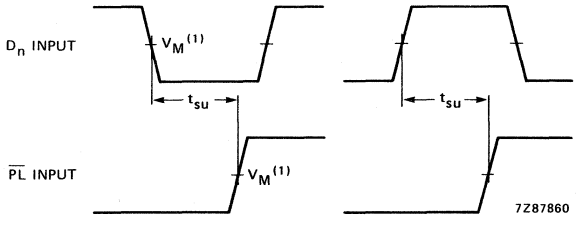


Fig. 10 Waveforms showing the set-up and hold times from the data inputs D_5 and D_7 to the parallel load input ($\overline{PL}$).

Note to Figs 6 and 7

The changing to output assumes internal Q_6 opposite state from Q_7.

Note to Fig. 9

$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

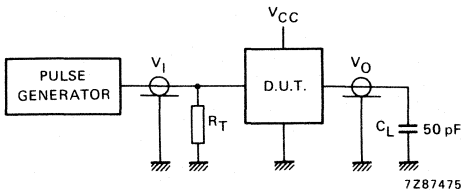


Fig. 11 Test circuit.

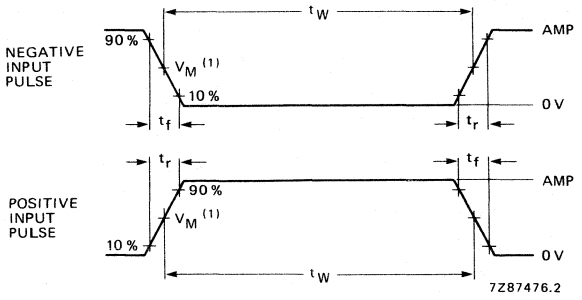


Fig. 12 Input pulse definitions.

Definitions for Figs 11 and 12:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

FEATURES

- Synchronous parallel-to-serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous master reset
- For asynchronous parallel data load see "165"
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT166 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT166 are 8-bit shift registers which have a fully synchronous serial or parallel data entry selected by an active LOW parallel enable ($\overline{PE}$) input. When $\overline{PE}$ is LOW one set-up time prior to the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into the internal bit position Q_0 from serial data input (D_s), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition.
This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_s input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input $\overline{CE}$ should only take place while CP is HIGH for predictable operation. A LOW on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_7 $\overline{MR}$ to Q_7	C_L = 15 pF V_{CC} = 5 V	14 14	17 19	ns ns
f_{max}	maximum clock frequency		59	49	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	41	41	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT166D; PC74HC/HCT166P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT166D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT166T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	D_s	serial data input
2, 3, 4, 5, 10, 11, 12, 14	D_0 to D_7	parallel data inputs
6	$\overline{CE}$	clock enable input (active LOW)
7	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
9	$\overline{MR}$	asynchronous master reset input (active LOW)
13	Q_7	serial output from the last stage
15	$\overline{PE}$	parallel enable input (active LOW)
16	V_{CC}	positive supply voltage

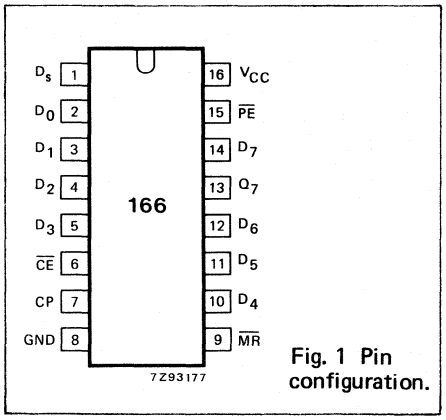


Fig. 1 Pin configuration.

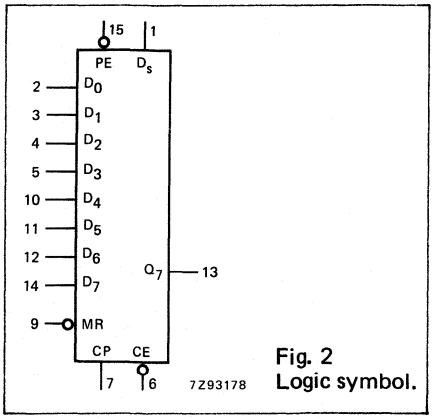


Fig. 2 Logic symbol.

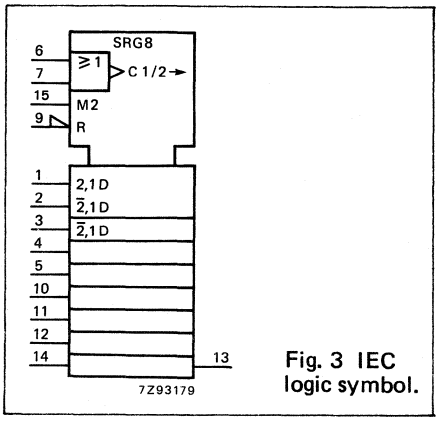


Fig. 3 IEC logic symbol.

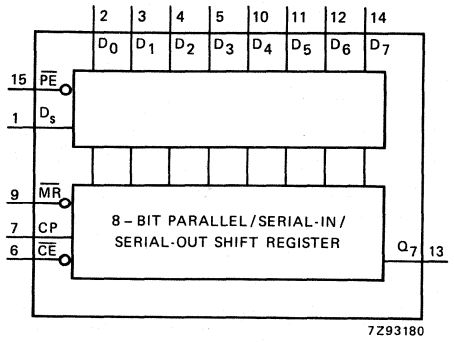


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUT
	$\overline{PE}$	$\overline{CE}$	CP	D_S	D_0-D_7	Q_0	Q_1-Q_6	Q_7
parallel load	l	l	↑	X	l - l	L	L - L	L
	l	l	↑	X	h - h	H	H - H	H
serial shift	h	l	↑	l	X - X	L	q_0- q_5	q_6
	h	l	↑	h	X - X	H	q_0- q_5	q_6
hold "do nothing"	X	h	X	X	X - X	q_0	q_1 - q_6	q_7

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

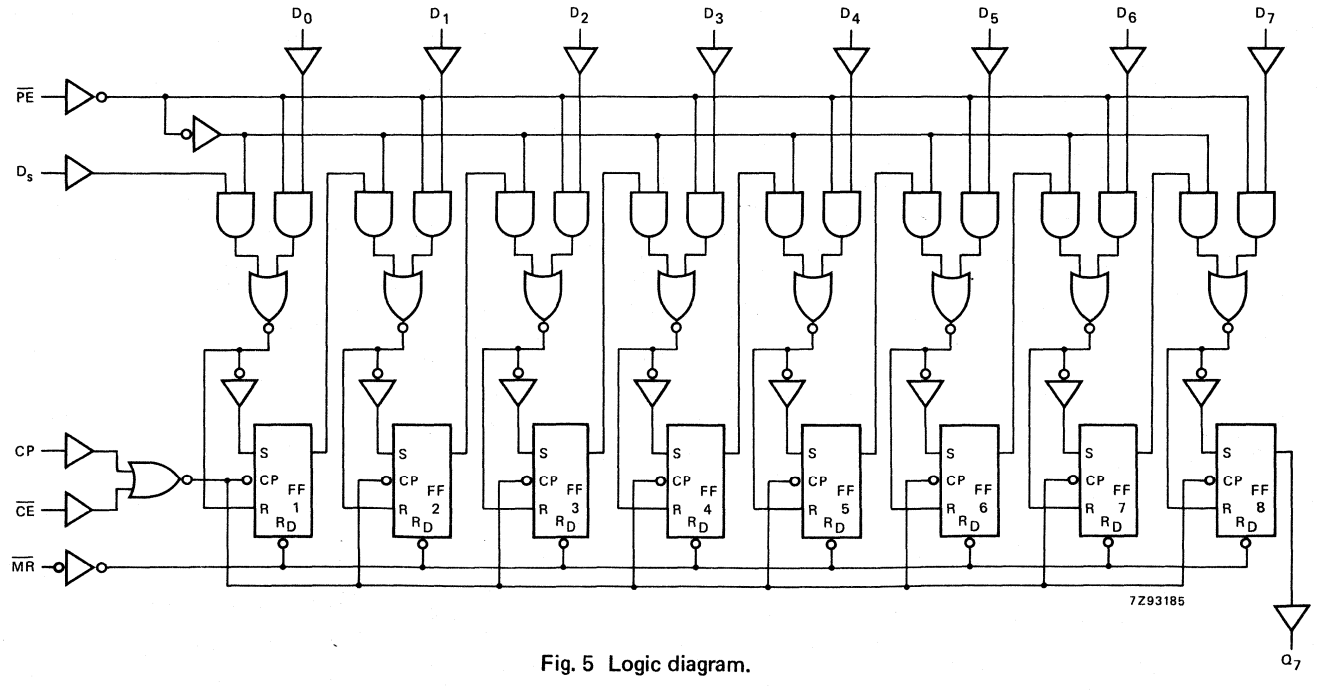


Fig. 5 Logic diagram.

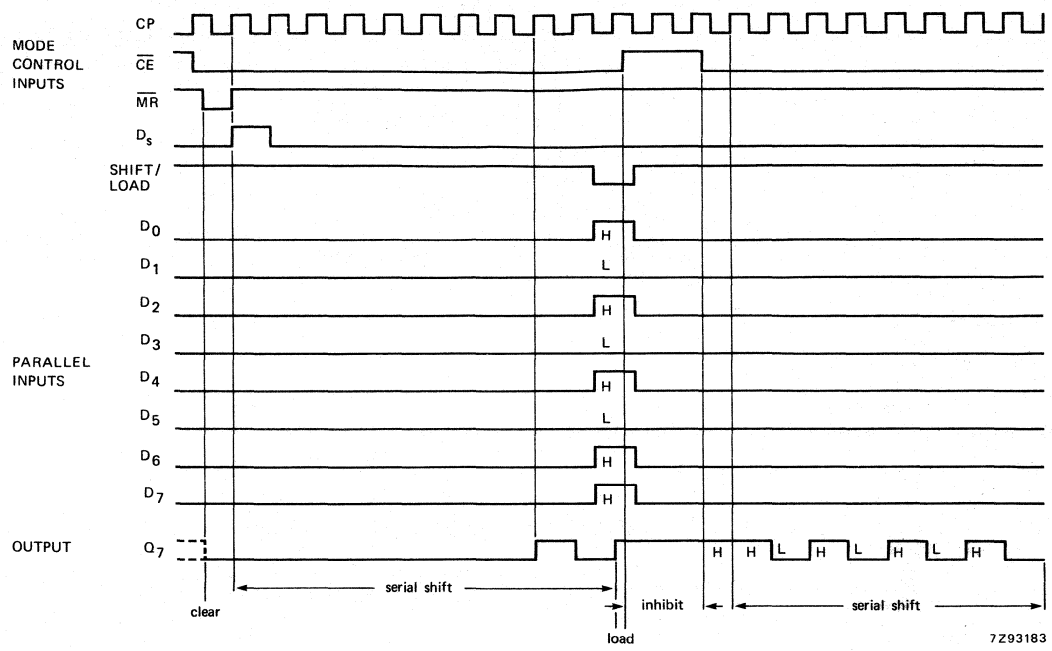


Fig. 6 Typical clear, shift, load, inhibit, and shift sequences.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_0 to D_7	0.35
D_S	0.35
$\overline{CP}$	0.80
$\overline{CE}$	0.80
$\overline{MR}$	0.40
$\overline{PE}$	0.60

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_7			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q_7			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width	125 25 21			155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n, $\overline{CE}$ to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time $\overline{PE}$ to CP	150 30 26			190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n, $\overline{CE}$ to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time $\overline{PE}$ to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_7			40		50		60	ns	4.5	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q_7			45		56		68	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 7
t_W	master reset pulse width	25			31		38		ns	4.5	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	0			0		0		ns	4.5	Fig. 8
t_{su}	set-up time D_n, $\overline{CE}$ to CP	16			20		24		ns	4.5	Fig. 9
t_{su}	set-up time $\overline{PE}$ to CP	30			38		45		ns	4.5	Fig. 8
t_h	hold time D_n, $\overline{CE}$ to CP	0			0		0		ns	4.5	Fig. 9
t_h	hold time $\overline{PE}$ to CP	0			0		0		ns	4.5	Fig. 9
f_{max}	maximum clock pulse frequency	25			20		17		MHz	4.5	Fig. 7

AC WAVEFORMS

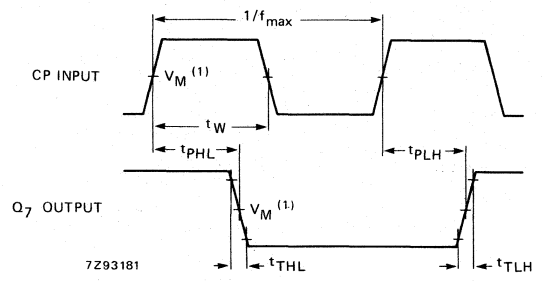


Fig. 7 Waveforms showing the clock (CP) to output (Q_7) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

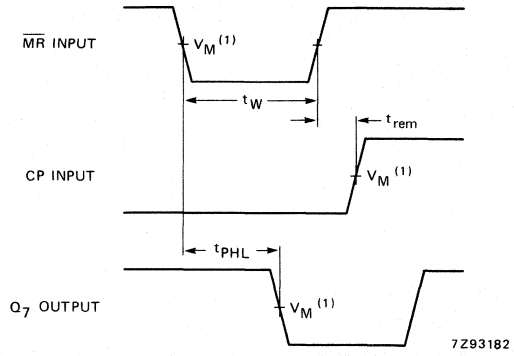


Fig. 8 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_7) propagation delay and the master reset to clock (CP) removal time.

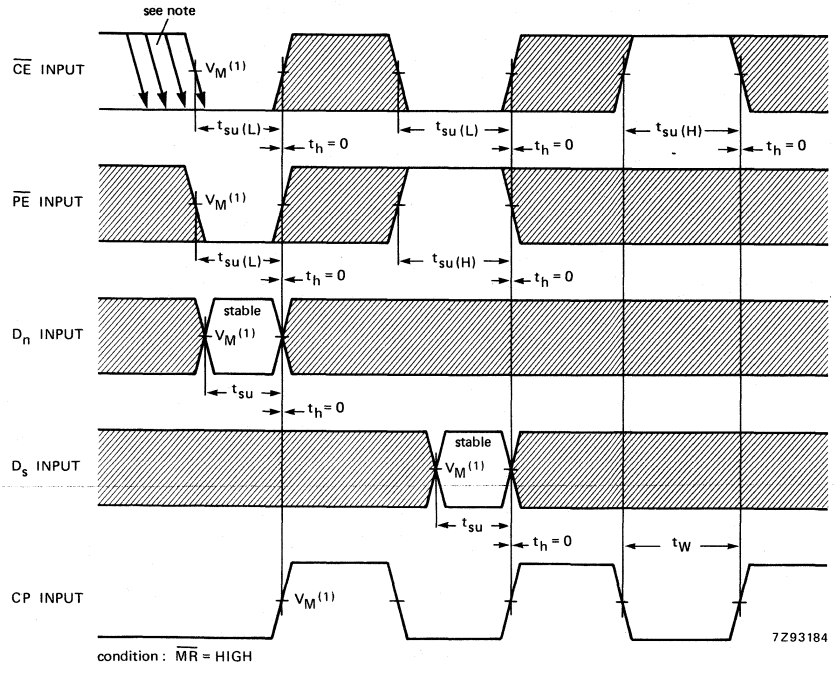


Fig. 9 Waveforms showing the set-up and hold times from the serial data input (D_S), the data inputs (D_n), the clock enable input (LOW $\overline{CE}$), the clock enable input $\overline{CE}$ and the parallel enable input to the clock (CP).

Note to Fig. 7

The changing to output assumes internal Q_6 opposite state from Q_7.

Note to Figs 7, 8 and 9

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the function table.

Note to Fig. 9

$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

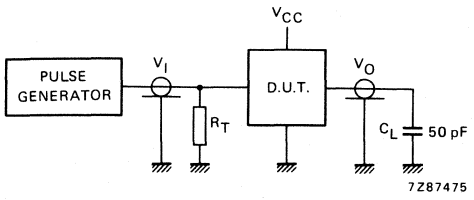


Fig. 10 Test circuit.

Definitions for Figs 10 and 11:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

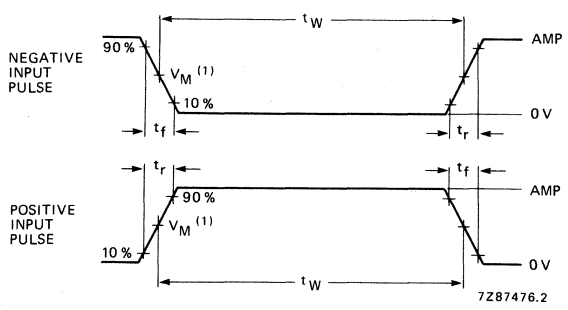


Fig. 11 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE

FEATURES

- **Gated input enable for hold (do nothing) mode**
- **Gated output enable control**
- **Edge-triggered D-type register**
- **Asynchronous master reset**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q_0 to Q_3) and master reset (MR).

When the two clock enable inputs ($\overline{E}_1$ and $\overline{E}_2$) are LOW, the data on the D_n inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both $\overline{E}_n$ inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ($\overline{OE}_1$ and $\overline{OE}_2$) are LOW, the data in the register is presented to the Q_n outputs. When one or both $\overline{OE}_n$ inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the $\overline{OE}_n$ transition does not affect the clock and reset operations.

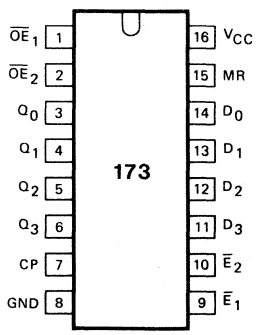


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	25	26	ns
f_{max}	maximum clock frequency		55	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT173P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT173D; PC74HC/HCT173D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT173T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
3, 4, 5, 6	Q_0 to Q_3	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\overline{E}_1$, $\overline{E}_2$	clock enable inputs (active LOW)
14, 13, 12, 11	D_0 to D_3	data inputs
15	MR	asynchronous master reset (active HIGH)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (register)
reset (clear)	H	X	X	X	X	L
parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	Q_n (register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0	Q_1	Q_2	Q_3
read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

HEX D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- **Six edge-triggered D-type flip-flops**
- **Asynchronous master reset**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT174 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT174 have six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output of the flip-flop.

A LOW level on the $\overline{MR}$ input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications where the true output is only required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	15	17	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT174P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT174D; PC74HC/HCT174D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT174T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2, 5, 7, 10, 12, 15	Q_0 to Q_5	flip-flop outputs
3, 4, 6, 11, 13, 14	D_0 to D_3	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

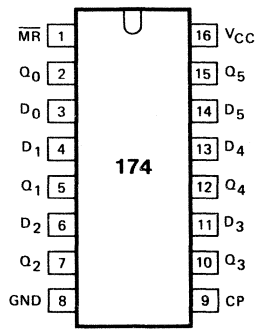


Fig. 1 Pin configuration.

QUAD D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Four edge-triggered D flip-flops
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT175 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT175 have four edge-triggered, D-type flip-flops with individual D inputs and both Q and $\overline{Q}$ outputs.

The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All Q_n outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$ $\overline{MR}$ to Q_n CP to Q_n, $\overline{Q}_n$ $\overline{MR}$ to $\overline{Q}_n$	C_L = 15 pF V_{CC} = 5 V	14 14 14 14	14 17 14 14	ns ns ns ns
f_{max}	maximum clock frequency		60	52	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	32	34	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT175P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT175D; PC74HC/HCT175D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT175T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 7, 10, 15	Q_0 to Q_3	flip-flop outputs
3, 6, 11, 14	$\overline{Q}_0$ to $\overline{Q}_3$	complementary flip-flop outputs
4, 5, 12, 13	D_0 to D_3	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

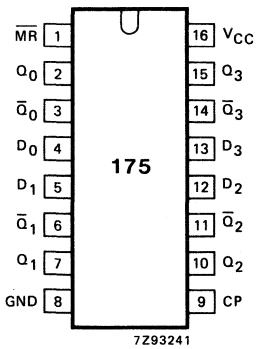


Fig. 1 Pin configuration.

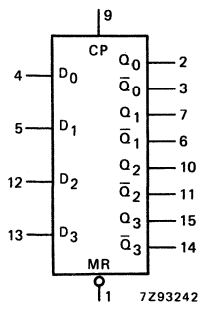


Fig. 2 Logic symbol.

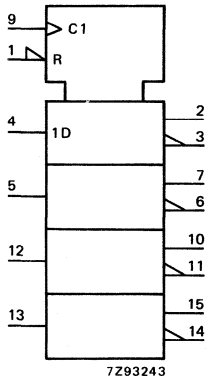


Fig. 3 IEC logic symbol.

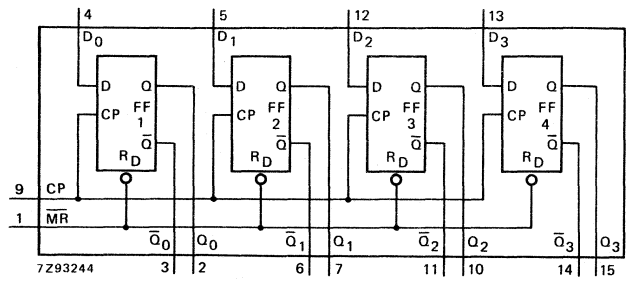


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
reset (clear)	L	X	X	L	H
load "1"	H	↑	h	H	L
load "0"	H	↑	l	L	H

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = don't care

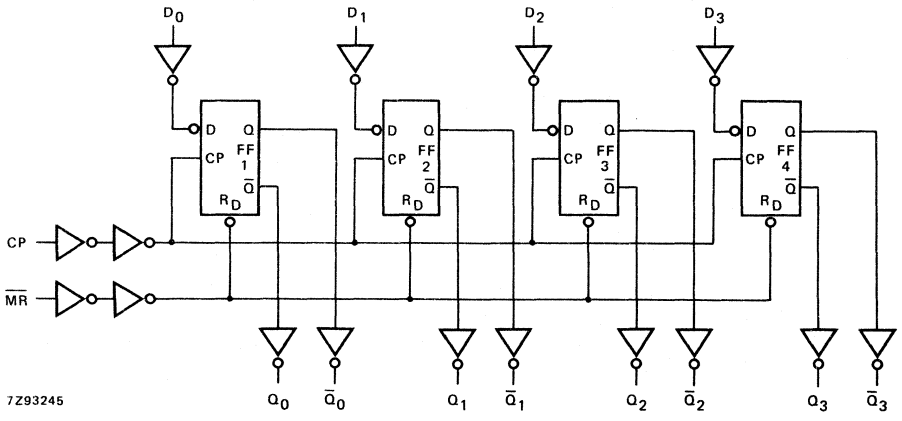


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$\overline{MR}$	1.00
CP	0.60
D_n	0.40

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time CP to D_n	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$			35		44		53	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			40		50		60	ns	4.5	Fig. 8
t_{PLH}	propagation delay $\overline{MR}$ to $\overline{Q}_n$			35		44		53	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 6
t_W	master reset pulse width LOW	20			25		30		ns	4.5	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	5			5		5		ns	4.5	Fig. 8
t_{su}	set-up time D_n to CP	20			25		30		ns	4.5	Fig. 7
t_h	hold time CP to D_n	5			5		5		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	25			20		17		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

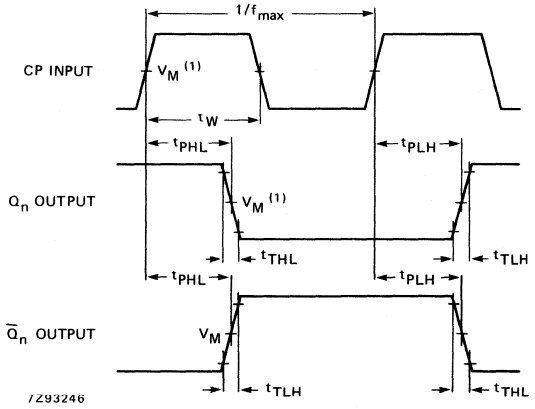


Fig. 6 Waveforms showing the clock (CP) to outputs (Q_n, $\overline{Q}_n$) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

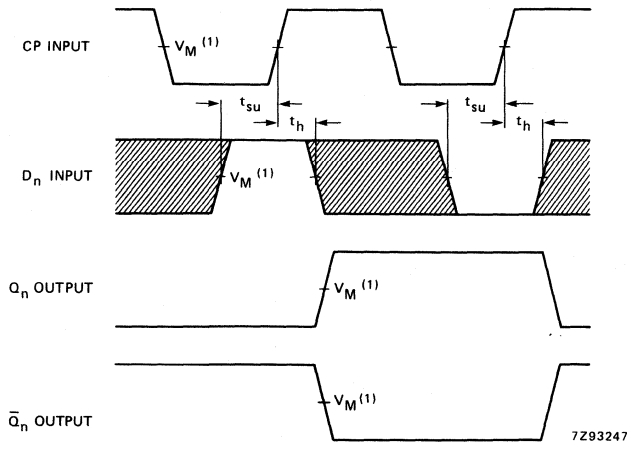


Fig. 7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

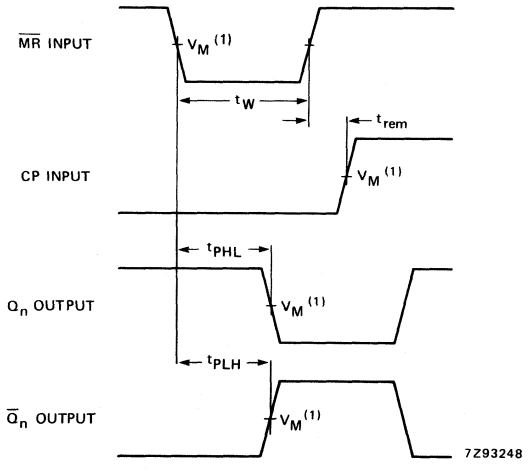


Fig. 8 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to outputs (Q_n, $\overline{Q}_n$) propagation delays and the master reset to clock (CP) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

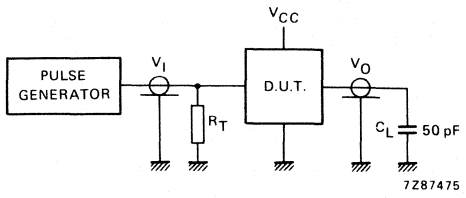


Fig. 9 Test circuit.

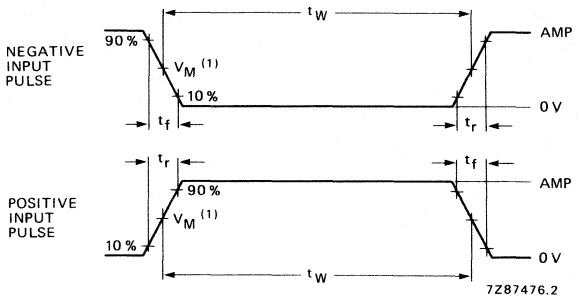


Fig. 10 Input pulse definitions.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

4-BIT ARITHMETIC LOGIC UNIT

FEATURES

- **Full carry look-ahead for high-speed arithmetic operation on long words**
- **Provides 16 arithmetic operations: add, subtract, compare, double, plus 12 others**
- **Provides all 16 logic operations of two variables: EXCLUSIVE-OR, compare, AND, NAND, NOR, OR plus 10 other logic operations**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT181 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT181 are 4-bit high-speed parallel Arithmetic Logic Units (ALU). Controlled by the four function select inputs (S_0 to S_3) and the mode control inputs (M), they can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands (see function table).

When the mode control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When M is LOW, the carries are enabled and the "181" performs arithmetic operations on the two 4-bit words. The "181" incorporates full internal carry look-ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the carry

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ or $\overline{B}_n$ to A=B	C_L = 15 pF; V_{CC} = 5 V	34	36	ns
	C_n to C_{n+4}		14	16	ns
	$\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$, $\overline{P}$, $\overline{F}$, C_{n+4}		17	19	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT181P: 24-lead DIL; plastic (SOT-101A).
PC54HC/HCT181D; PC74HC/HCT181D: 24-lead DIL; ceramic (cerdip) (SOT-94).
PC74HC/HCT181T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 22, 20, 18	$\overline{B}_0$ to $\overline{B}_3$	operand inputs (active LOW)
2, 23, 21, 19	$\overline{A}_0$ to $\overline{A}_3$	operand inputs (active LOW)
6, 5, 4, 3	S_0 to S_3	select inputs
7	C_n	carry input
8	M	mode control input
9, 10, 11, 13	$\overline{F}_0$ to $\overline{F}_3$	function outputs (active LOW)
12	GND	ground (0 V)
14	A=B	comparator output
15	$\overline{P}$	carry propagate output (active LOW)
16	C_{n+4}	carry output
17	$\overline{G}$	carry generate output (active LOW)
24	V_{CC}	positive supply voltage

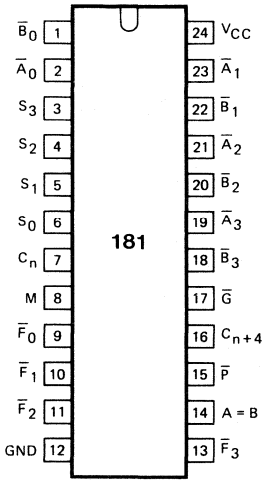


Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

propagation ($\overline{P}$) and carry generate ($\overline{G}$) signals. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the carry output (C_{n+4}) signal to the carry input (C_n) of the next unit.

For high-speed operation the device is used in conjunction with the "182" carry look-ahead circuit. One carry look-ahead package is required for each group of four "181" devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The comparator output (A=B) of the device goes HIGH when all four function outputs ($\overline{F}_0$ to $\overline{F}_3$) are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. A=B is an open drain output and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The A=B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The function table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no under-flow and no carry is generated when there is underflow.

As indicated, the "181" can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands.

FUNCTION TABLES

MODE SELECT INPUTS				ACTIVE HIGH INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC** (M=L; C_n=H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	A ⊕ B	A minus B minus 1
L	H	H	H	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}$ + B	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	logical 1	A plus A*
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC** (M=L; C_n=L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1
L	L	H	H	logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$
H	L	L	L	$\overline{A}B$	A plus (A + B)
H	L	L	H	A ⊕ B	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	logical 0	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A
H	H	H	L	AB	A$\overline{B}$ plus A
H	H	H	H	A	A

Notes to function tables

* Each bit is shifted to the next more significant position.
** Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

LOOK-AHEAD CARRY GENERATOR

FEATURES

- **Provides carry look-ahead across a group of four ALU's**
- **Multi-level look-ahead for high-speed arithmetic operation over long word length**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT182 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT182 carry look-ahead generators accept up to four pairs of active LOW carry propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and carry generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH carry input (C_n). The devices provide anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders.

The "182" also has active LOW carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 = P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The "182" can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{P}_n$, $\overline{G}_n$, C_n to any output	C_L = 15 pF; V_{CC} = 5 V	18	20	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT182P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT182D; PC74HC/HCT182D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT182T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	$\overline{G}_0$ to $\overline{G}_3$	carry generate inputs (active LOW)
4, 2, 15, 6	$\overline{P}_0$ to $\overline{P}_3$	carry propagate inputs (active LOW)
7	$\overline{P}$	carry propagate output (active LOW)
8	GND	ground (0 V)
9	C_{n+z}	function output
10	$\overline{G}$	carry generate output (active LOW)
11	C_{n+y}	function output
12	C_{n+x}	function output
13	C_n	carry input (active HIGH)
16	V_{CC}	positive supply voltage

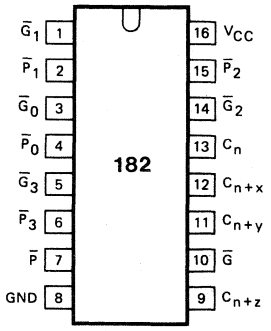


Fig. 1 Pin configuration.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	H	H	X	H	X					L		
X	H	X	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	L					H		
X	X	X	L	X	X	L					H		
X	X	L	X	L	X	L					H		
H	X	L	X	L	X	L					H		
X	X	X	X	X	H	X	H	H				H	
X	X	X	H	X	H	X	H	X				H	
X	X	X	H	X	H	X	H	L				H	
X	X	X	H	X	H	X	H	L				H	
X	X	X	L	X	L	L	L	L				L	
X	X	X	L	X	X	L	X	L				L	
X	X	X	L	X	X	L	X	L				L	
X	X	X	L	X	X	L	X	L				L	
X	H	H		X		X		X					H
X	X	H		H		X		X					H
X	X	H		X		H		X					H
X	X	H		X		X		X					H
X	X	L		X		L		L					L
X	X	L		X		L		L					L
X	X	L		X		L		L					L
X	X	L		X		L		L					L

H = HIGH voltage level
L = LOW voltage level
X = don't care

PRESETTABLE SYNCHRONOUS BCD DECADE UP/DOWN COUNTER

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT190 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT190 are asynchronously presettable up/down BCD decade counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}/D$) input signal determines the direction of counting as indicated in the function table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}/D$ input should be changed only when either $\overline{CE}$ or CP is HIGH.

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SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	22	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT190P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT190D; PC74HC/HCT190D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT190T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	$\overline{CE}$	count enable input (active LOW)
5	$\overline{U}/D$	up/down input
8	GND	ground (0 V)
11	$\overline{PL}$	parallel load input (active LOW)
12	TC	terminal count output
13	$\overline{RC}$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

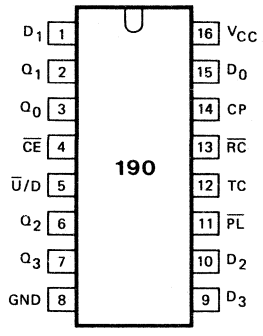

Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}/D$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the $\overline{RC}$ follows the clock pulse (CP). This feature simplifies the design of multistage counters. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the function table. The TC output can be used to accomplish look-ahead for high-speed operation.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
parallel load	L L	X X	X X	X X	L H	L H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊓	H	X	X	H	⊓	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	⊓	⊓

H = HIGH voltage level
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition
⊓ = one LOW level pulse
⊓ = TC goes LOW on a LOW-to-HIGH CP transition

PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT191 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT191 are asynchronously presettable 4-bit binary up/down counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}$/D) input signal determines the direction of counting as indicated in the function table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}$/D input should be changed only when either $\overline{CE}$ or CP is HIGH.

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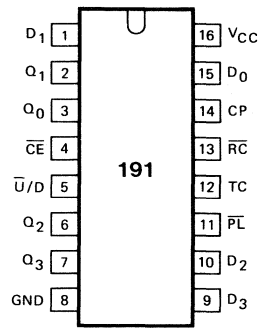

Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	22	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT191D; PC74HC/HCT191P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT191D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT191T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	$\overline{CE}$	count enable input (active LOW)
5	$\overline{U}$/D	up/down input
8	GND	ground (0 V)
11	$\overline{PL}$	parallel load input (active LOW)
12	TC	terminal count output
13	$\overline{RC}$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION (Cont'd)

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "15" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}/D$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the $\overline{RC}$ follows the clock pulse (CP). This feature simplifies the design of multistage counters. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the function table. The TC output can be used to accomplish look-ahead for high-speed operation.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
parallel load	L L	X X	X X	X X	L H	L H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓⊔	H	H	H	H	⊓	⊓⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓⊔	L	L	L	L	⊓	⊓⊔

H = HIGH voltage level
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition
⊓⊔ = one LOW level pulse
⊓ = TC goes LOW on a LOW-to-HIGH CP transition

PRESETTABLE SYNCHRONOUS BCD DECADE UP/DOWN COUNTER

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT192 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT192 are synchronous BCD up/down counters. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The "192" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

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SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_D, CP_U to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	22	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT192P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT192D; PC74HC/HCT192D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT192T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	CP_D	count down clock input*
5	CP_U	count up clock input*
8	GND	ground (0 V)
11	$\overline{PL}$	asynchronous parallel load input (active LOW)
12	$\overline{TC}_U$	terminal count up (carry) output (active LOW)
13	$\overline{TC}_D$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

* LOW-to-HIGH, edge triggered

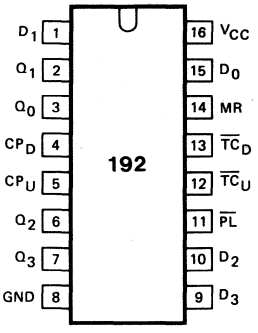


Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

One clock should be held HIGH while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9, the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW.
$\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock.
Likewise, the TC_D output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs (Q_0 to Q_3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q_0 to Q_3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X	X	count down				H	H**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition

* $\overline{TC}_U = CP_U$ at terminal count up (HLLH)
** $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT193 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The "193" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

(continued on next page)

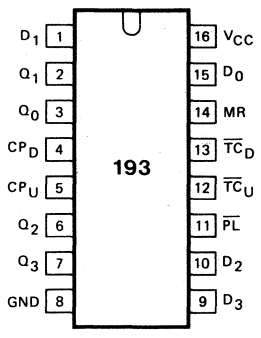


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_D, CP_U to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	22	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT193P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT193D; PC74HC/HCT193D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT193T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	CP_D	count down clock input*
5	CP_U	count up clock input*
8	GND	ground (0 V)
11	$\overline{PL}$	asynchronous parallel load input (active LOW)
12	$\overline{TC}_U$	terminal count up (carry) output (active LOW)
13	$\overline{TC}_D$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

* LOW-to-HIGH, edge triggered

GENERAL DESCRIPTION (Cont'd)

One clock should be held HIGH while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15,the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW.
$\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock.
Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs (Q_0 to Q_3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q_0 to Q_3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X	X	count down				H	H**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
* $\overline{TC}_U$ = CP_U at terminal count up (HHHH)
** $\overline{TC}_D$ = CP_D at terminal count down (LLLL)

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

FEATURES

- **Shift-left and shift-right capability**
- **Synchronous parallel and serial data transfer**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous master reset**
- **Hold ("do nothing") mode**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT194 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The functional characteristics of the 54/74HC/HCT194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.

The "194" design has special features which increase the range of application. The synchronous operation of the device is determined by the mode select inputs (S_0, S_1). As shown in the mode select table, data can be entered and shifted from left to right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) or, right to left ($Q_3 \rightarrow Q_2 \rightarrow Q_1$, etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold ("do nothing") mode. The first and last stages provide D-type serial data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	13	13	ns
t_{PHL}	$\overline{MR}$ to Q_n		11	13	ns
f_{max}	maximum clock frequency		60	60	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT194D; PC74HC/HCT194P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT194D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT194T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset input (active LOW)
2	D_{SR}	serial data input (shift right)
3, 4, 5, 6	D_0 to D_3	parallel data inputs
7	D_{SL}	serial data input (shift left)
8	GND	ground (0 V)
9, 10	S_0, S_1	mode control inputs
11	CP	clock input (LOW-to-HIGH edge-triggered)
15, 14, 13, 12	Q_0 to Q_3	parallel outputs
16	V_{CC}	positive supply voltage

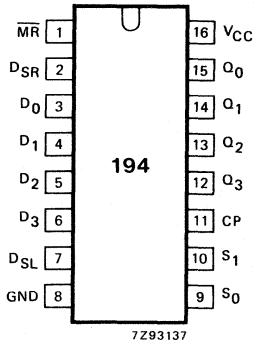


Fig. 1 Pin configuration.

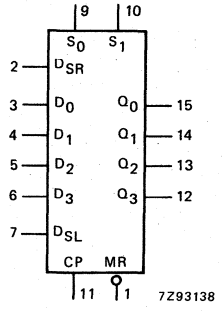


Fig. 2 Logic symbol.

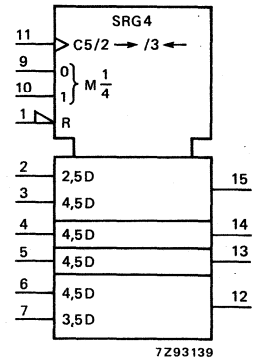


Fig. 3 IEC logic symbol.

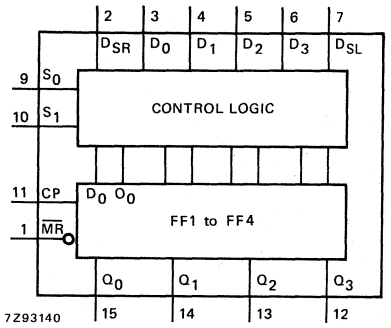


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd.)

inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The four parallel data inputs (D_0 to D_3) are D-type inputs. Data appearing on the D_0 to D_3 inputs, when S_0 and S_1 are HIGH, is transferred to the Q_0 to Q_3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

The "194" is similar in operation to the "195" universal shift register, with added features of shift-left without external connections and hold ("do nothing") modes of operation.

FUNCTION TABLE

OPERATING MODES	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
reset (clear)	X	L	X	X	X	X	X	L	L	L	L
hold ("do nothing")	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
shift left	↑ ↑	H H	h h	l l	X X	l h	X X	q_1 q_1	q_2 q_2	q_3 q_3	L H
shift right	↑ ↑	H H	l l	h h	l h	X X	X X	L H	q_0 q_0	q_1 q_1	q_2 q_2
parallel load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q,d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

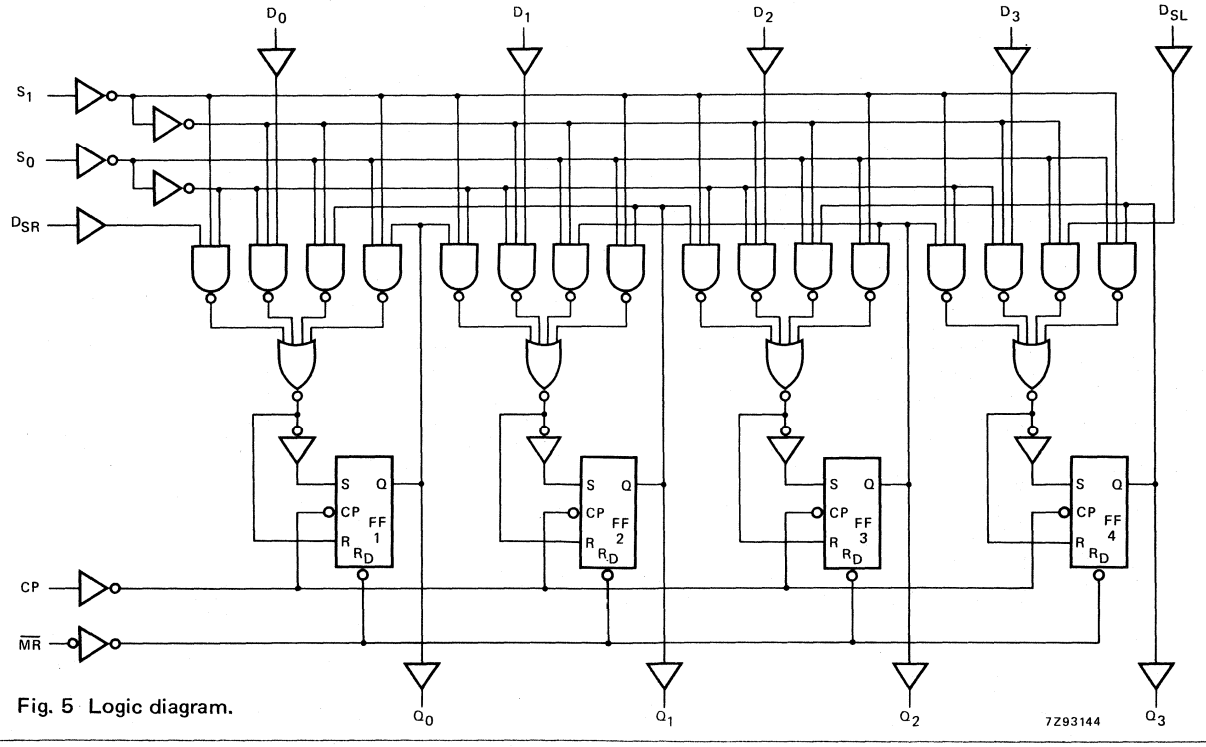


Fig. 5 Logic diagram.

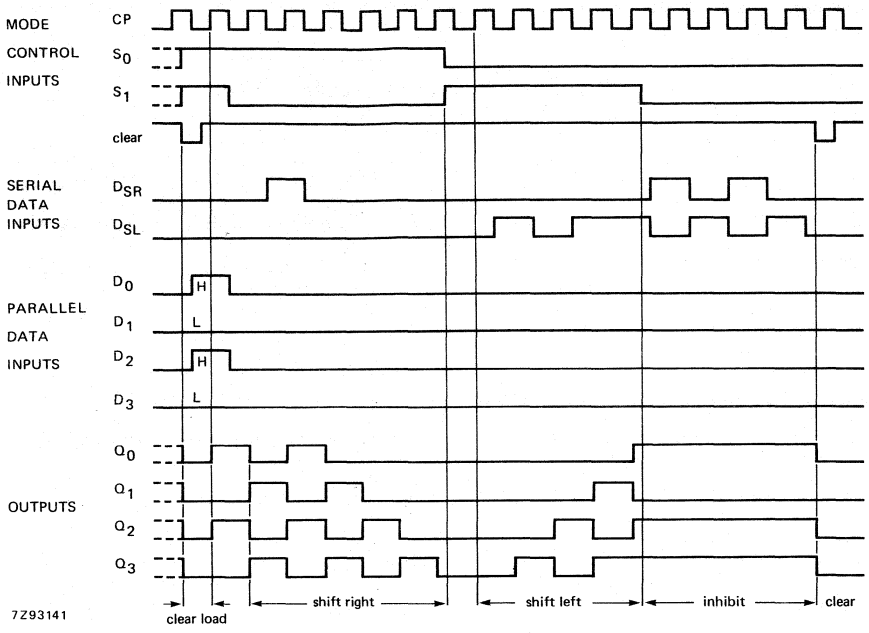


Fig. 6 Typical clear, clear-load, shift-right, shift-left, inhibit and clear timing sequences.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_n	0.15
D_{SR}, D_{SL}	0.15
$\overline{CP}$	0.50
$\overline{MR}$	0.45
S_n	0.90

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width; LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to CP	70 14 12			90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time S_0, S_1 to CP	80 16 12			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time D_{SR}, D_{SL} to CP	70 14 12			90 18 15		105 21 18		ns	2.0 4.5 6.0	
t_h	hold time D_n to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time S_0, S_1 to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D_{SR}, D_{SL} to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			32		40		48	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n			32		40		48	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 7
t_W	master reset pulse width; LOW	16			20		24		ns	4.5	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	12			15		18		ns	4.5	Fig. 8
t_{su}	set-up time D_n to CP	14			18		21		ns	4.5	Fig. 9
t_{su}	set-up time S_0, S_1 to CP	20			25		30		ns	4.5	Fig. 10
t_{su}	set-up time D_{SR}, D_{SL} to CP	16			20		24		ns	4.5	
t_h	hold time D_n to CP	0			0		0		ns	4.5	Fig. 9
t_h	hold time S_0, S_1 to CP	0			0		0		ns	4.5	Fig. 10
t_h	hold time D_{SR}, D_{SL} to CP	0			0		0		ns	4.5	
f_{max}	maximum clock pulse frequency	30			24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

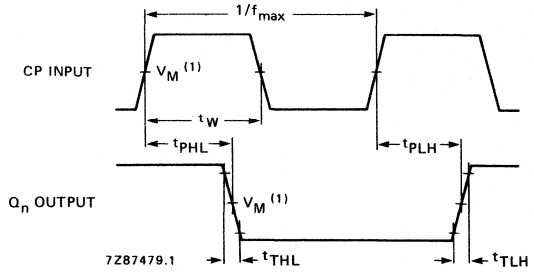


Fig. 7 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

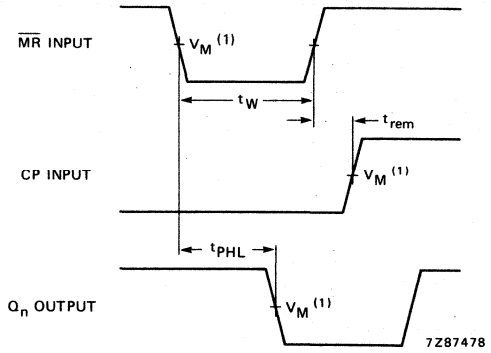


Fig. 8 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

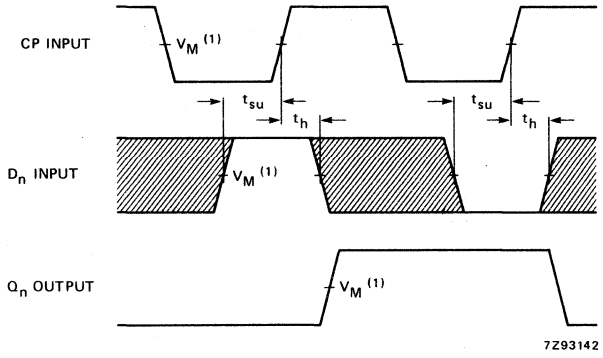


Fig. 9 Waveforms showing the set-up and hold times from the data inputs (D_n) to the clock (CP).

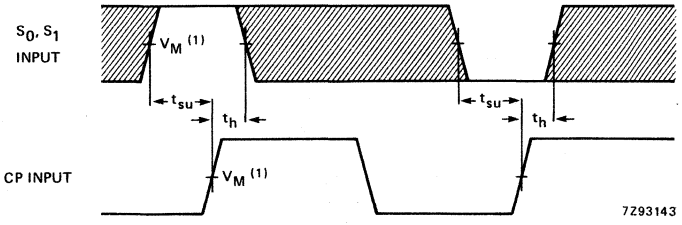


Fig. 10 Waveforms showing the set-up and hold times from the mode control inputs (S_n) to the clock input (CP).

Note to Figs 9 and 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

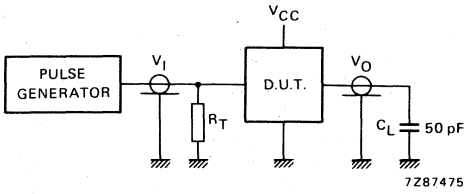


Fig. 11 Test circuit.

Definitions for Figs 11 and 12:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

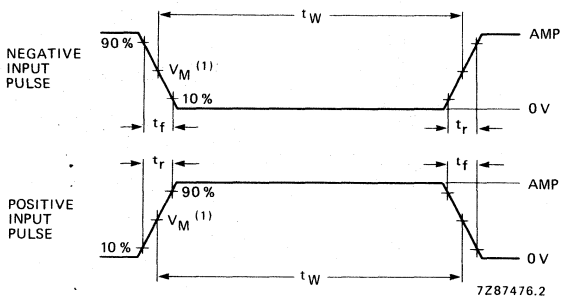


Fig. 12 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

4-BIT PARALLEL ACCESS SHIFT REGISTER

FEATURES

- **Asynchronous master reset**
- **J, $\overline{K}$, (D) inputs to the first stage**
- **Fully synchronous serial or parallel data transfer**
- **Shift right and parallel load capability**
- **Complement output from the last stage**
- **Output capability : standard**

GENERAL DESCRIPTION

The 54/74HC/HCT195 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT195 performs serial, parallel, serial-to-parallel or parallel-to-serial data transfer at very high speeds. The "195" operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the parallel load enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH and shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the $J\overline{K}$ type input for special applications and by tying the pins together, the simple D-type input for general applications. The "195" appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW.

After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0 to D_3) is transferred to the respective Q_0 to Q_3 outputs. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input LOW.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	14	14	ns
f_{max}	maximum clock frequency		60	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	105	105	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1,5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT195P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT195D; PC74HC/HCT195D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT195T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2	J	first stage J-input (active HIGH)
3	$\overline{K}$	first stage $\overline{K}$-input (active LOW)
4, 5, 6, 7	D_0 to D_3	parallel data inputs
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CP	clock input (LOW-to-HIGH edge-triggered)
11	$\overline{Q}_3$	inverted output from the last stage
15, 14, 13, 12	Q_0 to Q_3	parallel outputs
16	V_{CC}	positive supply voltage

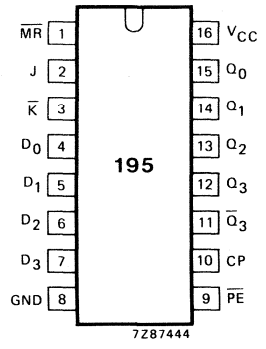


Fig. 1 Pin configuration.

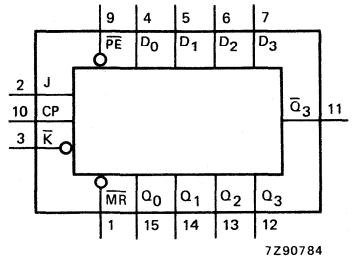


Fig. 2 Logic symbol.

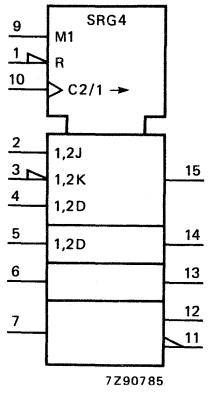


Fig. 3 IEC logic symbol.

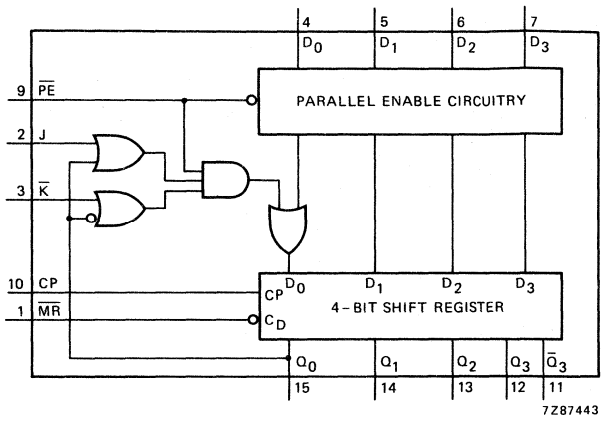


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd.)

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition.
There is no restriction on the activity of the J, $\overline{K}$, D_n and $\overline{PE}$ inputs for logic operation other than the set-up and hold time requirements. A LOW on the asynchronous master reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

APPLICATIONS

- **Serial data transfer**
- **Parallel data transfer**
- **Serial-to-parallel data transfer**
- **Parallel-to-serial data transfer**

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
shift, set first stage	H	↑	h	h	h	X	H	q0	q1	q2	$\overline{q}2$
shift, reset first stage	H	↑	h	l	l	X	L	q0	q1	q2	$\overline{q}2$
shift, toggle first stage	H	↑	h	h	l	X	$\overline{q}0$	q0	q1	q2	$\overline{q}2$
shift, retain first stage	H	↑	h	l	h	X	q0	q0	q1	q2	$\overline{q}2$
parallel load	H	↑	l	X	X	dn	d0	d1	d2	d3	$\overline{d}3$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q, d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

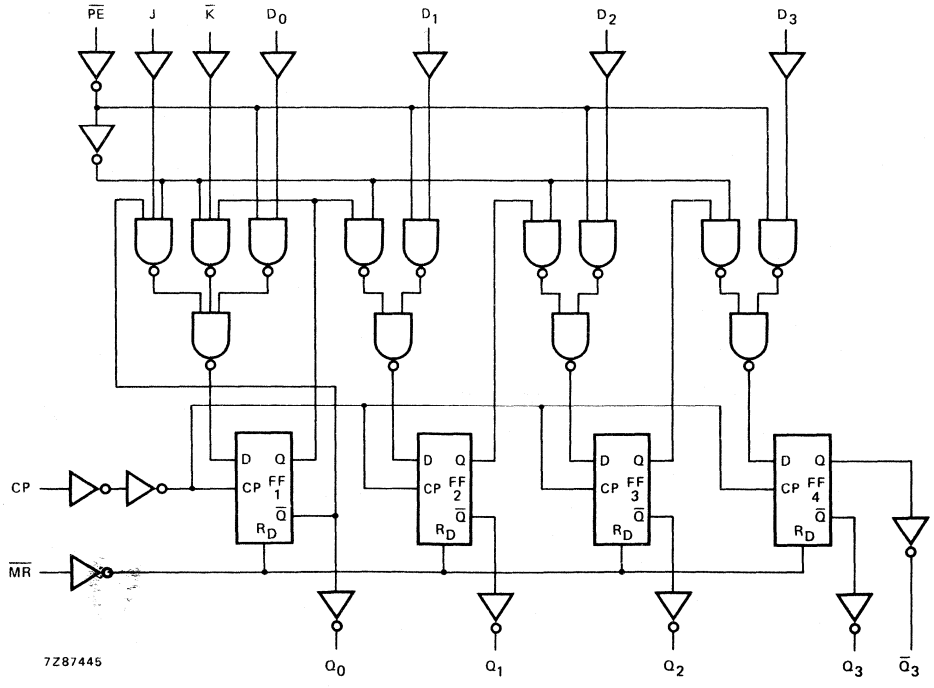


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$\overline{PE}$	0.65
all others	0.35

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time J, $\overline{K}$, $\overline{PE}$, D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs. 8 and 9
t_h	hold time J, $\overline{K}$, $\overline{PE}$, D_n to CP	3 3 3			3 3 3		3 3 3		ns	2.0 4.5 6.0	Figs. 8 and 9
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n			35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 6
t_W	master reset pulse width; LOW	20			25		30		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	16			20		24		ns	4.5	Fig. 7
t_{su}	set-up time J, $\overline{K}$, $\overline{PE}$, D_n to CP	20			25		30		ns	4.5	Figs. 8 and 9
t_h	hold time J, $\overline{K}$, $\overline{PE}$, D_n to CP	3			3		3		ns	4.5	Figs. 8 and 9
f_{max}	maximum clock pulse frequency	25			20		16		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

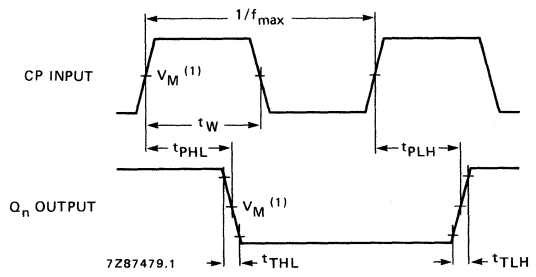


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

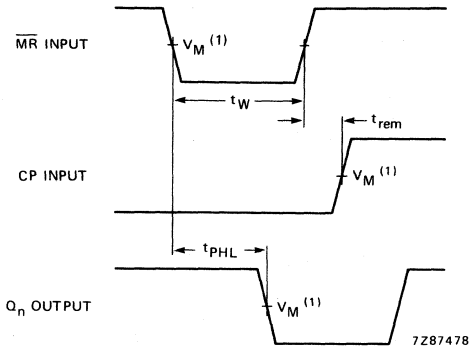


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time

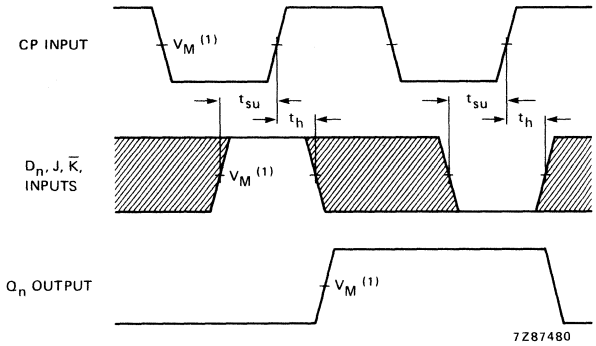


Fig. 8 Waveforms showing the data set-up and hold times for J, $\overline{K}$ and D_n inputs.

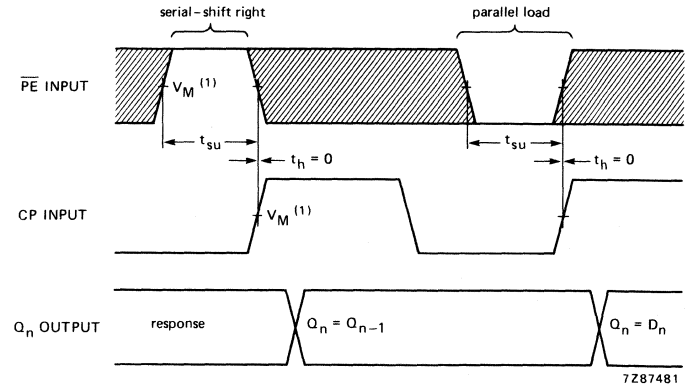


Fig. 9 Waveforms showing the set-up and hold times from the parallel enable input ($\overline{PE}$) to the clock (CP).

Note to Figs. 8 and 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

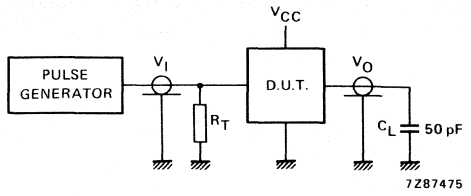


Fig. 10 Test circuit

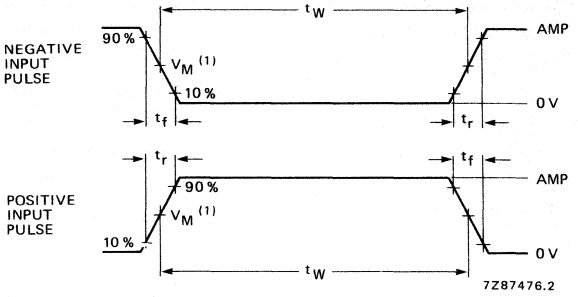


Fig. 11 Input pulse definitions

Definitions for Figs. 10 and 11:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- **Pulse width variance is typically less than ± 5%**
- **Pin-out identical to "123"**
- **Overriding reset terminates output pulse**
- **nB inputs have hysteresis for improved noise immunity**
- **Wide pulse range: 70 ns (typ) to ∞**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT221 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT221 are dual retriggerable monostable multivibrators. Each multivibrator features an active LOW-going edge input ($n\overline{A}$) and an active HIGH-going edge input (nB), either of which can be used as an enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the nB inputs allow jitter-free triggering from inputs with slow transition rates, providing the circuit with excellent noise immunity.

Once triggered, the outputs (nQ, $n\overline{Q}$) are independent of further transitions of $n\overline{A}$ and nB inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW reset inputs ($n\overline{R}_D$). Input pulses may be of any duration relative to the output pulse. The output pulse length may be varied from 35 ns to the maximum shown in the features by choosing appropriate timing components. With R_{EXT} = 2 kΩ and C_{EXT} = 28 pF, an output pulse of typical 70 ns is achieved which may be used as a DC triggered reset signal.

(continued on next page)

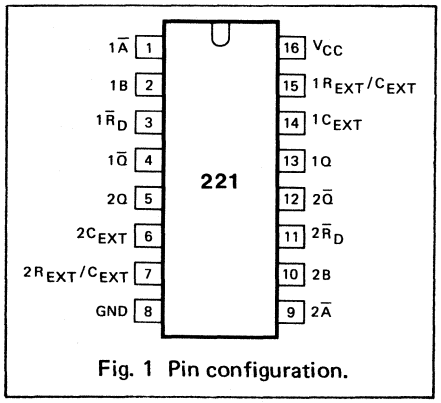


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB, $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 5 V R_{EXT} = 5 kΩ C_{EXT} = 0 pF	30	32	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C ; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT221P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT221D; PC74HC/HCT221D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT221T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset inputs (active LOW)
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

Note

It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

GENERAL DESCRIPTION (Cont'd)

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications pulse stability will only be limited by the accuracy of the external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than two decade of timing resistance (2 kΩ to any practical value) for the 54/74HC/HCT221.

Throughout these ranges the output pulse width is defined by the following relationship:

$$t_W = C_{EXT}R_{EXT}\ln 2$$

$$t_W = 0.7C_{EXT}R_{EXT}$$

In circuits where pulse cut-off is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used.

Pin assignments for the "221" are identical to those of the "123" so that the "221" can be substituted for those products in systems not using the retrigger by merely changing the value of R_{EXT} and/or C_{EXT}.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\bar{R}_D$	$n\bar{A}$	nB	nQ	$n\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎴
H	↓	H	⎍	⎴
↑	L	H	⎍	⎴

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH-level output pulse
⎴ = one LOW-level output pulse

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

1-TO-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

FEATURES

- **Combines 1-of-8 decoder with 3-bit latch**
- **Multiple input enable for easy expansion or independent controls**
- **Active HIGH mutually exclusive outputs**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT237 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT237 are 1-of-8 decoder/demultiplexers with latches at the three address inputs (A_n). The "237" essentially combines the 1-of-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the "237" acts as a 1-of-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs, before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable input ($\overline{E}_1$ and E_2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are LOW unless $\overline{E}_1$ is LOW and E_2 is HIGH.

The "237" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

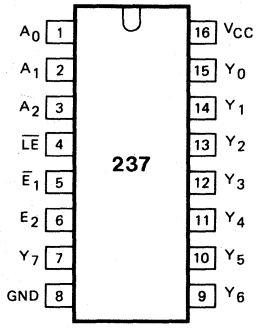


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT237P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT237D; PC74HC/HCT237D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT237T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	data inputs
4	$\overline{LE}$	latch enable input (active LOW)
5	$\overline{E}_1$	data enable input (active LOW)
6	E_2	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y_0 to Y_7	multiplexer outputs
16	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E_2	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	L	H	X	X	X	stable							
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

3-TO-8 LINE DECODER/DEMULTIPLEXER

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT238 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active HIGH outputs (Y_0 to Y_7).
The "238" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be LOW unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "238" to a 1-of-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter.

The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF; V_{CC} = 5 V	13	17	ns
t_{PHL}	E_3 to Y_n		15	19	ns
	$\overline{E}_n$ to Y_n		15	14	ns
t_{PLH}	E_3 to Y_n		15	22	ns
	$\overline{E}_n$ to Y_n				
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	72	76	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT238P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT238D; PC74HC/HCT238D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT238T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12 11, 10, 9, 7	Y_0 to Y_7	outputs (active HIGH)
16	V_{CC}	positive supply voltage

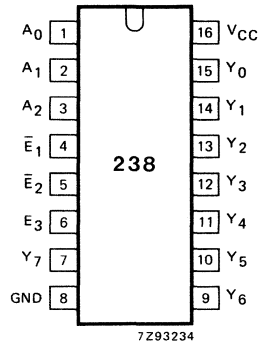


Fig. 1 Pin configuration.

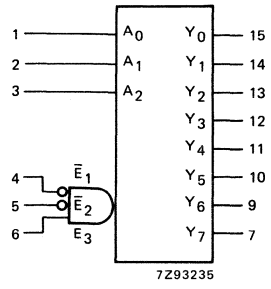


Fig. 2 Logic symbol.

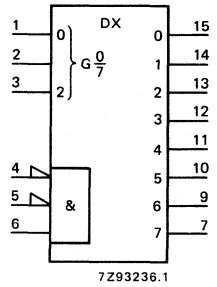


Fig. 3 IEC logic symbol.

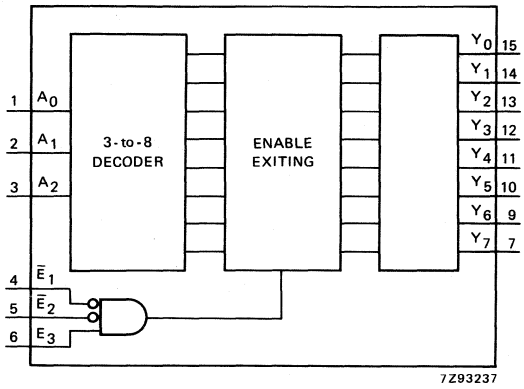


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

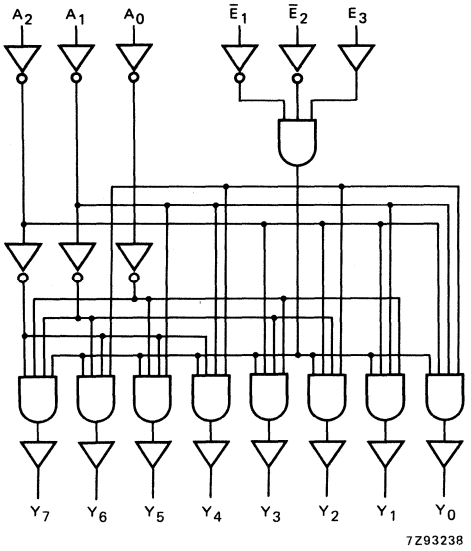


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		500	mW	for standard temperature range; −40 to +85 °C; 74HC/HCT above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		500	mW	for extended temperature range; −55 to +125°C; 54HC/HCT above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
A_n	0.70
$\overline{E}_n$	0.40
E_3	1.50

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay E_3 to Y_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_n$ to Y_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay A_n to Y_n			35		53		63	ns	4.5	Fig. 6
t_{PLH}	propagation delay A_n to Y_n			35		48		57	ns	4.5	Fig. 6
t_{PHL}	propagation delay E_3 to Y_n			40		60		72	ns	4.5	Fig. 6
t_{PLH}	propagation delay E_3 to Y_n			34		43		51	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{E}_n$ to Y_n			40		55		66	ns	4.5	Fig. 7
t_{PLH}	propagation delay $\overline{E}_n$ to Y_n			40		65		78	ns	4.5	Fig. 7
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

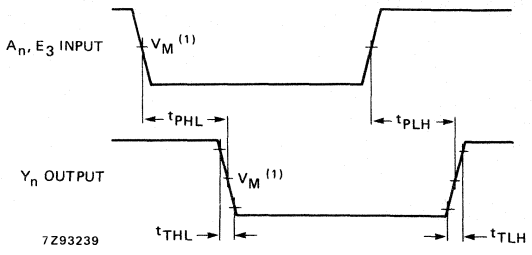


Fig. 6 Waveforms showing the address input (A_n) and enable input (E_3) to output (Y_n) propagation delays and the output transition times.

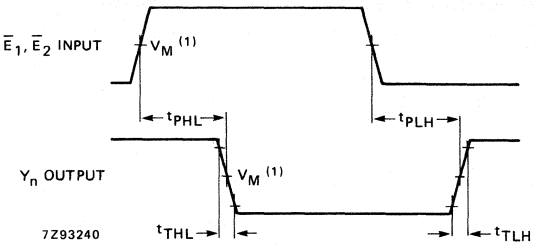


Fig. 7 Waveforms showing the enable input ($\overline{E}_n$) to output (Y_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

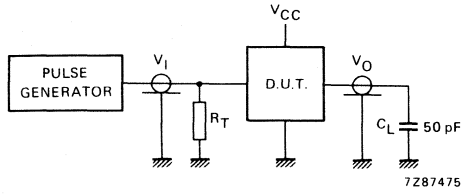


Fig. 8 Test circuit.

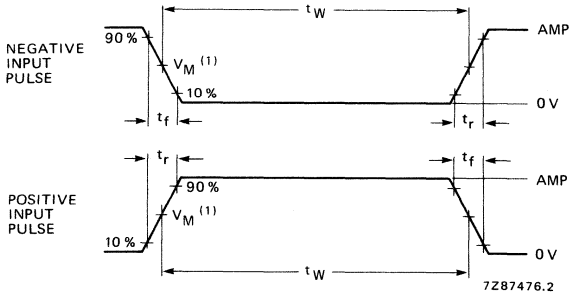


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT240 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT240 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "240" is identical to the "244" but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	9	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT240P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT240T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

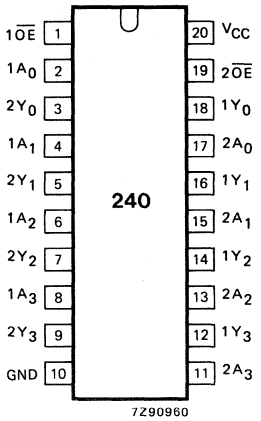


Fig. 1 Pin configuration.

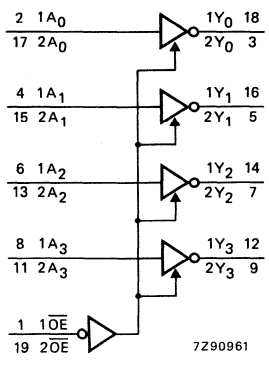


Fig. 2 Logic symbol.

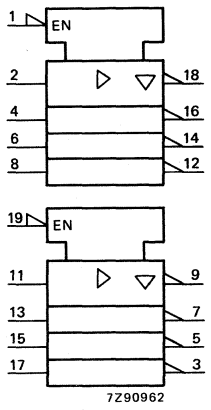


Fig. 3 IEC logic symbol.

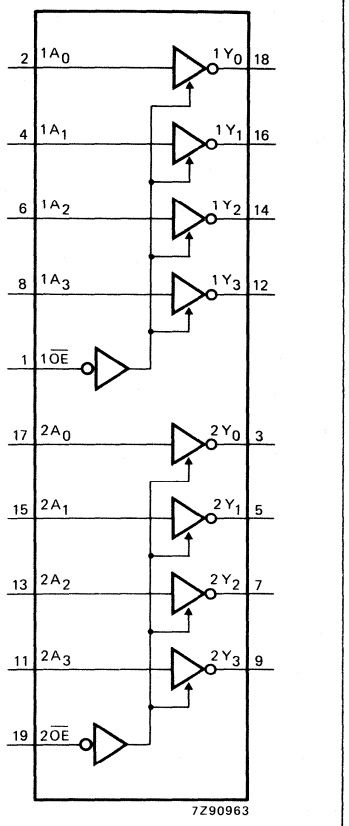


Fig. 4 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$1A_n$	1.50
$2A_n$	1.50
$1\overline{OE}$	0.70
$2\overline{OE}$	0.70

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$			110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$			22		28		33	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$			30		38		45	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$			30		38		45	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

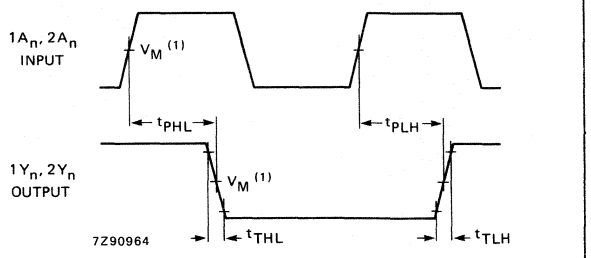


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

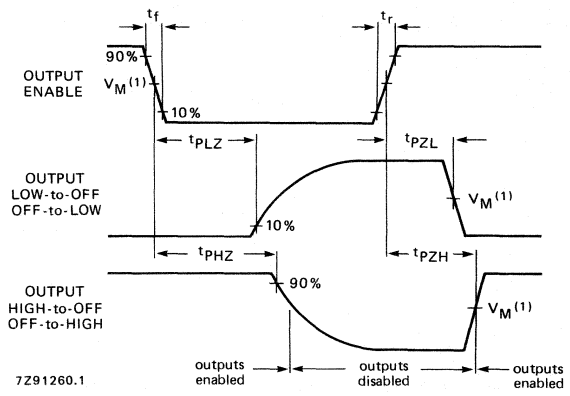


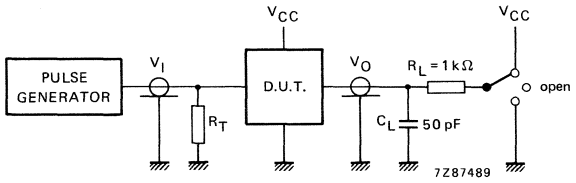
Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DEVELOPMENT DATA

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 7 Test circuit for 3-state outputs.

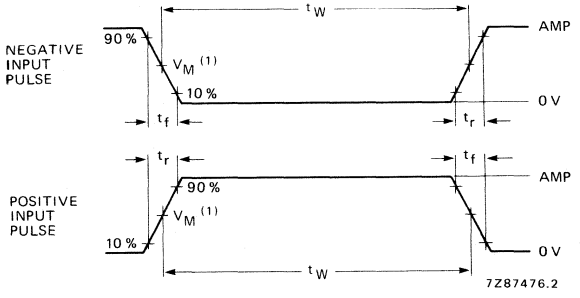


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT241 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The PC54/74HC/HCT241 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	$1A_n$	$1Y_n$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	$2A_n$	$2Y_n$
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT241P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT241T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	2OE	output enable input (active LOW)
20	V_{CC}	positive supply voltage

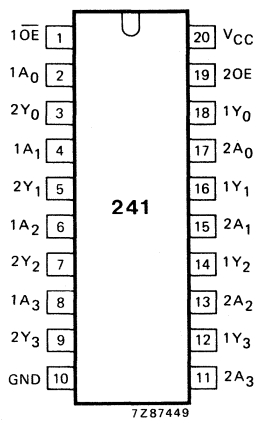


Fig. 1 Pin configuration.

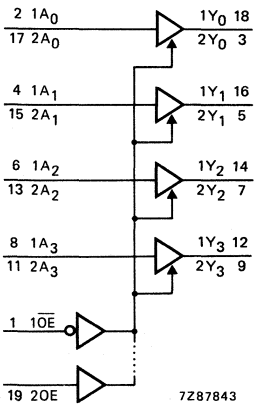


Fig. 2 Logic symbol.

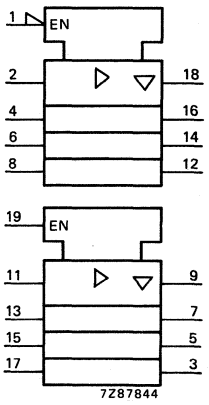


Fig. 3 IEC logic symbol.

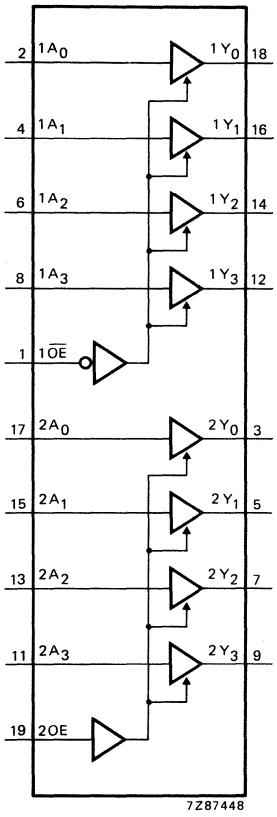


Fig. 4 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$1A_n$	0.70
$2A_n$	0.70
$1\overline{OE}$	0.70
2OE	1.50

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$			26		33		39	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$			38		48		57	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$			38		48		57	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

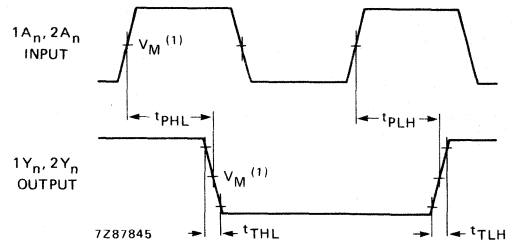


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

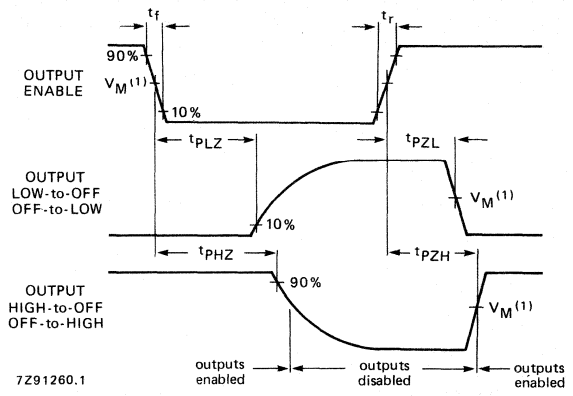
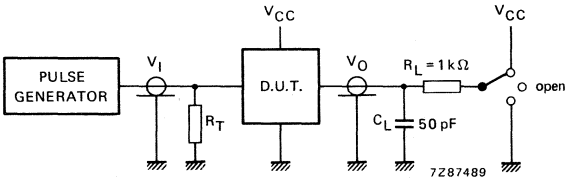


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 7 Test circuit for 3-state outputs.

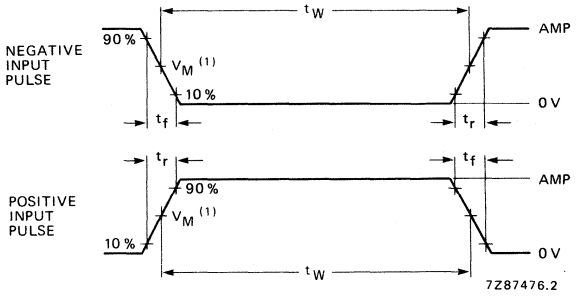


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD BUS TRANSCEIVER; 3-STATE; INVERTING

FEATURES

- Inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT242 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT242 are quad bus transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.
They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ($\overline{OE}_A$ and OE_B) can be used to isolate the buses.

The "242" is similar to the "243" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF; V_{CC} = 5 V	10	12	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	50	58	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT242P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT242D; PC74HC/HCT242D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT242T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_A$	output enable input (active LOW)
2, 12	n.c.	not connected
3, 4, 5, 6	A_0 to A_3	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	B_0 to B_3	data inputs/outputs
13	OE_B	output enable input
14	V_{CC}	positive supply voltage

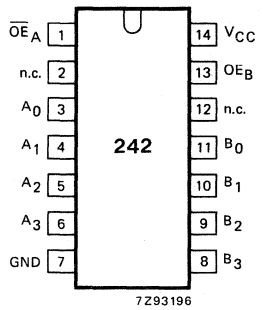


Fig. 1 Pin configuration.

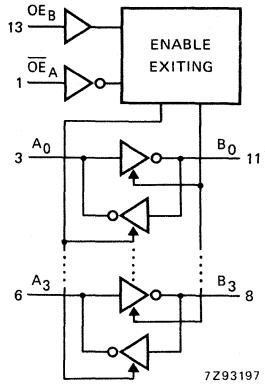


Fig. 2 Logic symbol.

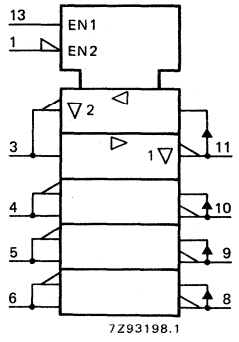


Fig. 3 IEC logic symbol.

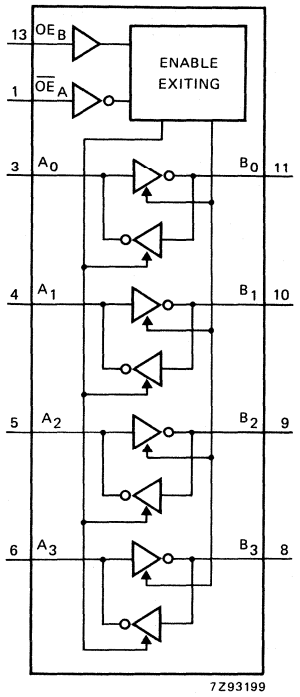


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	inputs	$B = \overline{A}$
H	L	Z	Z
L	H	Z	Z
H	H	$A = \overline{B}$	inputs

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current (note 1)			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

Note

1. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND. This is because an input stage is connected to the terminal permanently.

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current (note 2)			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.
2. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND.
   This is because an input stage is connected to the terminal permanently.

input	unit load coefficient
A_n	0.75
B_n	0.75
$\overline{OE}_A$	0.75
OE_B	0.75

AC CHARACTERISTICS FOR 54/74HC

GND =0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Figs 6 and 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Figs 6 and 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n			30		38		45	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n			45		56		68	ns	4.5	Figs 6 and 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n			45		56		68	ns	4.5	Figs 6 and 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

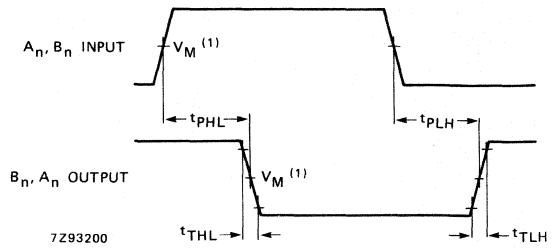


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

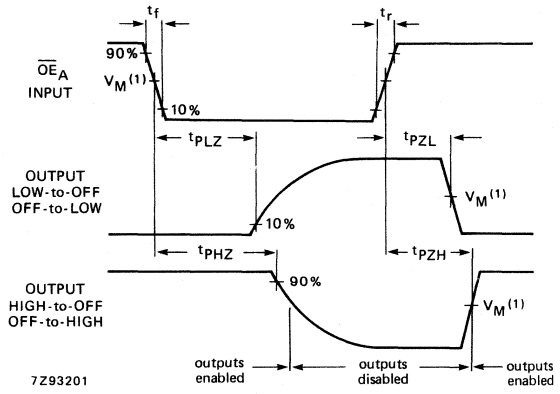


Fig. 6 Waveforms showing the 3-state enable and disable times for input $\overline{OE}_A$.

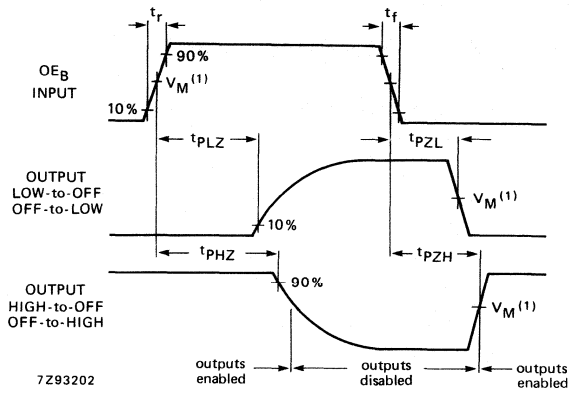
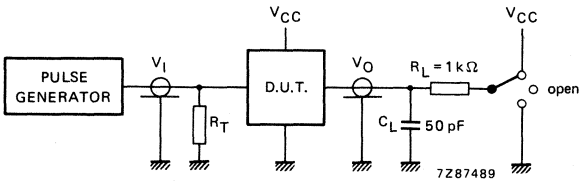


Fig. 7 Waveforms showing the 3-state enable and disable times for input OE_B.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 8 Test circuit for 3-state outputs.

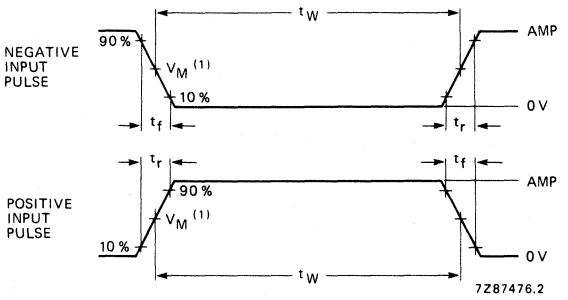


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD BUS TRANSCEIVER; 3-STATE

FEATURES

- Non-inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT243 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT243 are quad bus transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.
They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ($\overline{OE}_A$ and OE_B) can be used to isolate the buses.

The "243" is similar to the "242" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	50	54	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT243P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT243D; PC74HC/HCT243D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT243T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_A$	output enable input (active LOW)
2, 12	n.c.	not connected
3, 4, 5, 6	A_0 to A_3	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	B_0 to B_3	data inputs/outputs
13	OE_B	output enable input
14	V_{CC}	positive supply voltage

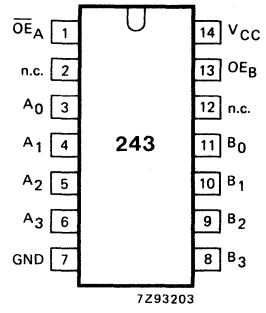


Fig. 1 Pin configuration.

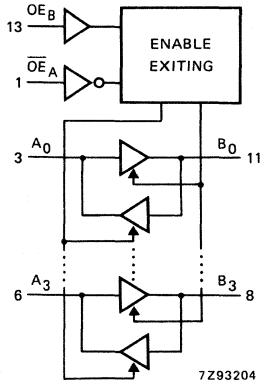


Fig. 2 Logic symbol.

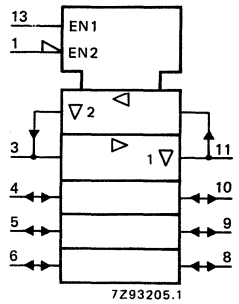


Fig. 3 IEC logic symbol.

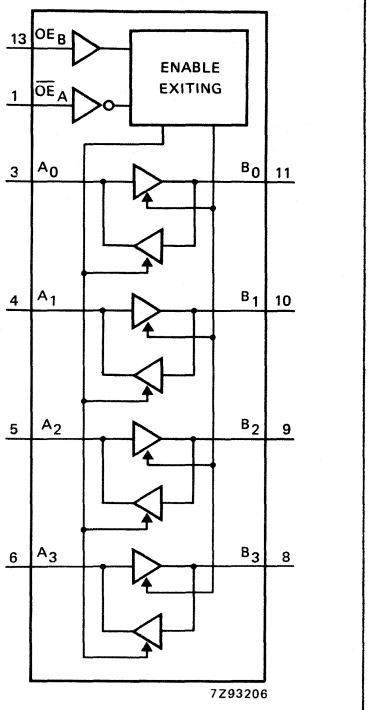


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	inputs	B = A
H	L	Z	Z
L	H	Z	Z
H	H	A = B	inputs

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current (note 1)			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

Note

1. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND. This is because an input stage is connected to the terminal permanently.

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
I_{CC}	quiescent supply current (note 2)			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
A_n	0.75
B_n	0.75
$\overline{OE}_A$	0.75
OE_B	0.75

2. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND.
   This is because an input stage is connected to the terminal permanently.

AC CHARACTERISTICS FOR 54/74HC

GND =0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n			110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Figs 6 and 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Figs 6 and 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n			27		34		41	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n			45		56		68	ns	4.5	Figs 6 and 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n			45		56		68	ns	4.5	Figs 6 and 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

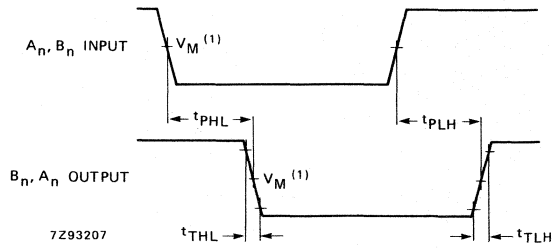


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

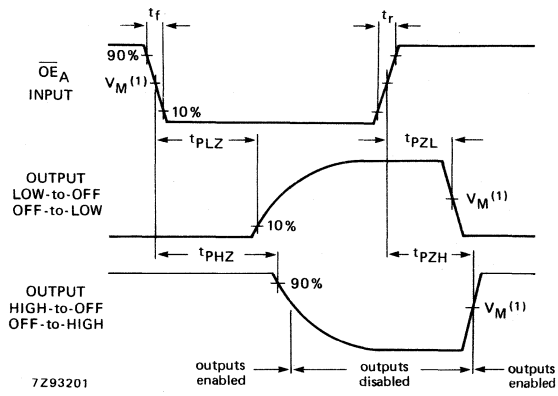


Fig. 6 Waveforms showing the 3-state enable and disable times for input $\overline{OE}_A$.

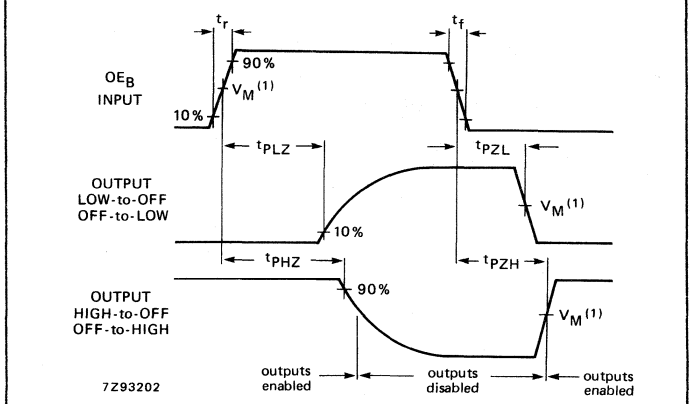
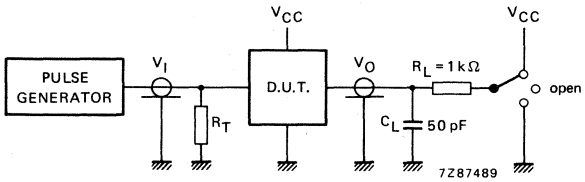


Fig. 7 Waveforms showing the 3-state enable and disable times for input OE_B.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 8 Test circuit for 3-state outputs.

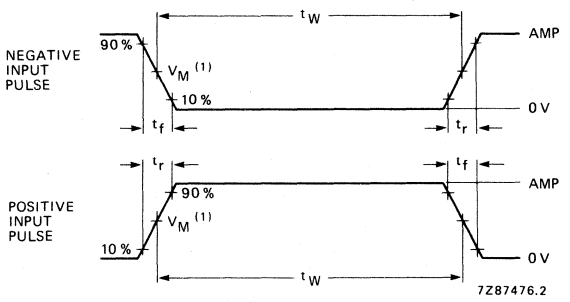


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT244 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT244 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.
The "244" is identical to the "240" but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	9	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT244P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT244T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

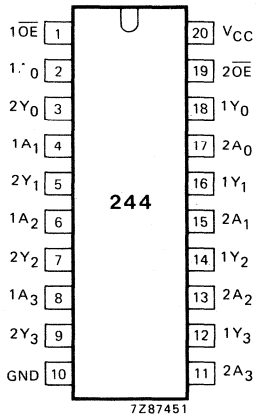


Fig. 1 Pin configuration.

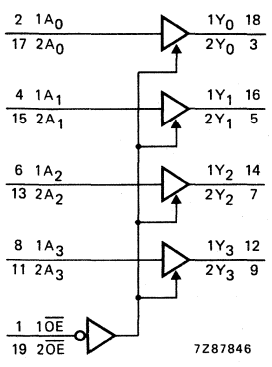


Fig. 2 Logic symbol.

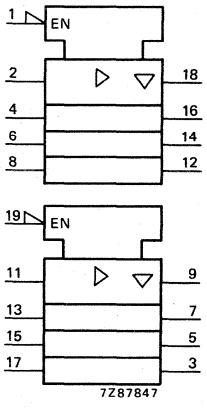


Fig. 3 IEC logic symbol.

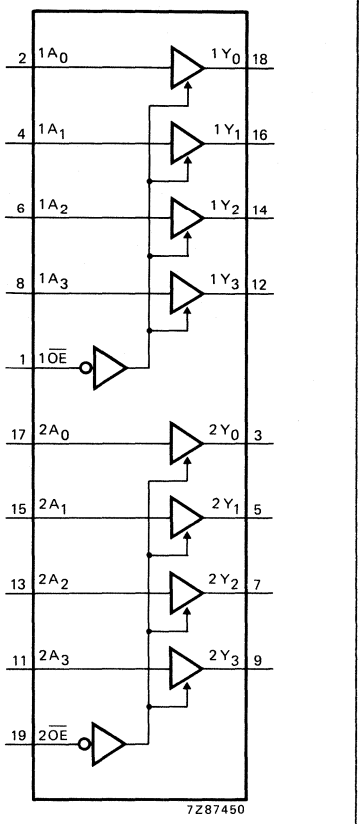


Fig. 4 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$1A_n$	0.70
$2A_n$	0.70
$1\overline{OE}$	0.70
$2\overline{OE}$	0.70

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$			110 22 19		145 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$			26		33		39	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$			30		38		45	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$			30		38		45	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

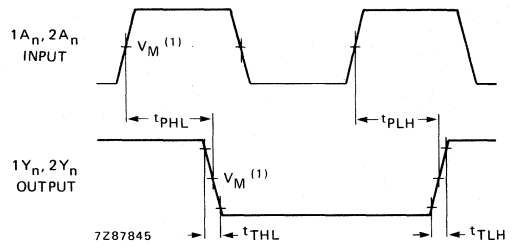


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

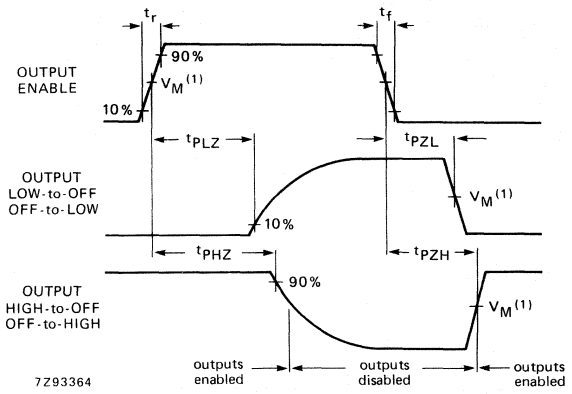
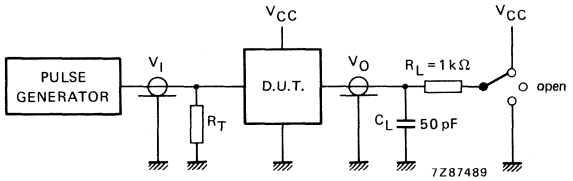


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 7 Test circuit for 3-state outputs.

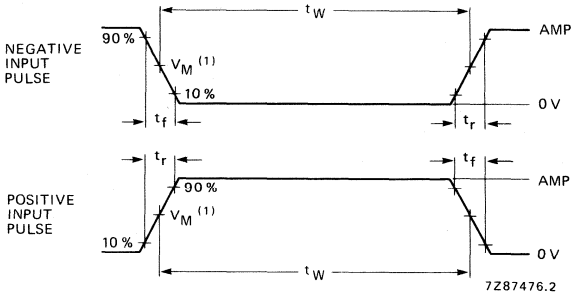


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

OCTAL BUS TRANSCEIVER; 3-STATE

FEATURES

- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.
The "245" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.
The "245" is similar to the "640" but has true (non-inverting) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n	C_L = 15 pF; V_{CC} = 5 V	8	9	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT245P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT245T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

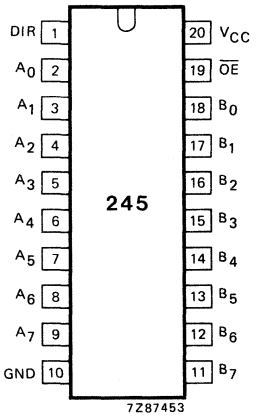


Fig. 1 Pin configuration.

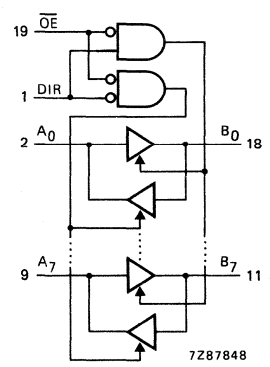


Fig. 2 Logic symbol.

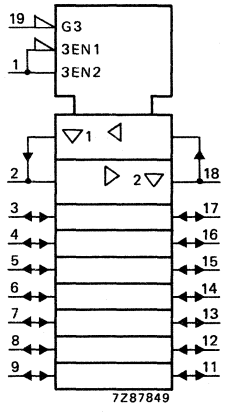


Fig. 3 IEC logic symbol.

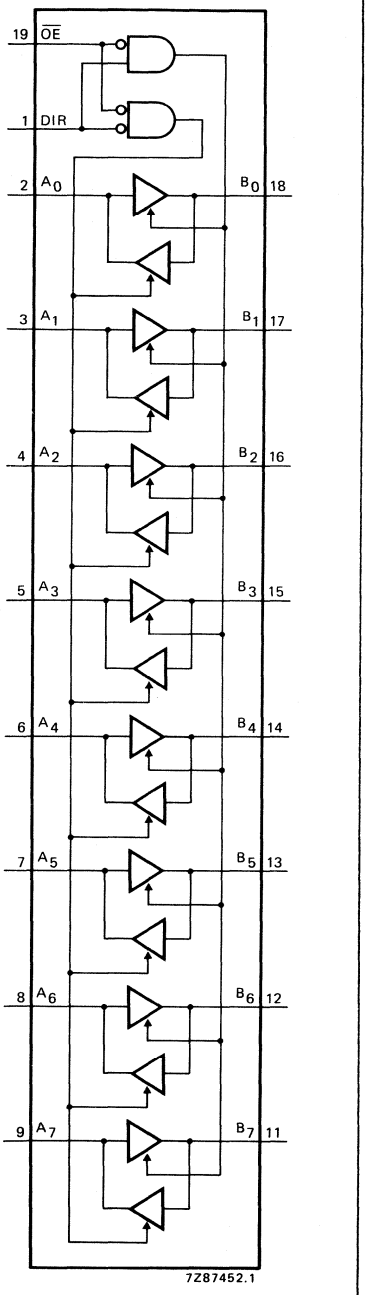


Fig. 4 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current A_n and B_n			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current (note 1)			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

Note

1. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND.
   This is because an input stage is connected to the terminal permanently.

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current A_n and B_n			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current (note 2)			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.
2. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND.
   This is because an input stage is connected to the terminal permanently.

input	unit load coefficient
A_n	0.40
B_n	0.40
$\overline{OE}$	1.50
DIR	0.90

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n			24		30		36	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n			30		38		45	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n			30		38		45	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

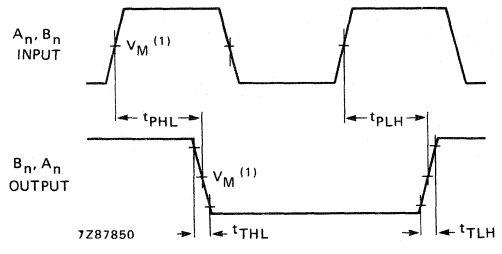


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

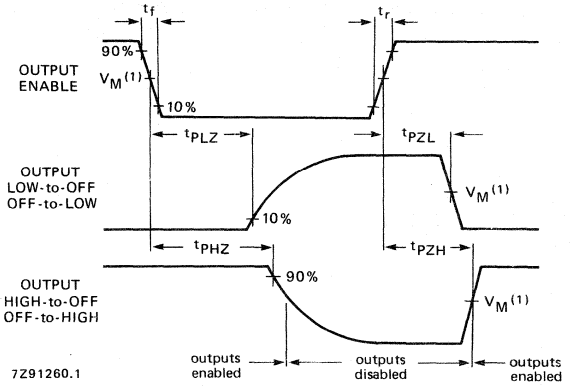
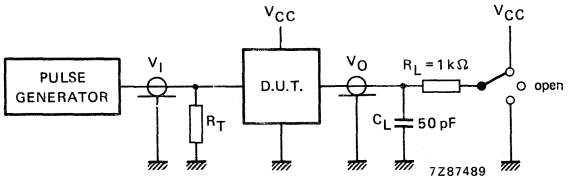


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 7 Test circuit for 3-state outputs.

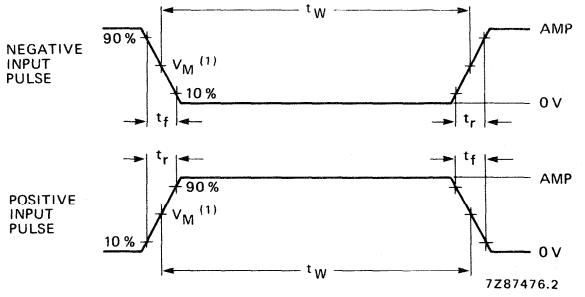


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

8-INPUT MULTIPLEXER; 3-STATE

FEATURES

- True and complement outputs
- Both outputs are 3-state for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT251 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT251 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S_0, S_1, S_2) controlling the switch positions.
Assertion (Y) and negation ($\overline{Y}$) outputs are both provided.
The output enable input ($\overline{OE}$) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \overline{OE}.(I_0.\overline{S}_0.\overline{S}_1.\overline{S}_2 + I_1.S_0.\overline{S}_1.\overline{S}_2 + I_2.\overline{S}_0.S_1.\overline{S}_2 + I_3.S_0.S_1.\overline{S}_2 + I_4.\overline{S}_0.\overline{S}_1.S_2 + I_5.S_0.\overline{S}_1.S_2 + I_6.\overline{S}_0.S_1.S_2 + I_7.S_0.S_1.S_2)$$

Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to Y I_n to $\overline{Y}$ S_n to Y S_n to $\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	 14 16 20 22	 18 18 25 25	 ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	42	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT251P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT251D; PC74HC/HCT251D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT251T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	$\overline{Y}$	complementary multiplexer output
7	$\overline{OE}$	3-state output enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage

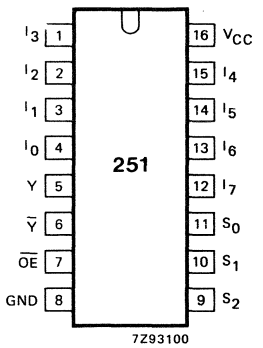


Fig. 1 Pin configuration.

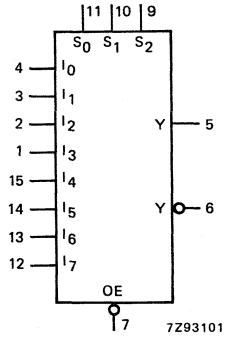


Fig. 2 Logic symbol.

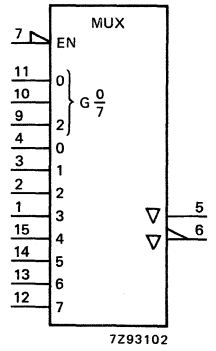


Fig. 3 IEC logic symbol.

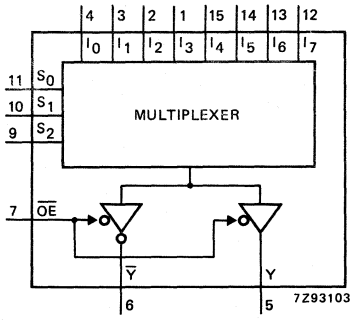


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

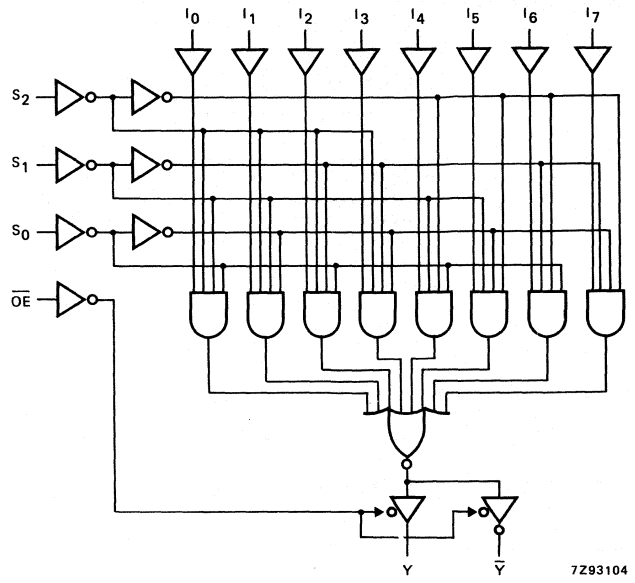


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
I_n	0.55
S_0	0.55
S_1, S_2	0.55
$\overline{OE}$	2.65

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Y			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to $\overline{Y}$			190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_n to Y			240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to $\overline{Y}$			325 52 44		325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Y, $\overline{Y}$			110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Y, $\overline{Y}$			140 28 24		170 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Y			42		53		65	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to $\overline{Y}$			42		53		65	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_n to Y			58		73		87	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to $\overline{Y}$			58		73		87	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Y, $\overline{Y}$			30		38		45	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Y, $\overline{Y}$			28		35		42	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

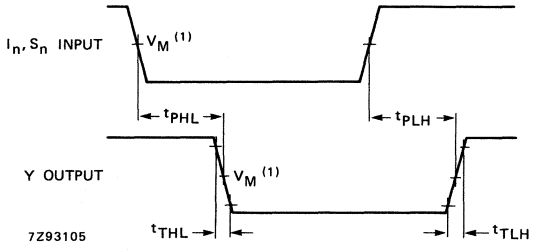


Fig. 6 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output (Y) propagation delays and the output transition times.

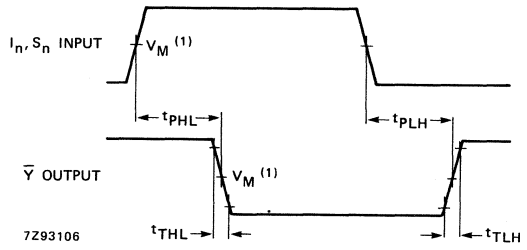


Fig. 7 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output ($\overline{Y}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

AC WAVEFORMS

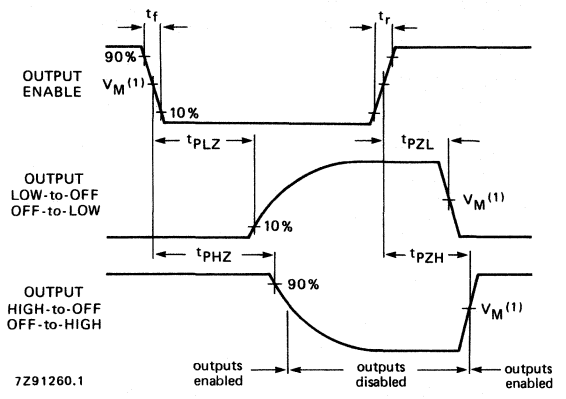
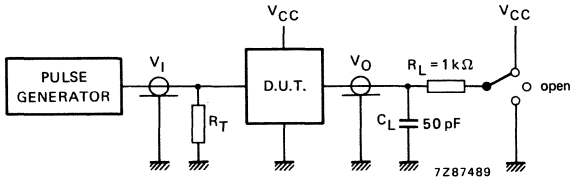


Fig. 8 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 9 Test circuit for 3-state outputs.

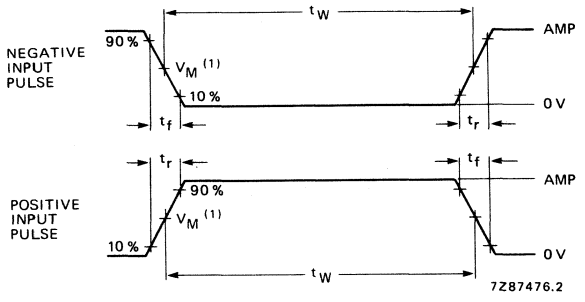


Fig. 10 Input pulse definitions.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DUAL 4-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Non-inverting data path
- 3-state outputs for bus interface and multiplex expansion
- Common select inputs
- Separate output enable inputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT253 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT253 have two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common data select inputs (S_0, S_1).

When the individual output enable ($1\overline{OE}$, $2\overline{OE}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to the high impedance OFF-state.

The "253" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S_0 and S_1.

The logic equations for the outputs are:

$$1Y = 1\overline{OE}(1I_0.\overline{S}_1.\overline{S}_0+1I_1.\overline{S}_1.S_0+ +1I_2.S_1.\overline{S}_0+1I_3.S_1.S_0)$$

$$2Y = 2\overline{OE}(2I_0.\overline{S}_1.\overline{S}_0+2I_1.\overline{S}_1.S_0+ +2I_2.S_1.\overline{S}_0+2I_3.S_1.S_0)$$

APPLICATIONS

- Data selectors
- Data multiplexers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1I_n$, $2I_n$ to nY; S_n to nY	C_L = 15 pF; V_{CC} = 5 V	17	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	55	55	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT253P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT253D; PC74HC/HCT253D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT253T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
7, 9	1Y, 2Y	3-state multiplexer outputs
8	GND	ground (0 V)
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage

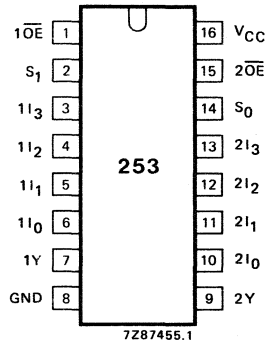


Fig. 1 Pin configuration.

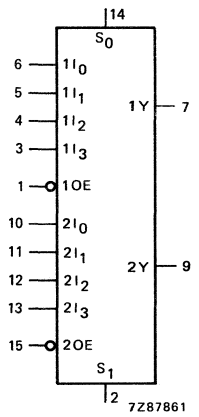


Fig. 2 Logic symbol.

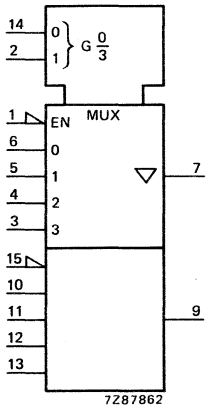


Fig. 3 IEC logic symbol.

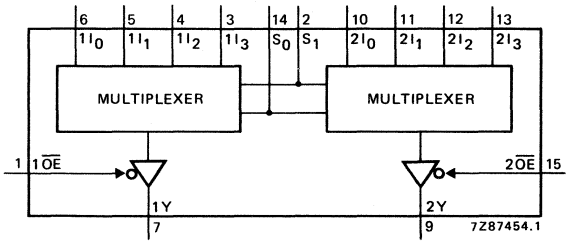


Fig. 4 Functional diagram.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	nI_0	nI_1	nI_2	nI_3	$n\overline{OE}$	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

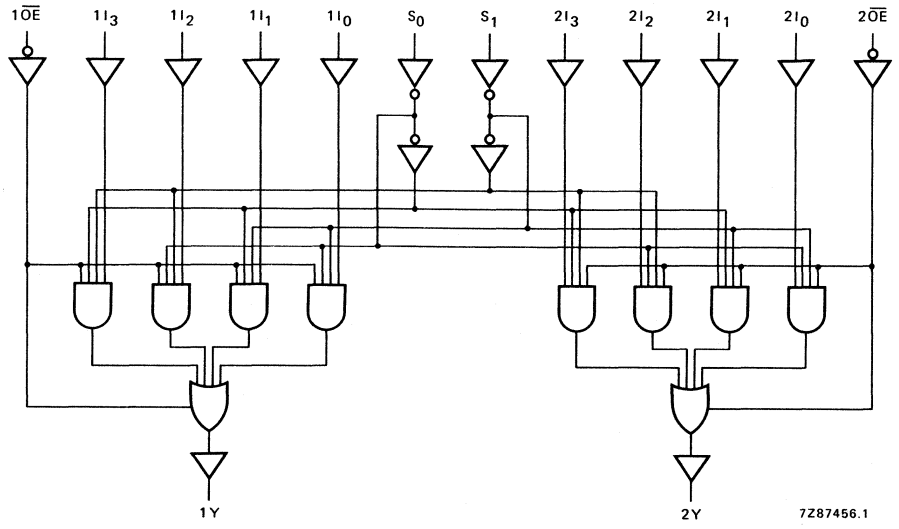


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$1I_n$	0.35
$2I_n$	0.35
$n\overline{OE}$	1.00
S_0	1.00
S_1	1.00

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to nY			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY			40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to nY			40		50		60	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY			30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY			30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

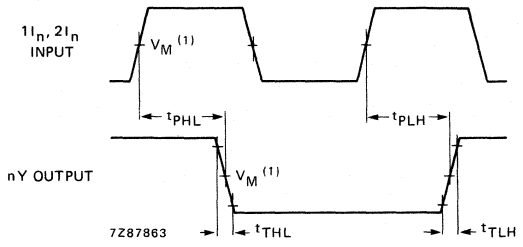


Fig. 6 Waveforms showing the input ($1I_n$, $2I_n$) to output (1Y, 2Y) propagation delays and the output transition times.

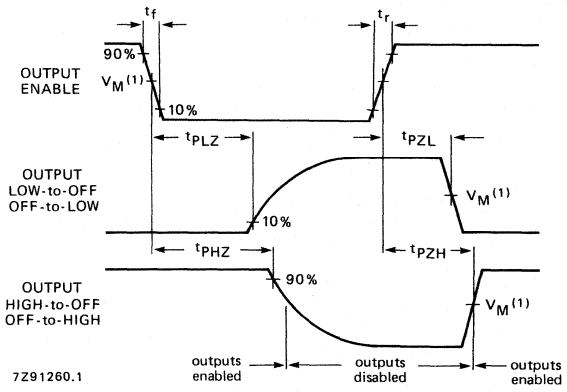
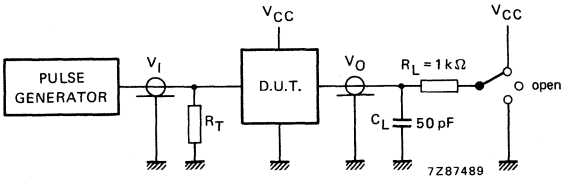


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 8 Test circuit for 3-state outputs.

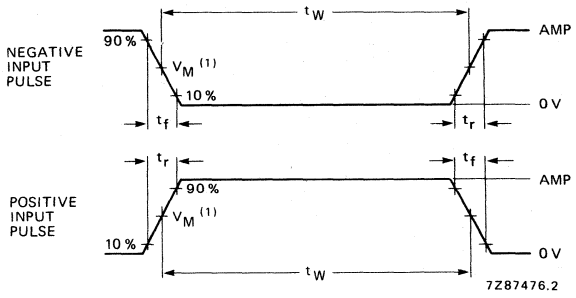


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

QUAD 2-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT257 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT257 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH.

Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the select inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$1Y = \overline{OE}.(1I_1.S + 1I_0.\overline{S})$

$2Y = \overline{OE}.(2I_1.S + 2I_0.\overline{S})$

$3Y = \overline{OE}.(3I_1.S + 3I_0.\overline{S})$

$4Y = \overline{OE}.(4I_1.S + 4I_0.\overline{S})$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY S to nY	C_L = 15 pF V_{CC} = 5 V	12 14	12 14	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	45	45	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT257P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT257D; PC74HC/HCT257D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT257T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 14, 11	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 13, 10	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 12, 9	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage

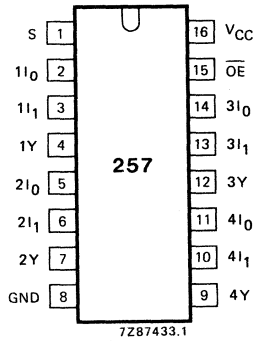


Fig. 1 Pin configuration.

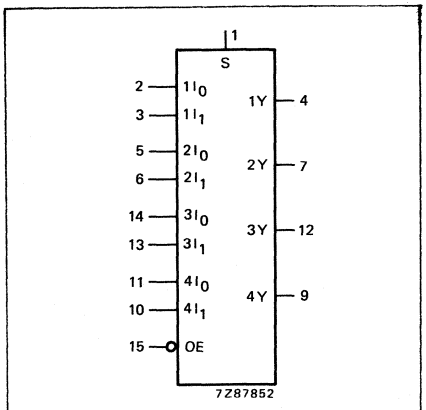


Fig. 2 Logic symbol.

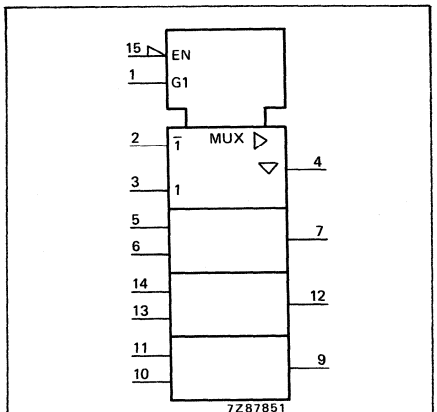


Fig. 3 IEC logic symbol.

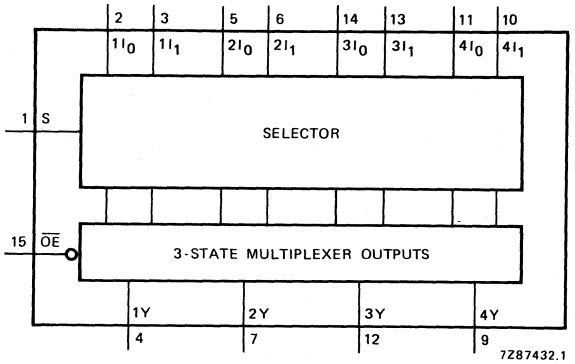


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

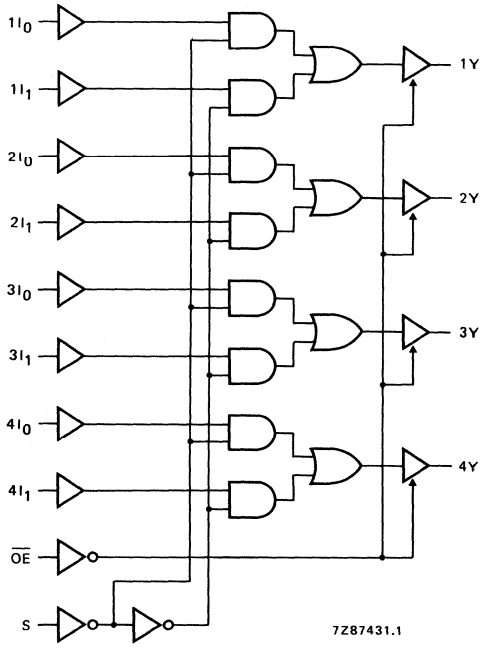


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nI_0	0.40
nI_1	0.40
$\overline{OE}$	1.35
S	0.65

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY			130 26 22		165 33 28		225 39 33	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to nY			135 35 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY			30		38		45	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to nY			35		44		53	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY			30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY			30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

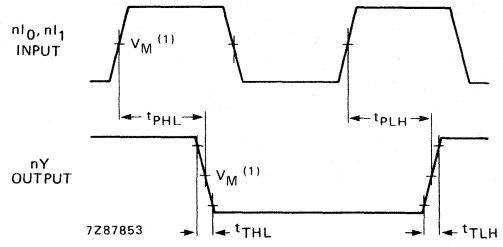


Fig. 6 Waveforms showing the input (nI_0, nI_1) to output (nY) propagation delays and the output transition times.

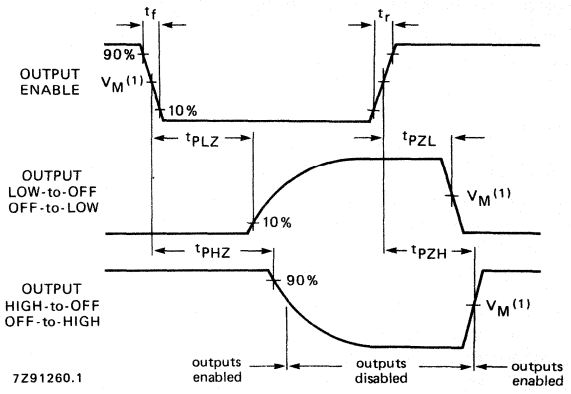
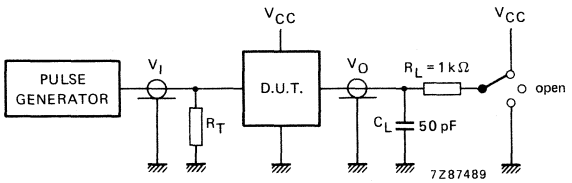


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 8 Test circuit for 3-state outputs.

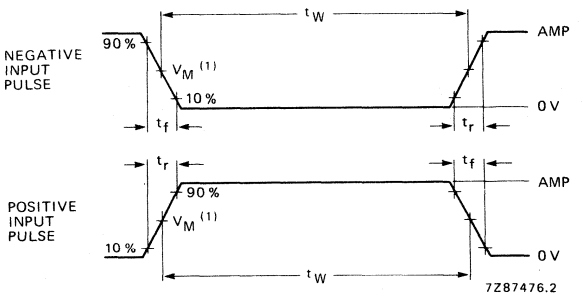


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

QUAD 2-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT258 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT258 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH.

Data appears at the outputs ($1\overline{Y}$ to $4\overline{Y}$) in inverted form from the select inputs.

The "258" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$$1\overline{Y} = \overline{\overline{OE}.(1I_1.S + 1I_0.\overline{S})}$$
$$2\overline{Y} = \overline{\overline{OE}.(2I_1.S + 2I_0.\overline{S})}$$
$$3\overline{Y} = \overline{\overline{OE}.(3I_1.S + 3I_0.\overline{S})}$$
$$4\overline{Y} = \overline{\overline{OE}.(4I_1.S + 4I_0.\overline{S})}$$

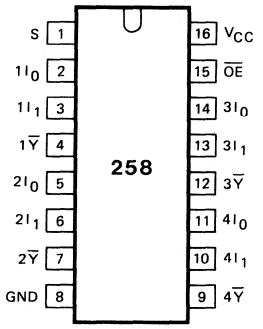


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1, S to $n\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	14	16	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT258P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT258D; PC74HC/HCT258D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT258T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 14, 11	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 13, 10	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 12, 9	$1\overline{Y}$ to $4\overline{Y}$	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	$n\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

8-BIT ADDRESSABLE LATCH

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 1-to-8 active HIGH decoder
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT259 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The "259" are multifunctional devices capable of storing single-line data in eight addressable latches, and also 1-to-8 decoder and demultiplexer, with active HIGH outputs (Q_0 to Q_7), functions are available.

The "259" also incorporates an active LOW common reset ($\overline{MR}$) for resetting all latches, as well as, an active LOW enable input ($\overline{LE}$).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D to Q_n	C_L = 15 pF; V_{CC} = 5 V	17	18	ns
	A_n, $\overline{LE}$ to Q_n		16	18	ns
t_{PHL}	$\overline{MR}$ to Q_n		15	19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT259P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT259D; PC74HC/HCT259D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT259T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5, 6, 7, 9 10, 11, 12	Q_0 to Q_7	latch outputs
8	GND	ground (0 V)
13	D	data input
14	$\overline{LE}$	latch enable input (active LOW)
15	$\overline{MR}$	conditional reset input (active LOW)
16	V_{CC}	positive supply voltage

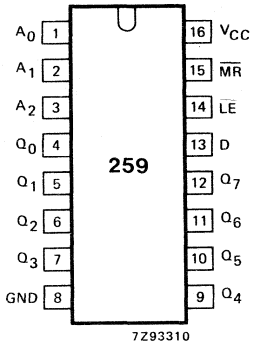


Fig. 1 Pin configuration.

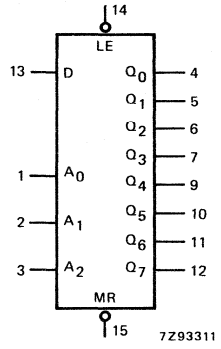


Fig. 2 Logic symbol.

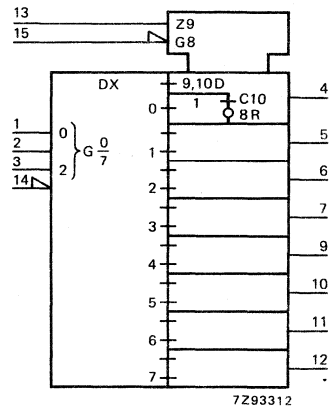


Fig. 3 IEC logic symbol.

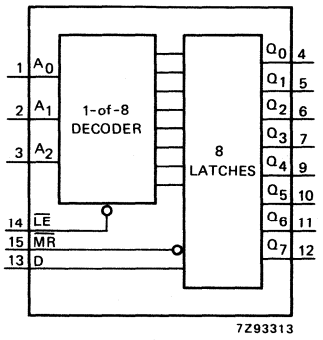


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd.)

The "259" has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 1-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A_0 to A_2) and data (D) input. When operating the "259" as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the "259".

MODE SELECT TABLE

$\overline{LE}$	$\overline{MR}$	MODE
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{LE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
addressable latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	H	L	q_0	q_1	q_2	Q=d	q_4	q_5	q_6	q_7
	H	L	d	L	L	H	q_0	q_1	q_2	q_3	Q=d	q_5	q_6	q_7
	H	L	d	H	L	H	q_0	q_1	q_2	q_3	q_4	Q=d	q_6	q_7
	H	L	d	L	H	H	q_0	q_1	q_2	q_3	q_4	q_5	Q=d	q_7
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

H = HIGH voltage level
L = LOW voltage level
X = don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{LE}$ transition
q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

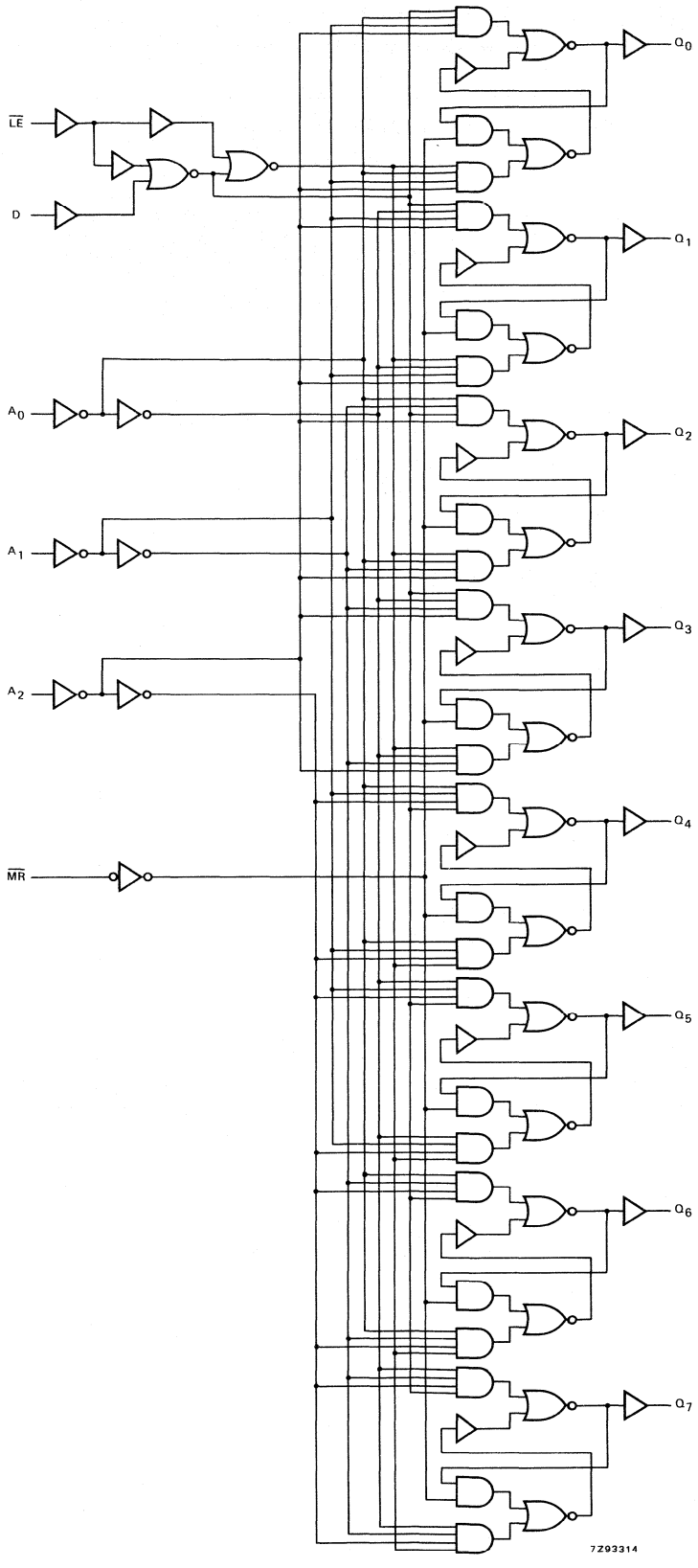


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		500	mW	for standard temperature range; −40 to +85 °C; 74HC/HCT above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		500	mW	for extended temperature range; −55 to +125°C; 54HC/HCT above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
A_n	1.50
$\overline{LE}$	1.50
D	1.20
$\overline{MR}$	0.75

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D to Q_n			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n			195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Q_n			195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		119 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t_W	$\overline{LE}$ pulse width HIGH or LOW	70 14 12			90 18 15		105 21 12		ns	2.0 4.5 6.0	Fig. 6
t_W	$\overline{MR}$ pulse width LOW	70 14 12			90 18 15		105 21 12		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D, A_n to $\overline{LE}$	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11
t_h	hold time D to $\overline{LE}$	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time A_n to $\overline{LE}$	2 2 2			2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 11

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D to Q_n			44		55		66	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n			43		54		65	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Q_n			44		55		66	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n			45		56		68	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7
t_W	$\overline{LE}$ pulse width HIGH or LOW	22			28		33		ns	4.5	Fig. 6
t_W	$\overline{MR}$ pulse width LOW	20			25		30		ns	4.5	Fig. 9
t_{su}	set-up time D to $\overline{LE}$	20			25		30		ns	4.5	Fig. 10
t_{su}	set-up time A_n to $\overline{LE}$	22			28		33		ns	4.5	Fig. 11
t_h	hold time D to $\overline{LE}$	0			0		0		ns	4.5	Fig. 10
t_h	hold time A_n to $\overline{LE}$	0			0		0		ns	4.5	Fig. 11

AC WAVEFORMS

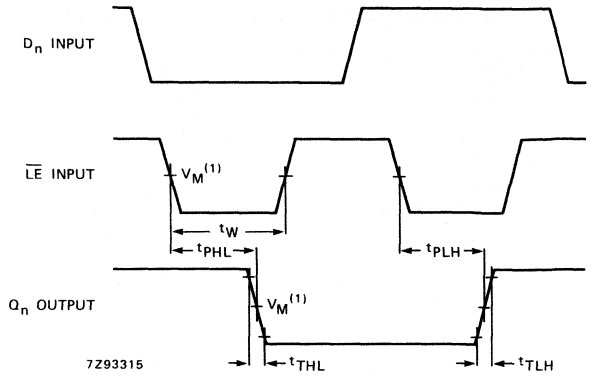


Fig. 6 Waveforms showing the enable input ($\overline{LE}$) to output (Q_n) propagation delays, the enable input pulse width and the output transition times.

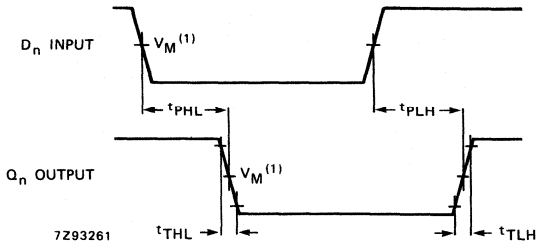


Fig. 7 Waveforms showing the data input (D) to output (Q_n) propagation delays and the output transition times.

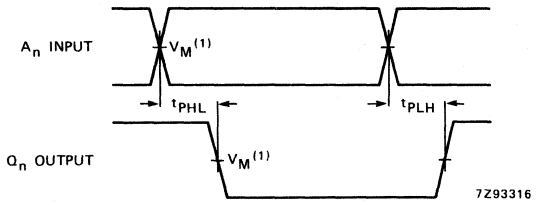


Fig. 8 Waveforms showing the address inputs (A_n) to outputs (Q_n) propagation delays and the output transition times.

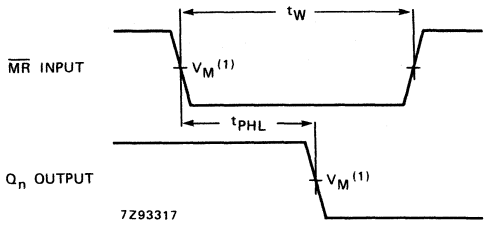


Fig. 9 Waveforms showing the conditional reset input ($\overline{MR}$) to output (Q_n) propagation delays.

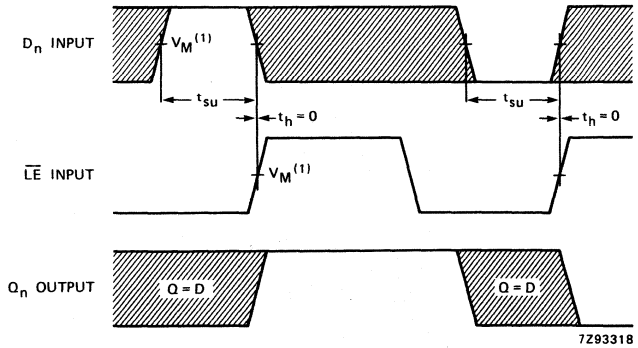


Fig. 10 Waveforms showing the data set-up and hold times for D input to $\overline{LE}$ input.

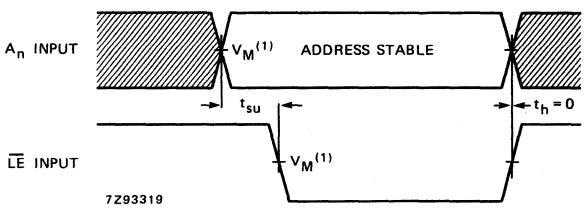


Fig. 11 Waveforms showing the address set-up and hold times for A_n inputs to $\overline{LE}$ input.

Note to Figs 10 and 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

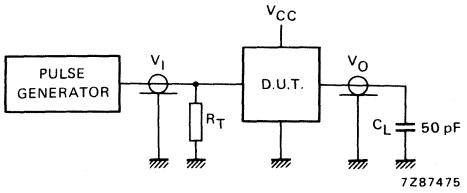


Fig. 12 Test circuit.

Definitions for Figs 12 and 13:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

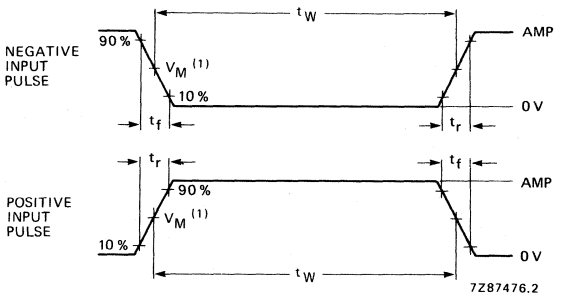


Fig. 13 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD 2-INPUT EXCLUSIVE-NOR GATE

FEATURES

- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC7266 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC7266 provide the EXCLUSIVE-NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	8	ns
C_I	input capacitance		3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC7266P: 14-lead DIL; plastic (SOT-27).
PC54HC7266D; PC74HC7266D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC7266T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 6, 8, 13	1A to 4A	data inputs
2, 5, 9, 12	1B to 4B	data inputs
3, 4, 10, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

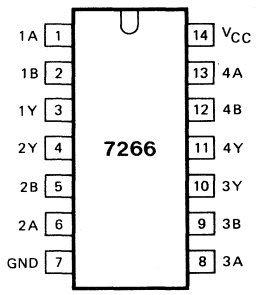


Fig. 1 Pin configuration.

OCTAL D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- **Ideal buffer for MOS microprocessor or memory**
- **Common clock and master reset**
- **Eight positive edge-triggered D-type flip-flops**
- **See "377" for clock enable version**
- **See "373" for transparent latch version**
- **See "374" for 3-state version**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	13 14	15 18	ns ns
f_{max}	maximum clock frequency		58	36	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	23	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT273P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT273T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

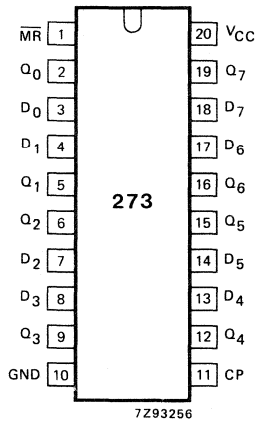


Fig. 1 Pin configuration.

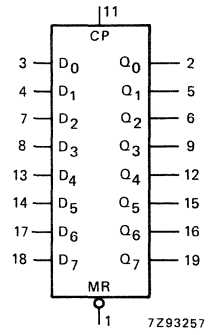


Fig. 2 Logic symbol.

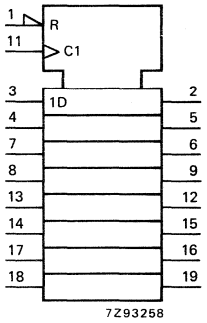


Fig. 3 IEC logic symbol.

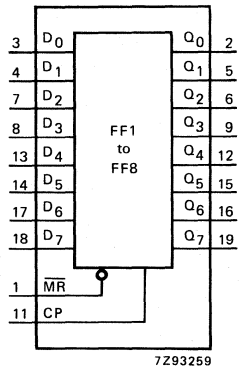


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	L
load "0"	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH transition
X = don't care

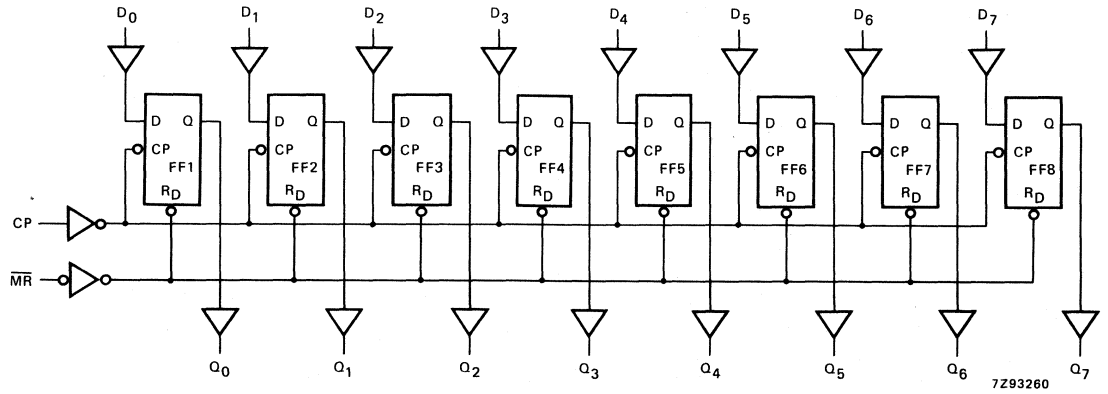


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$\overline{MR}$	1.00
CP	1.75
D_n	0.15

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time CP to D_n	3 3 3			3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			37		46		56	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n			43		54		65	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	26			33		39		ns	4.5	Fig. 6
t_W	master reset pulse width LOW	20			25		30		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	15			19		22		ns	4.5	Fig. 7
t_{su}	set-up time D_n to CP	20			25		30		ns	4.5	Fig. 8
t_h	hold time CP to D_n	3			3		3		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	19			15		13		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

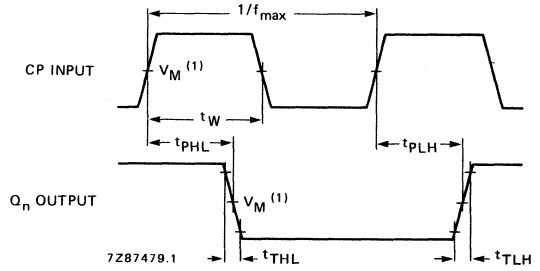


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.

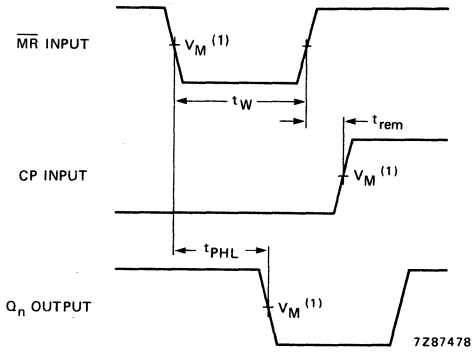


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

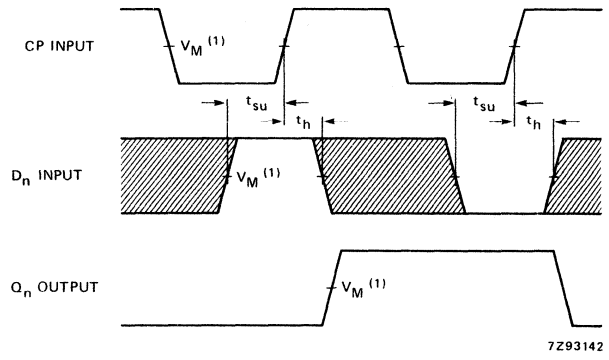


Fig. 8 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

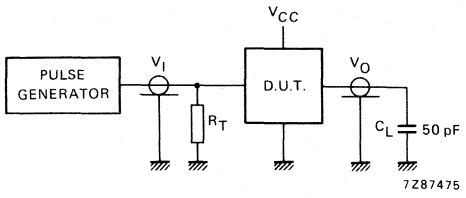


Fig. 9 Test circuit.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

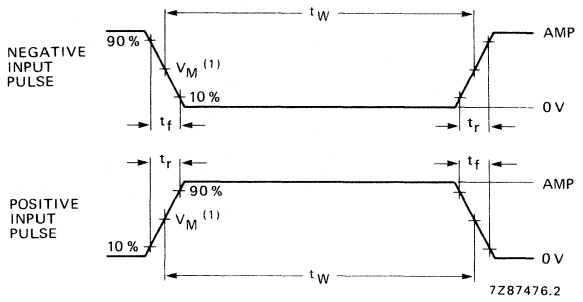


Fig. 10 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

FEATURES

- **Word-length easily expanded by cascading**
- **Similar pin configuration to the "180" for easy system up-grading**
- **Generates either odd or even parity for nine data bits**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT280 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT280 are 9-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems. Both even and odd parity outputs are available for generating or checking even or odd parity up to 9 bits.

The even parity output (Σ_E) is HIGH when an even number of data inputs (I_0 to I_8) are HIGH. The odd parity output (Σ_O) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the even outputs (Σ_E) of up to nine parallel devices to the data inputs of the final stage.

APPLICATIONS

- **25-line parity generator/checker**
- **81-line parity generator/checker**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to Σ_E I_n to Σ_O	C_L = 15 pF V_{CC} = 5 V	 17 17	 19 18	 ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	65	65	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT280P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT280D; PC74HC/HCT280D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT280T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 9, 10, 11, 12, 13, 1, 2, 4	I_0 to I_8	data inputs
5, 6	Σ_E, Σ_O	parity outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

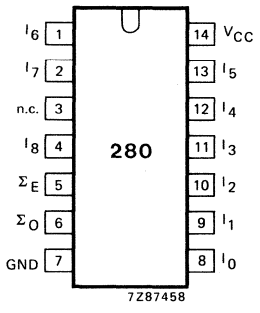


Fig. 1 Pin configuration.

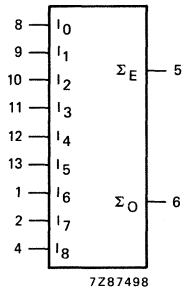


Fig. 2 Logic symbol.

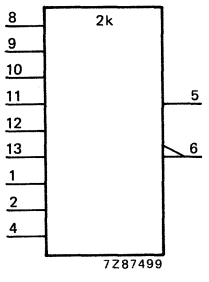


Fig. 3 IEC logic symbol.

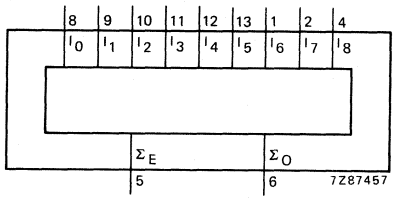


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS	OUTPUTS	
number of HIGH data inputs (I_0 to I_8)	Σ_E	Σ_O
even	H	L
odd	L	H

H = HIGH voltage level
L = LOW voltage level

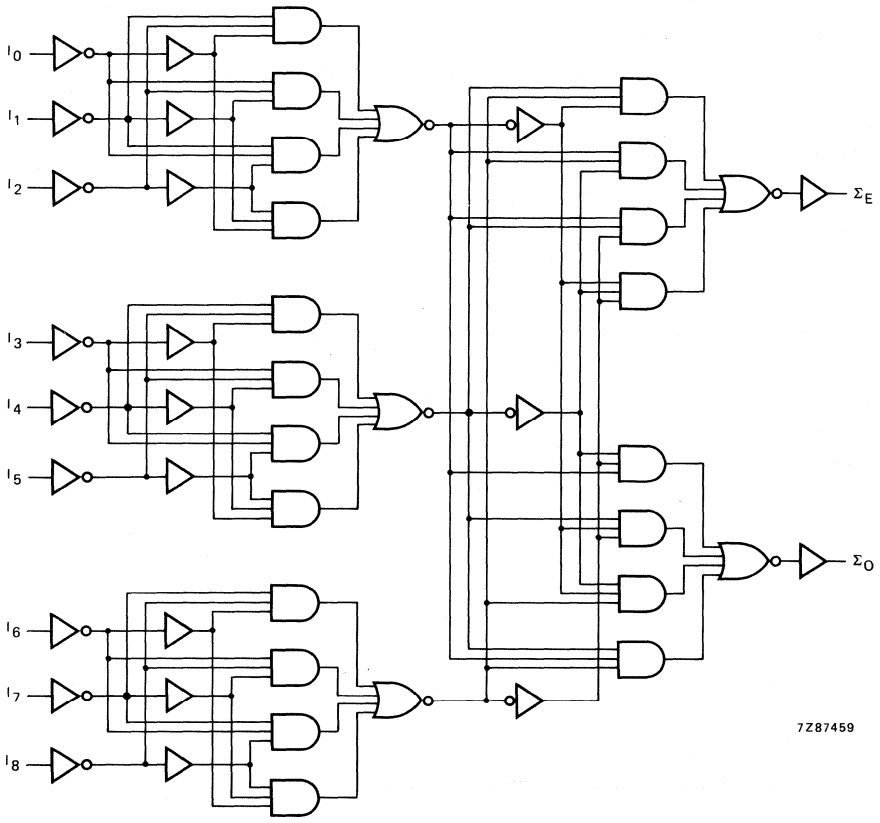


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
I_n	1.0

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Σ_E			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to Σ_O			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Σ_E			42		53		63	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to Σ_O			45		56		68	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

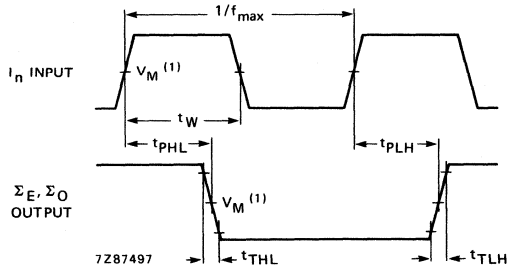


Fig. 6 Waveforms showing the data input (I_n) to parity outputs (Σ_E, Σ_O) propagation delays and the output transition time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

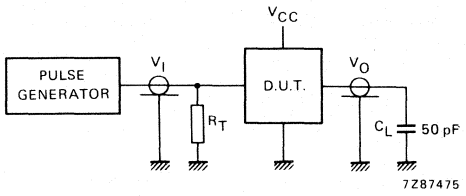


Fig. 7 Test circuit.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

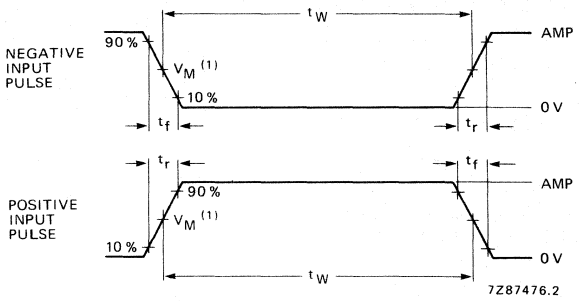


Fig. 8 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

4-BIT FULL ADDER WITH FAST CARRY

FEATURES

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal carry look-ahead
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT283 add two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 to Σ_4) and the out-going carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + + 4(A_3 + B_3) + 8(A_4 + B_4) = = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the "283" can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results Σ_1 to Σ_4 and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1 can arbitrary be assigned to pins 5, 6, 7, etc.

See the "583" for the BCD version.

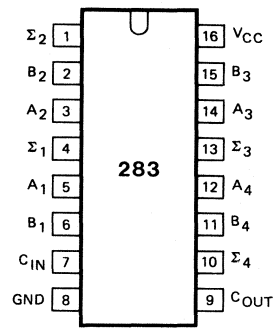


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n, B_n, C_n to any output	C_L = 15 pF; V_{CC} = 5 V	12	14	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT283P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT283D; PC74HC/HCT283D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT283T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	Σ_1 to Σ_4	sum outputs
5, 3, 14, 12	A_1 to A_4	A operand inputs
6, 2, 15, 11	B_1 to B_4	B operand inputs
7	C_{IN}	carry input
8	GND	ground (0 V)
9	C_{OUT}	carry output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

H = HIGH voltage level
L = LOW voltage level

Examples

1001
1010 (10 + 9 = 19) (carry + 5 + 6 = 12)
for active LOW

10011
for active HIGH

DIGITAL PHASE-LOCKED-LOOP FILTER

FEATURES

- Digital design avoids analog compensation errors
- Easily cascadable for higher order loops
- Useful frequency from DC to:
  50 MHz typical (K-clock)
  35 MHz typical (I/D-clock)
- Power-on reset
- Output capability:
  bus driver/standard

GENERAL DESCRIPTION

The 54/74HC/HCT297 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT297 are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-n counter, to build first order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and ege-controlled (ECPD) phase detectors are provided for maximum flexibility.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation or to cascade to higher order phase-locked-loops.

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With, A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwith by manipulating the A through D inputs can maximize the overall performance of the digital phase-locked loop.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\phi A_2, \phi B$ to $ECPD_{OUT}$	C_L = 15 pF; V_{CC} = 5 V	15	17	ns
f_{max}	maximum K_{CP} frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT297P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT297D; PC74HC/HCT297D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT297T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1, 15, 14	A, B, C, D	modulo control inputs
3	EN_{CTR}	K-counter enable input
4	K_{CP}	K-counter clock input
5	I/D_{CP}	increment/decrement clock input
6	$D/\overline{U}$	down/up control input
7	I/D_{OUT}	increment/decrement bus output
8	GND	ground (0 V)
9, 10, 13	$\phi A_1, \phi B, \phi A_2$	phase inputs
11	$XORPD_{OUT}$	EXCLUSIVE-OR phase detector output
12	$ECPD_{OUT}$	edge-controlled phase detector output
16	V_{CC}	positive supply voltage

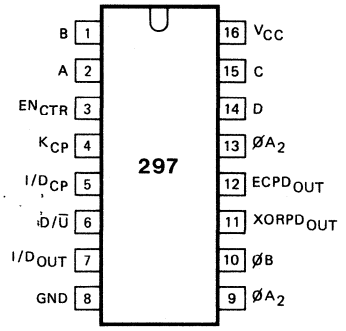


Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

The "297" can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by V_{CC} and temperature variations, but depends solely on accuracies of the K-clock, I/D-clock and loop propagation delays.

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time, depending on the direction of the phase error ($\phi_{IN} - \phi_{OUT}$). Within these limits, the phase detector output varies linearly with the input phase error according to the gain k_d, which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{phase detector output} = \frac{\%\,\text{HIGH} - \%\,\text{LOW}}{100}$$

The output of the phase detector will be $k_d\phi_e$, where the phase error $\phi_e = \phi_{IN} - \phi_{OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function, but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (k_d) for an XORPD is 4, because its output remains HIGH ($XORPD_{OUT}$ = 1) for a phase error of 1/4 cycle.
Similarly, k_d for the ECPD is 2, since its output remains HIGH for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕ_e defined to be zero. For the basic DPLL system ϕ_e = 0, when the phase detector output is a square wave.

The XORPD inputs are 1/4 cycle out-of-phase for zero phase error. For the ECPD, ϕ_e = 0 when the inputs are 1/2 cycle out-of-phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mf_c, which is a multiple M of the loop centre frequency f_c. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(k_d\phi_e Mf_c)/K$. The carry and borrow pulses go to the increment/decrement (I/D) circuit, which, in the absence of any carry or borrow pulse, has an output that is 1/2 of the input clock (I/D_{CP}). The input clock is just a multiple, 2N, of the loop centre frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT}. Thus the output of the I/D circuit will be $Nf_c + (k_d\phi_e Mf_c)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus: $f_o = f_c + (k_d\phi_e Mf_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M = 2N.

Thus the simple first-order phase-locked-loop with a adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

K-COUNTER (DIGITAL CONTROL) FUNCTION TABLE

D	C	B	A	MODULO (K)
L	L	L	L	inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

EXCLUSIVE-OR PHASE DETECTOR FUNCTION TABLE

ϕA_1	ϕB	$XORPD_{OUT}$
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR TABLE

ϕA_2	ϕB	$ECPD_{OUT}$
H or L	↓	H
↓	H or L	L
H or L	↑	no change
↑	H or L	no change

H = HIGH voltage level
L = LOW voltage level
↓ = HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

8-BIT UNIVERSAL SHIFT REGISTER; 3-STATE

FEATURES

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes: shift left
  shift right
  hold (store)
  load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability:
  bus driver (parallel I/Os)
  standard (serial outputs)

GENERAL DESCRIPTION

The 54/74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (S_0 and S_1), as shown in the mode select table.

All flip-flop outputs have 3-state buffers to separate these outputs (I/O_0 to I/O_7) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q_0 and Q_7) are used for expansion in serial shifting of longer words.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay CP to Q_0, Q_7 CP to I/O_n	C_L = 15 pF V_{CC} = 5 V	17 17	17 18	ns ns
t_{PLH}	CP to Q_0, Q_7 CP to I/O_n		17 17	14 17	ns ns
t_{PHL}	$\overline{MR}$ to Q_0, Q_7 or I/O_n		18	19	ns
f_{max}	maximum clock frequency		41	41	MHz
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	170	170	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT299P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT299T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION **See next page**

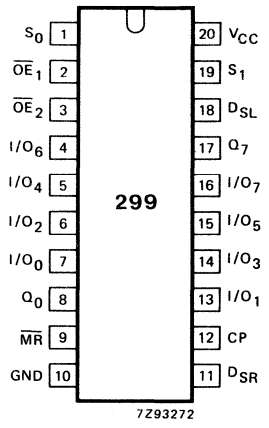


Fig. 1 Pin configuration.

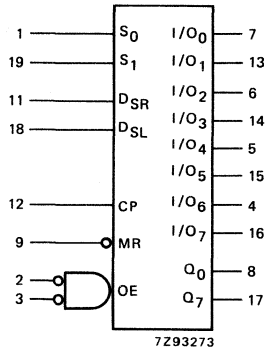


Fig. 2 Logic symbol.

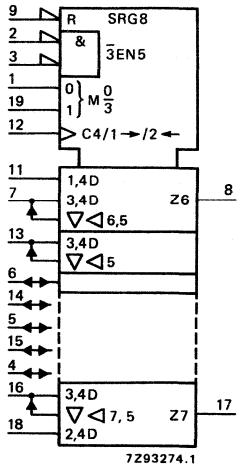


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	S_0, S_1	mode select inputs
2, 3	$\overline{OE}_1$, $\overline{OE}_2$	3-state output enable inputs (active LOW)
7, 13, 6, 14, 5, 15, 4, 16	I/O_0 to I/O_7	parallel data inputs or 3-state parallel outputs (bus driver)
8, 17	Q_0, Q_7	serial outputs (standard output)
9	$\overline{MR}$	asynchronous master reset input (active LOW)
10	GND	ground (0 V)
11	D_{SR}	serial data shift-right input
12	CP	clock input (LOW-to-HIGH, edge-triggered)
18	D_{SL}	serial data shift-left input
20	V_{CC}	positive supply voltage

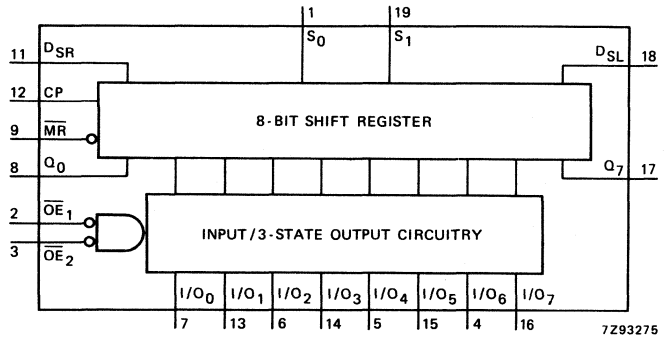


Fig. 4 Functional diagram.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	asynchronous reset; Q_0-Q_7 = LOW
H	H	H	↑	parallel load; $I/O_n \rightarrow Q_n$
H	L	H	↑	shift right; $D_{SR} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$ etc.
H	H	L	↑	shift left; $D_{SL} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$ etc.
H	L	L	X	hold

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION (Cont'd.)

A LOW signal on the asynchronous master reset input ($\overline{MR}$) overrides the S_n and clock (CP) inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on the 3-state output enable inputs ($\overline{OE}_1$ or $\overline{OE}_2$) disables the 3-state buffers and the I/O_n outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1, when in preparation for a parallel load operation.

DEVELOPMENT DATA

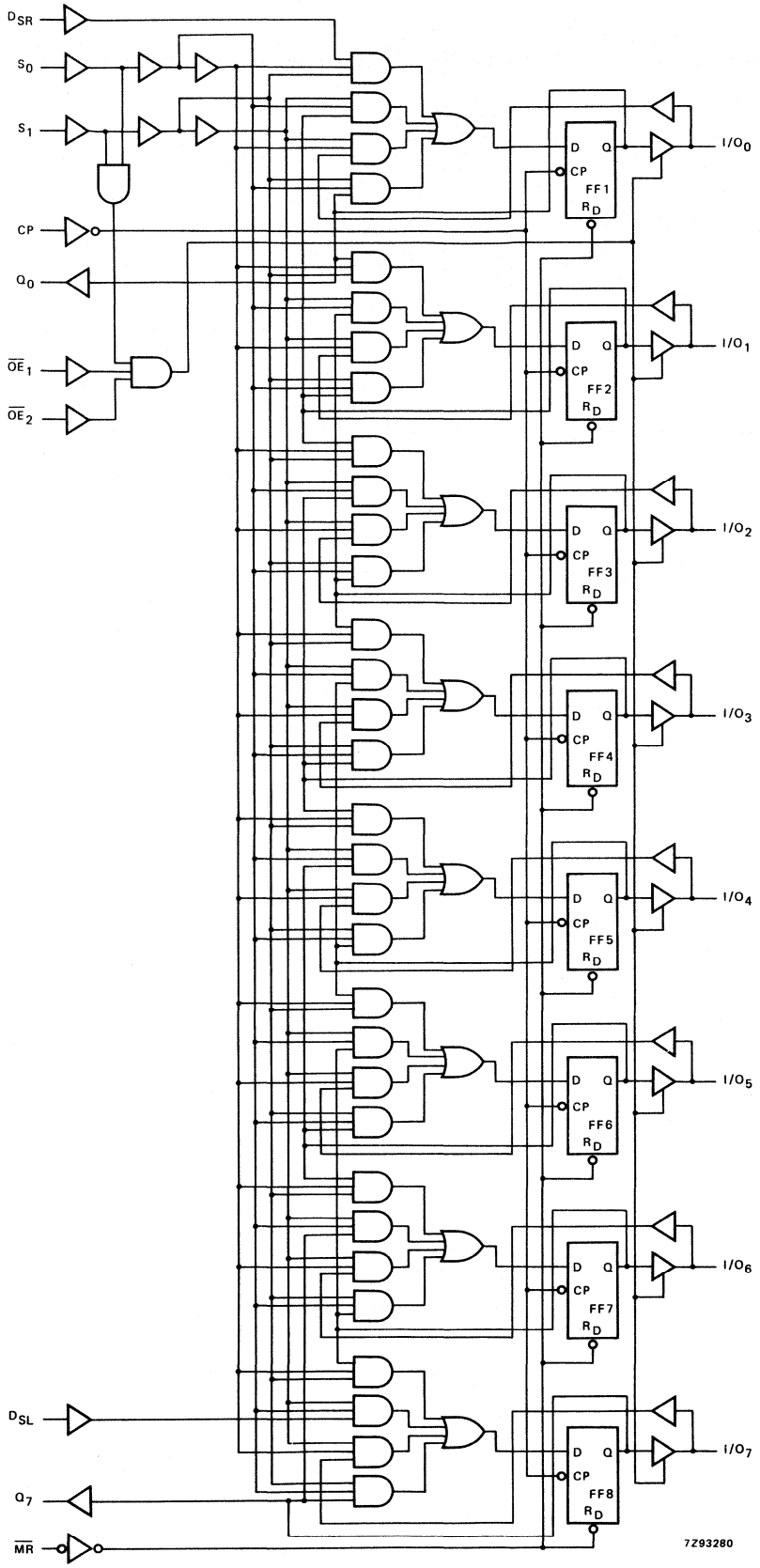


Fig. 5 Logic diagram.

RATINGS (STANDARD OUTPUTS)

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RATINGS (BUS DRIVER OUTPUTS)

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC (STANDARD OUTPUTS)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current (note 1)			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

Note

1. When testing I_{CC}, I/O_n outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND. This is because an input stage is connected to the terminal permanently.

DC CHARACTERISTICS FOR 54/74HCT (STANDARD OUTPUTS)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current (note 2)			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.
2. When testing I_{CC}, I/O_n outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND.
   This is because an input stage is connected to the terminal permanently.

input	unit load coefficient
I/O_n	0.20
D_{SR}, D_{SL}	0.20
$\overline{CP}$, S_0	0.60
$\overline{MR}$, S_1	0.20
$\overline{OE}_n$	0.30

DC CHARACTERISTICS FOR 54/74HC (BUS DRIVER OUTPUTS)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current (note 1)			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

Note

1. When testing I_{CC}, I/O_n outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND. This is because an input stage is connected to the terminal permanently.

DC CHARACTERISTICS FOR 54/74HCT (BUS DRIVER OUTPUTS)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current (note 2)			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.
2. When testing I_{CC}, I/O_n outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND.
   This is because an input stage is connected to the terminal permanently.

input	unit load coefficient
I/O_n	0.20
D_{SR}, D_{SL}	0.20
CP, S_0	0.60
$\overline{MR}$, S_1	0.20
$\overline{OE}_n$	0.30

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_0, Q_7			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay CP to I/O_n			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_0, Q_7 or I/O_n			220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_0, Q_7 or I/O_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}	3-state output disable time $\overline{OE}_n$ to Q_0, Q_7 or I/O_n			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 9
t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_0, Q_7 or I/O_n			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/ t_{TLH}	output transition time bus driver (I/O_n)			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time standard (Q_0, Q_7)			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	125 25 21			155 31 26		190 28 32		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time I/O_n, D_{SR}, D_{SL} to CP	150 30 26			190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time S_0, S_1 to CP	180 36 31			225 45 38		270 54 46		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time I/O_n, D_{SR}, D_{SL} to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time S_0, S_1 to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	4 22 26			4 18 21		3 15 18		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay CP to Q_0, Q_7			41		51		62	ns	4.5	Fig. 6
t_{PLH}	propagation delay CP to Q_0, Q_7			35		44		53	ns	4.5	Fig. 6
t_{PHL}	propagation delay CP to I/O_n			44		55		66	ns	4.5	Fig. 6
t_{PLH}	propagation delay CP to I/O_n			40		50		60	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_0, Q_7 or I/O_n			46		58		69	ns	4.5	Fig. 7
t_{PZH}	3-state output enable time $\overline{OE}_n$ to Q_0, Q_7 or I/O_n			40		50		60	ns	4.5	Fig. 9
t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_0, Q_7 or I/O_n			35		44		53	ns	4.5	Fig. 9
t_{PHZ}	3-state output disable time $\overline{OE}_n$ to Q_0, Q_7 or I/O_n			40		50		60	ns	4.5	Fig. 9
t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_0, Q_7 or I/O_n			35		44		53	ns	4.5	Fig. 9
t_{THL}/ t_{TLH}	output transition time bus driver (I/O_n)			12		15		18	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time standard (Q_0, Q_7)			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	25			33		39		ns	4.5	Fig. 6
t_W	master reset pulse width LOW	20			25		30		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	10			9		11		ns	4.5	Fig. 7
t_{su}	set-up time I/O_n, D_{SR}, D_{SL} to CP	30			38		45		ns	4.5	Fig. 6
t_{su}	set-up time S_0, S_1 to CP	32			40		48		ns	4.5	Fig. 8
t_h	hold time I/O_n, D_{SR}, D_{SL} to CP	0			0		0		ns	4.5	Fig. 6
t_h	hold time S_0, S_1 to CP	0			0		0		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	22			18		15		MHz	4.5	Fig. 6

AC WAVEFORMS

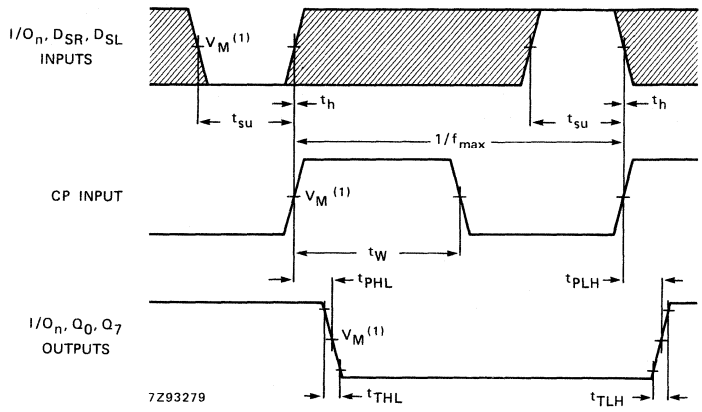


Fig. 6 Waveforms showing the clock (CP) to output (I/O_n, Q_0, Q_7) propagation delays, the clock pulse width, the I/O_n, D_{SR} and D_{SL} to CP set-up and hold times, the output transition times and the maximum clock frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

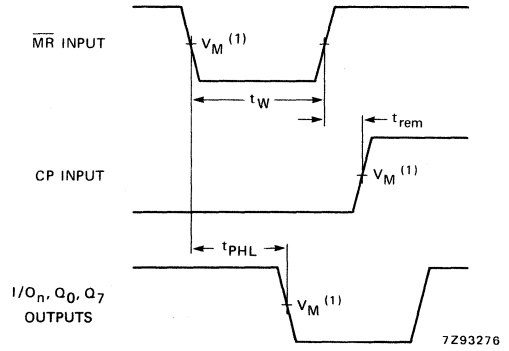


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width (LOW), the master reset to output (I/O_n, Q_0, Q_7) propagation delays and the master reset to clock (CP) removal time.

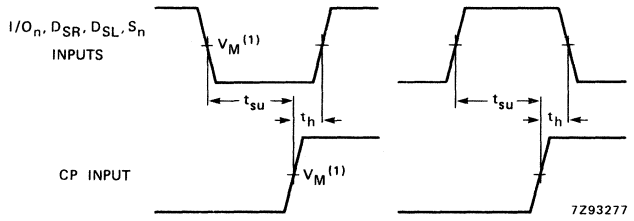


Fig. 8 Waveforms showing the set-up and hold times from the mode control inputs (S_0, S_1) to the clock (CP).

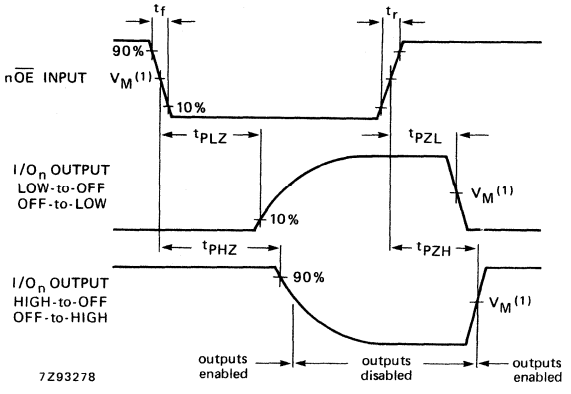
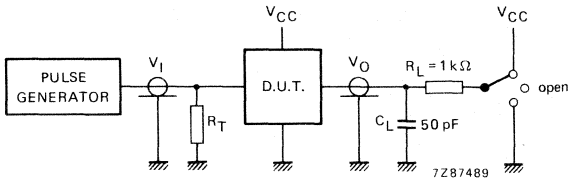


Fig. 9 Waveforms showing the 3-state enable and disable times for $\overline{OE}_n$ inputs.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 10 Test circuit

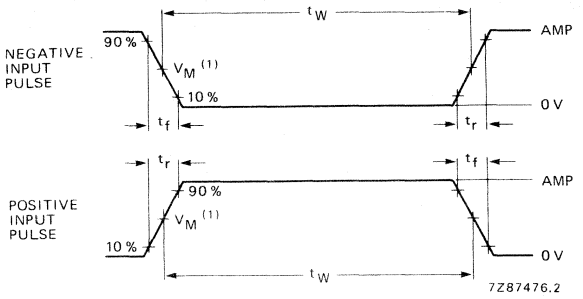


Fig. 11 Input pulse definitions

Definitions for Figs. 10 and 11:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

8-INPUT MULTIPLEXER/REGISTER WITH TRANSPARENT LATCHES; 3-STATE

FEATURES

- **Transparent data latch**
- **Transparent address latch**
- **Easily expanding**
- **Complementary outputs**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT354 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT354 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input ($\overline{LE}$).

The transparent 8-bit data latches are enabled when the active LOW data enable input ($\overline{E}$) is LOW.
When the output enable input $\overline{OE}_1$ = HIGH, $\overline{OE}_2$ = HIGH or OE_3 = LOW, the outputs go to the high impedance OFF-state.
Operation of these output enable inputs does not affect the state of the latches.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay S_n, D_n to Y, $\overline{Y}$	C_L = 15 pF; V_{CC} = 5 V	23	25	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT354P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT354T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D_0 to D_7	data inputs
9	$\overline{E}$	data enable input (active LOW)
10	GND	ground (0 V)
11	$\overline{LE}$	latch enable input (active LOW)
14, 13, 12	S_0, S_1, S_2	select inputs
15, 16	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
17	OE_3	output enable input (active HIGH)
18	$\overline{Y}$	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V_{CC}	positive supply voltage

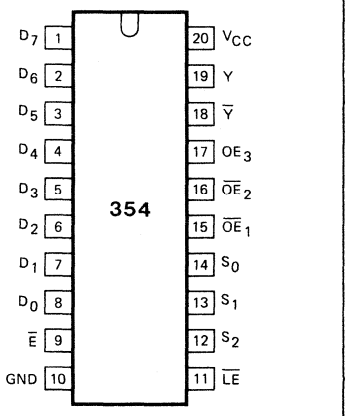


Fig. 1 Pin configuration.

FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION
ADDRESS *				OUTPUT ENABLE					
S_2	S_1	S_0	$\overline{E}$	$\overline{OE}_1$	$\overline{OE}_2$	OE_3	Y	$\overline{Y}$	
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	L	L	L	H	D_0	$\overline{D}_0$	data latch is transparent
L	L	H	L	L	L	H	D_1	$\overline{D}_1$	
L	H	L	L	L	L	H	D_2	$\overline{D}_2$	
L	H	H	L	L	L	H	D_3	$\overline{D}_3$	
H	L	L	L	L	L	H	D_4	$\overline{D}_4$	
H	L	H	L	L	L	H	D_5	$\overline{D}_5$	
H	H	L	L	L	L	H	D_6	$\overline{D}_6$	
H	H	H	L	L	L	H	D_7	$\overline{D}_7$	
L	L	L	H	L	L	H	D_{0n}	$\overline{D}_{0n}$	data is latched
L	L	H	H	L	L	H	D_{1n}	$\overline{D}_{1n}$	
L	H	L	H	L	L	H	D_{2n}	$\overline{D}_{2n}$	
L	H	H	H	L	L	H	D_{3n}	$\overline{D}_{3n}$	
H	L	L	H	L	L	H	D_{4n}	$\overline{D}_{4n}$	
H	L	H	H	L	L	H	D_{5n}	$\overline{D}_{5n}$	
H	H	L	H	L	L	H	D_{6n}	$\overline{D}_{6n}$	
H	H	H	H	L	L	H	D_{7n}	$\overline{D}_{7n}$	

D_0 to D_7 = data at inputs D_0 to D_7
D_{0n} to D_{7n} = data at inputs D_0 to D_7 before the most recent LOW-to-HIGH transition of $\overline{E}$

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

* This column shows the input address set-up with $\overline{LE}$ = LOW

8-INPUT MULTIPLEXER/REGISTER; 3-STATE

FEATURES

- Non-transparent data latch
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT356 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT356 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input $\overline{LE}$.

Data on the 8 input lines (D_0 to D_7) is clocked into a edge-triggered data register by a LOW-to-HIGH transition of the clock (CP).
When the output enable input $\overline{OE}_1$ = HIGH, $\overline{OE}_2$ = HIGH or OE_3 = LOW, the outputs go to the high impedance OFF-state.
Operation of these output enable inputs does not affect the state of the latches and register.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay S_n, CP to Y, $\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	23	25	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT356P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT356T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D_0 to D_7	data inputs
9	CP	clock input (LOW-to-HIGH, edge-triggered)
10	GND	ground (0 V)
11	$\overline{LE}$	latch enable input (active LOW)
14, 13, 12	S_0, S_1, S_2	select inputs
15, 16	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
17	OE_3	output enable input (active HIGH)
18	$\overline{Y}$	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V_{CC}	positive supply voltage

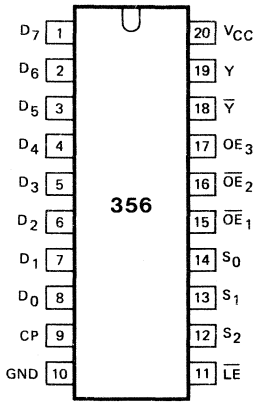


Fig. 1 Pin configuration.

FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION
ADDRESS *				OUTPUT ENABLE					
S_2	S_1	S_0	CP	$\overline{OE}_1$	$\overline{OE}_2$	OE_3	Y	$\overline{Y}$	
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	↑	L	L	H	D_{0n}	$\overline{D}_{0n}$	data is clocked into latch
L	L	H	↑	L	L	H	D_{1n}	$\overline{D}_{1n}$	
L	H	L	↑	L	L	H	D_{2n}	$\overline{D}_{2n}$	
L	H	H	↑	L	L	H	D_{3n}	$\overline{D}_{3n}$	
H	L	L	↑	L	L	H	D_{4n}	$\overline{D}_{4n}$	
H	L	H	↑	L	L	H	D_{5n}	$\overline{D}_{5n}$	
H	H	L	↑	L	L	H	D_{6n}	$\overline{D}_{6n}$	
H	H	H	↑	L	L	H	D_{7n}	$\overline{D}_{7n}$	
L	L	L	**	L	L	H	D_{0p}	$\overline{D}_{0p}$	outputs do not change states
L	L	H	**	L	L	H	D_{1p}	$\overline{D}_{1p}$	
L	H	L	**	L	L	H	D_{2p}	$\overline{D}_{2p}$	
L	H	H	**	L	L	H	D_{3p}	$\overline{D}_{3p}$	
H	L	L	**	L	L	H	D_{4p}	$\overline{D}_{4p}$	
H	L	H	**	L	L	H	D_{5p}	$\overline{D}_{5p}$	
H	H	L	**	L	L	H	D_{6p}	$\overline{D}_{6p}$	
H	H	H	**	L	L	H	D_{7p}	$\overline{D}_{7p}$	

D_{0n} to D_{7n} = data present at inputs D_0 to D_7 when the data latch clock made the transition from LOW-to-HIGH

D_{0p} to D_{7p} = data previously latched into the data latch by the LOW-to-HIGH transition of the data latch clock

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Z = high impedance OFF-state

* This column shows the input address set-up with $\overline{LE}$ = LOW.
** CP is HIGH, LOW or ↓.

HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT365 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT365 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "365" is identical to the "366" but has non-inverting outputs.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	9	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT365P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT365D; PC74HC/HCT365D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT365T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

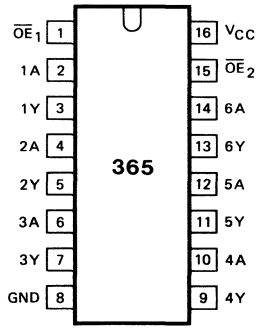


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT366 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT366 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "366" is identical to the "365" but has inverting outputs.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	n$\overline{Y}$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	9	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT366P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT366D; PC74HC/HCT366D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT366T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1$\overline{Y}$ to 6$\overline{Y}$	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

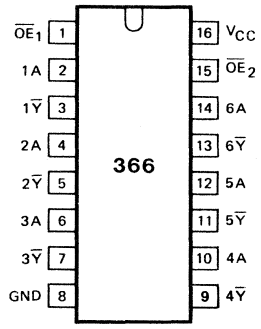


Fig. 1 Pin configuration.

HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT367 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT367 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$.

A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The "367" is identical to the "368" but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	9	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT367P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT367D; PC74HC/HCT367D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT367T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

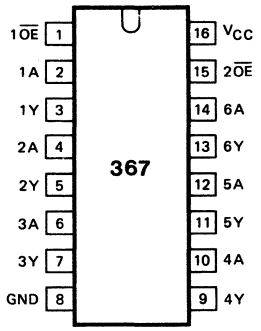


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- **Inverting outputs**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT368 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT368 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$.

A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The "368" is identical to the "367" but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nA	$n\overline{Y}$
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to $n\overline{Y}$	C_L = 15 pF; V_{CC} = 5 V	9	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT368P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT368D; PC74HC/HCT368D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT368T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	$1\overline{Y}$ to $6\overline{Y}$	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

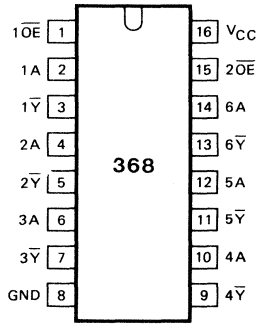


Fig. 1 Pin configuration.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE

FEATURES

- **3-state non-inverting outputs for bus oriented applications**
- **Common 3-state output enable input**
- **Functionally identical to the "563", "573" and "533"**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT373 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT373 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "373" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "373" is functionally identical to the "533", "563" and "573", but the "563" and "533" have inverted outputs and the "563" and "573" have a different pin arrangement.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n LE to Q_n	C_L = 15 pF V_{CC} = 5 V	12 14	14 14	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	45	41	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT373P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT373T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

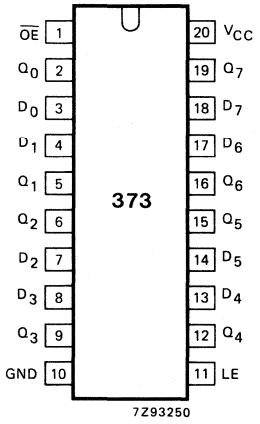


Fig. 1 Pin configuration.

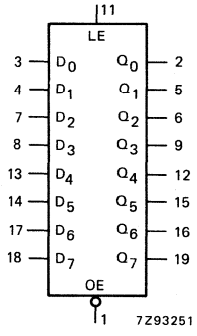


Fig. 2 Logic symbol.

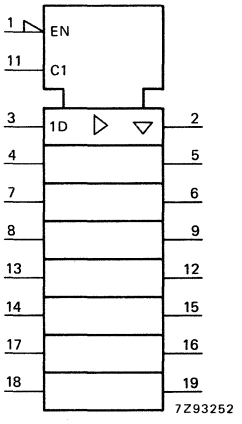


Fig. 3 IEC logic symbol.

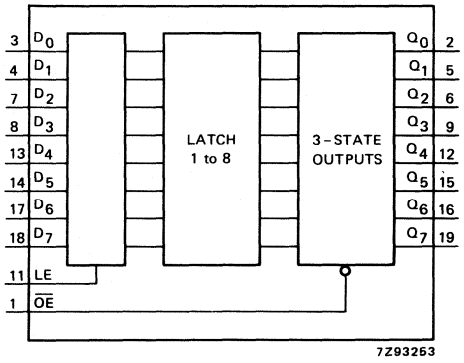


Fig. 4 Functional diagram.

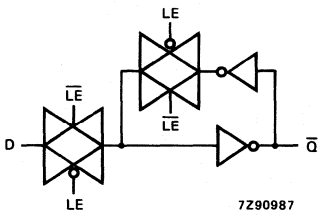


Fig. 5 Logic diagram (one latch).

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	L	l	L	L
	L	L	h	H	H
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition

L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition

Z = high impedance OFF-state

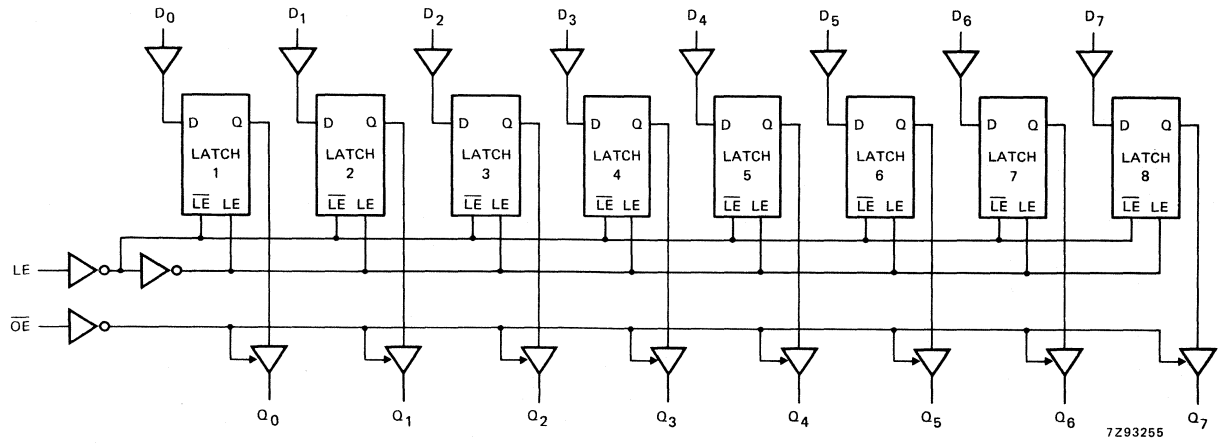


Fig. 6 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_n	0.30
LE	1.50
$\overline{OE}$	1.00

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to Q_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 7
t_W	LE pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to LE	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D_n to LE	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n			35		44		53	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to Q_n			35		44		53	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n			35		44		53	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n			35		44		53	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 7
t_W	LE pulse width HIGH	16			20		24		ns	4.5	Fig. 8
t_{su}	set-up time D_n to LE	12			15		18		ns	4.5	Fig. 10
t_h	hold time D_n to LE	8			10		12		ns	4.5	Fig. 10

DEVELOPMENT DATA

AC WAVEFORMS

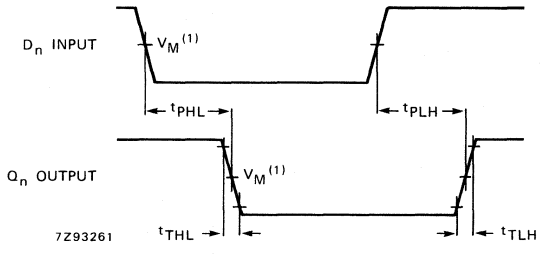


Fig. 7 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.

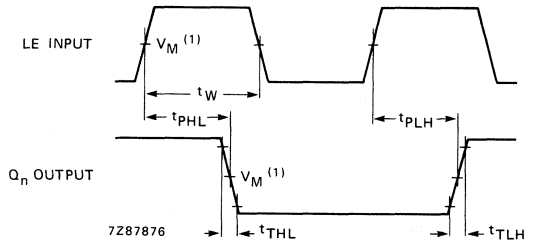


Fig. 8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

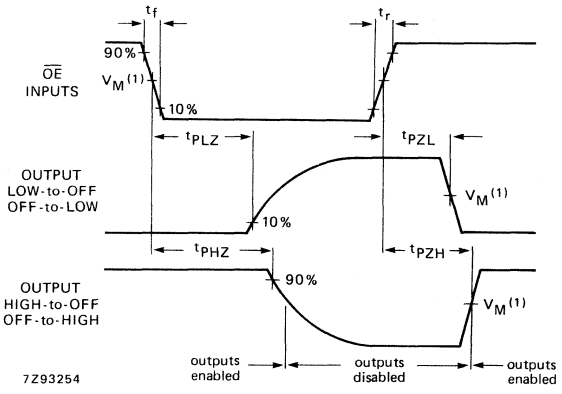


Fig. 9 Waveforms showing the 3-state enable and disable times.

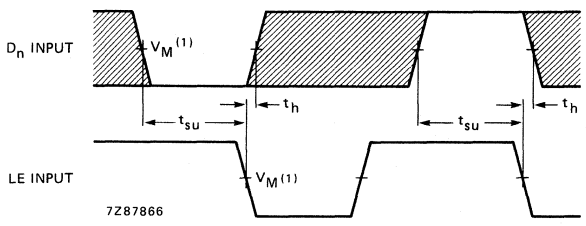


Fig. 10 Waveforms showing the data set-up and hold times for D_n input to LE input.

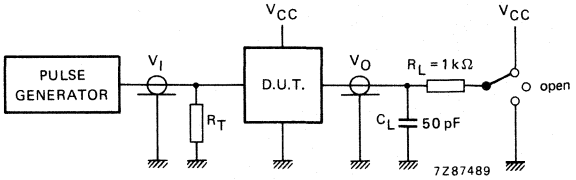
Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 11 Test circuit for 3-state outputs.

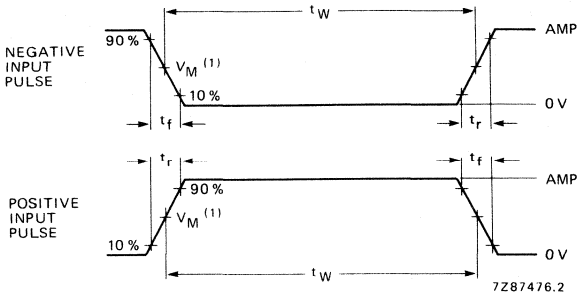


Fig. 12 Input pulse definitions.

Definitions for Figs 11 and 12:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT374 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications.
A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	15	13	ns
f_{max}	maximum clock frequency		60	48	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT374P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT374T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

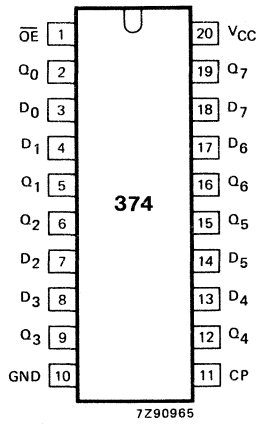


Fig. 1 Pin configuration.

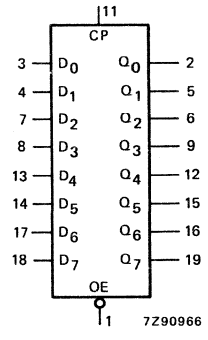


Fig. 2 Logic symbol.

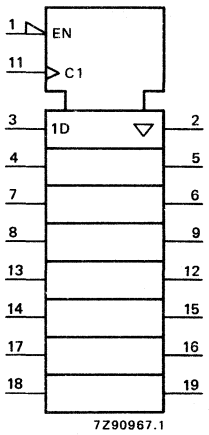


Fig. 3 IEC logic symbol.

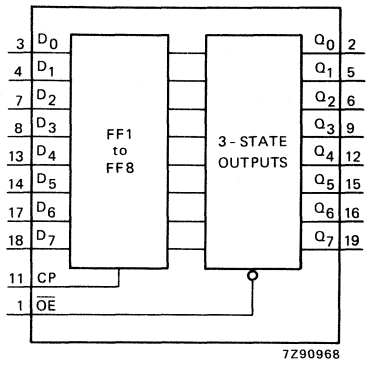


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP–FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

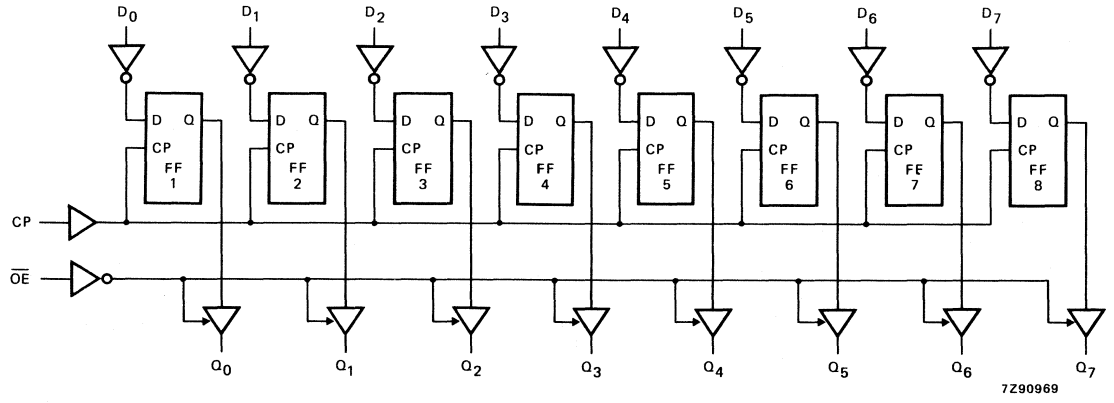


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$\overline{OE}$	1.25
CP	0.90
D_n	0.35

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to CP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			32		40		48	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n			32		40		48	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n			34		43		51	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	22			28		33		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	20			25		30		ns	4.5	Fig. 8
t_h	hold time D_n to CP	5			5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	22			18		15		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

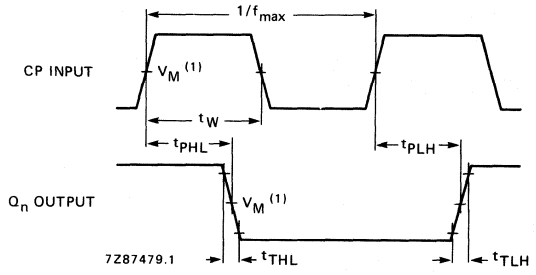


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

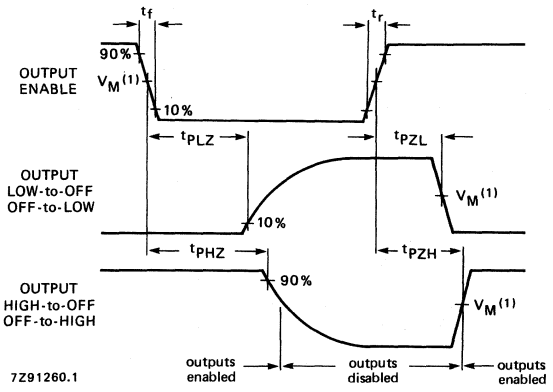


Fig. 7 Waveforms showing the 3-state enable and disable times.

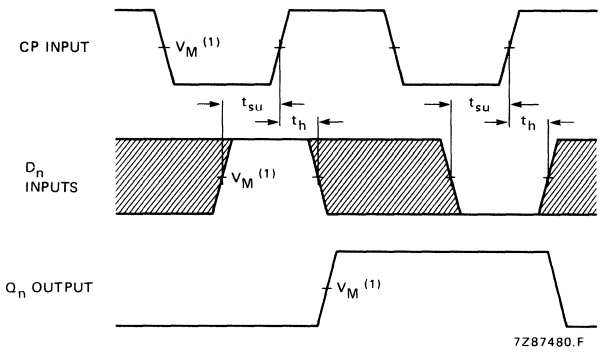


Fig. 8 Waveforms showing the data set-up and hold times for D_n input.

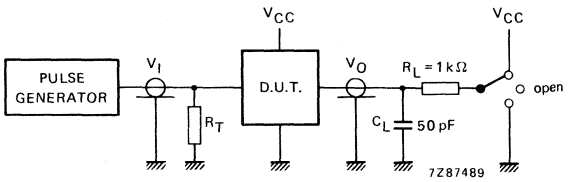
Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 9 Test circuit for 3-state outputs.

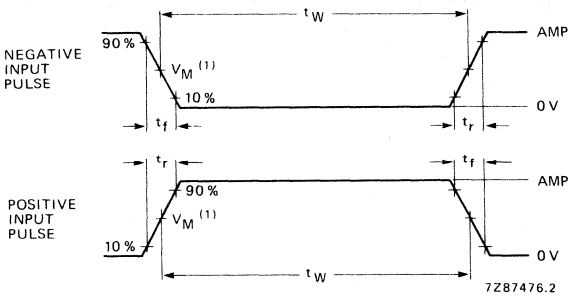


Fig. 10 Input pulse definitions.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

OCTAL D-TYPE FLIP-FLOP WITH DATA ENABLE; POSITIVE-EDGE TRIGGER

FEATURES

- Ideal for addressable register applications
- Data enable for address and data synchronization applications
- Eight positive-edge triggered D-type flip-flops
- See "273" for master reset version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT377 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT377 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs.
A common clock (CP) input loads all flip-flops simultaneously when the data enable ($\overline{E}$) is LOW.
The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

The $\overline{E}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	13	15	ns
f_{max}	maximum clock frequency		60	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT377P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT377T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{E}$	data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

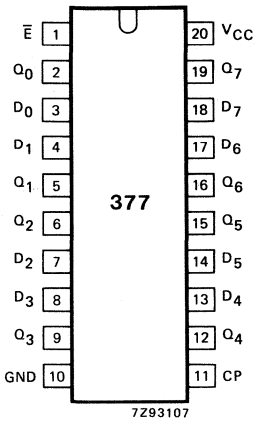


Fig. 1 Pin configuration.

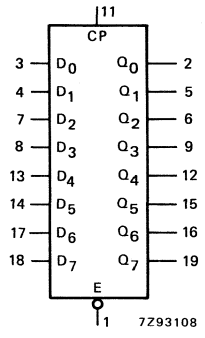


Fig. 2 Logic symbol.

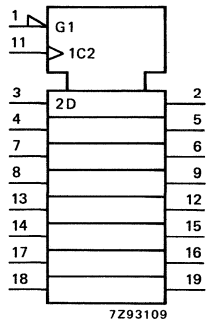


Fig. 3 IEC logic symbol.

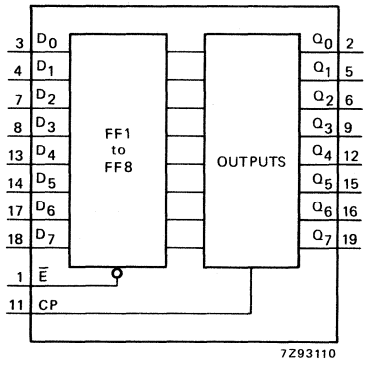


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	CP	$\overline{E}$	D_n	Q_n
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑ X	h H	X X	no change no change

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = don't care

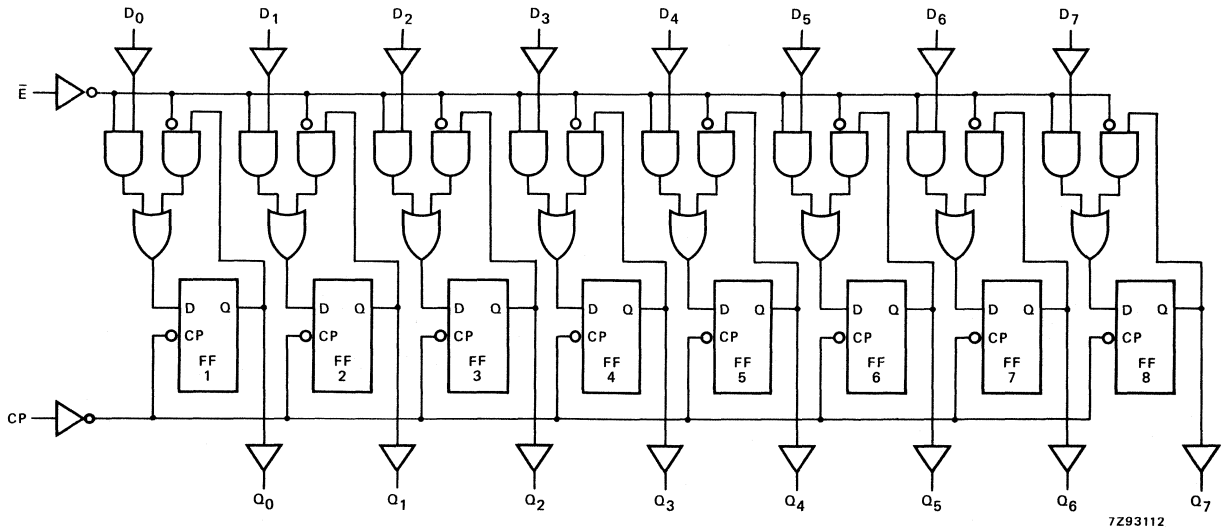


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$\overline{E}$	1.50
CP	0.50
D_n	0.20

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time $\overline{E}$ to CP	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time D_n to CP	3 3 3			3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time $\overline{E}$ to CP	4 4 4			4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			36		45		54	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	12			15		18		ns	4.5	Fig. 7
t_{su}	set-up time $\overline{E}$ to CP	22			28		33		ns	4.5	Fig. 7
t_h	hold time D_n to CP	2			2		2		ns	4.5	Fig. 7
t_h	hold time $\overline{E}$ to CP	3			3		3		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	25			19		16		MHz	4.5	Fig. 6

AC WAVEFORMS

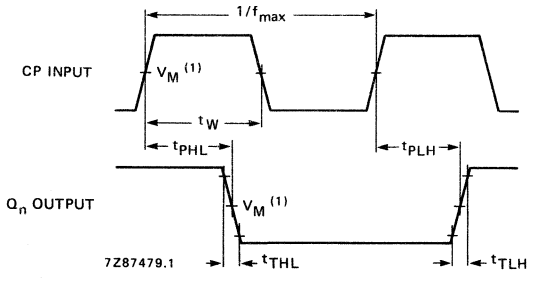


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

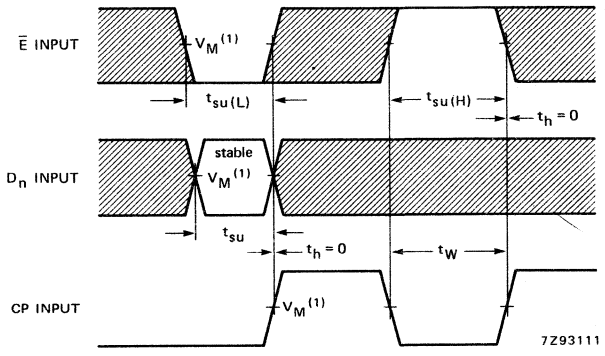


Fig. 7 Waveforms showing the data set-up and hold times from the data input (D_n) and from the data enable input ($\overline{E}$) to the clock (CP).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

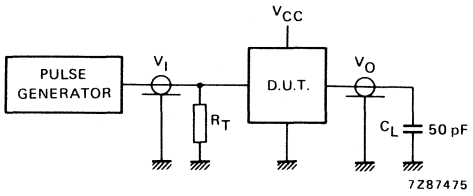


Fig. 8 Test circuit.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

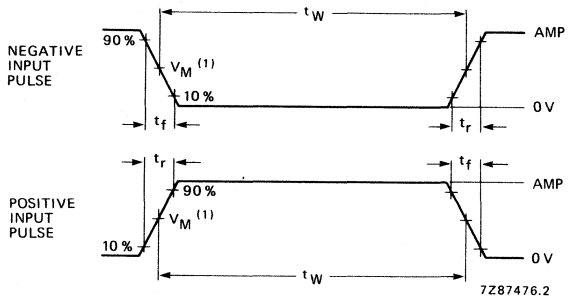


Fig. 9 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DUAL DECADE RIPPLE COUNTER

FEATURES

- Two BCD decade or bi-quinary counters
- One package can be configures to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two master reset inputs to clear each decade counter individually
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT390 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT390 are dual 4-bit decade ripple counters divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset input (nMR). If the two master reset inputs (1MR and 2MR) can be used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks ($n\overline{CP}_0$ and $n\overline{CP}_1$) of each section allow ripple counter or frequency dividion applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0 $n\overline{CP}_0$ to nQ_3	C_L = 15 pF V_{CC} = 5 V	12 24	14 26	ns ns
f_{max}	maximum clock frequency		50	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT390P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT390D; PC74HC/HCT390D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT390T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{CP}_0$, $2\overline{CP}_0$	clock input divide-by-2 section (HIGH-to-LOW, edge-triggered)
2, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 5, 6, 7	$1Q_0$ to $1Q_3$	flip-flop outputs
4, 12	$1\overline{CP}_1$, $2\overline{CP}_1$	clock input divide-by-5 section (HIGH-to-LOW, edge triggered)
8	GND	ground (0 V)
13, 11, 10, 9	$2Q_0$ to $2Q_3$	flip-flop outputs
16	V_{CC}	positive supply voltage

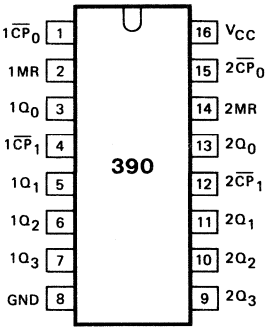


Fig. 1 Pin configuration.

Each section is triggered by the HIGH-to-LOW transition of the clock inputs ($n\overline{CP}_0$ and $n\overline{CP}_1$).
For BCD decade operation, the nQ_0 output is connected to the $n\overline{CP}_1$ input of the divide-by-5 section. For bi-quinary decade operation, the nQ_3 output is connected to the nCP_0 input and nQ_0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A HIGH level on the nMR input overrides the clocks and sets the four outputs LOW.

BCD COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note

Output Q_0 connected to $n\overline{CP}_1$ with counter input on $n\overline{CP}_0$.

H = HIGH voltage level
L = LOW voltage level

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Note

Output Q_3 connected to $n\overline{CP}_0$ with counter input on $n\overline{CP}_1$.

DUAL 4-BIT BINARY RIPPLE COUNTER

FEATURES

- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT393 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT393 are 4-bit binary ripple counters with separate clocks (1$\overline{CP}$ and 2 $\overline{CP}$) and master reset (1MR and 2MR) inputs to each counter.
The operation of each half of the "393" is the same as the "93" except no external clock connections are required.
The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.
A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0 nQ to nQ_{n+1} nMR to nQ_n	C_L = 15 pF V_{CC} = 5 V	 11 4 11	 13 4 13	 ns ns ns
f_{max}	maximum clock frequency		60	58	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	23	25	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT393D; PC74HC/HCT393P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT393D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT393T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1$\overline{CP}$, 2$\overline{CP}$	clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 4, 5, 6, 11, 10, 9, 8	$1Q_0$ to $1Q_3$, $2Q_0$ to $2Q_3$	flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

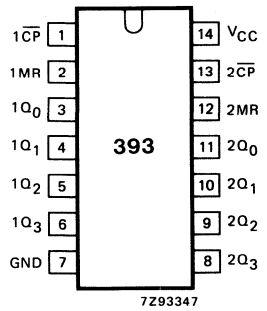


Fig. 1 Pin configuration.

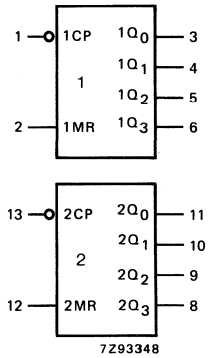


Fig. 2 Logic symbol.

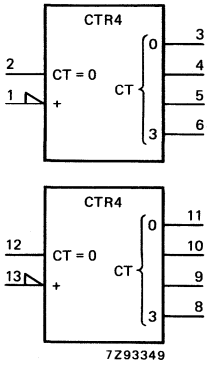


Fig. 3 IEC logic symbol.

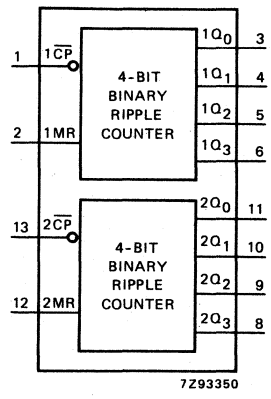


Fig. 4 Functional diagram.

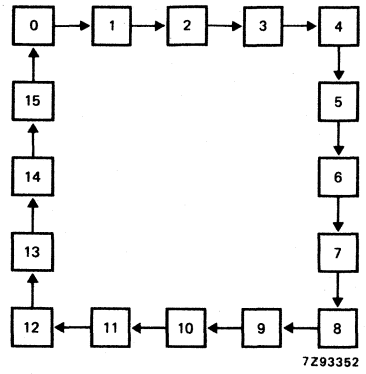


Fig. 5 State diagram.

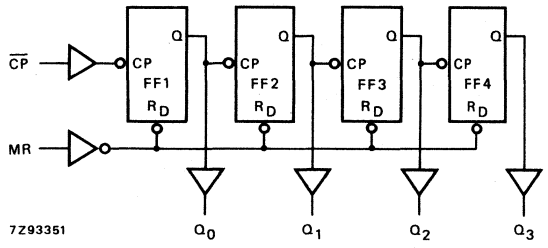


Fig. 6 Logic diagram (one counter).

COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$1\overline{CP}$	0.4
$2\overline{CP}$	0.4
1MR	1.0
2MR	1.0

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay nQ_n to nQ_{n+1}			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay nMR to nQ_n			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width; HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time nMR to $n\overline{CP}$	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0			32		40		48	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay nQ_n to nQ_{n+1}			12		15		18	ns	4.5	Fig. 7
t_{PHL}	propagation delay nMR to nQ_n			32		40		48	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	19			24		29		ns	4.5	Fig. 7
t_W	master reset pulse width; HIGH	16			20		24		ns	4.5	Fig. 8
t_{rem}	removal time nMR to $n\overline{CP}$	5			5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	27			22		18		MHz	4.5	Fig. 7

AC WAVEFORMS

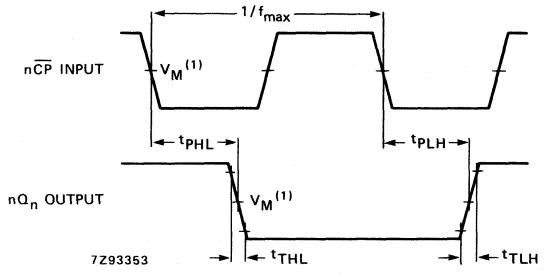


Fig. 7 Waveforms showing the clock ($n\overline{CP}$) to output ($1Q_n$, $2Q_n$) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

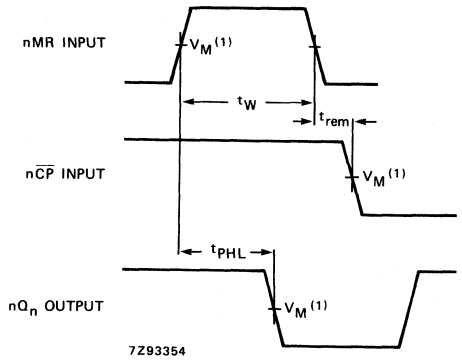


Fig. 8 Waveforms showing the master reset (nMR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($n\overline{CP}$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

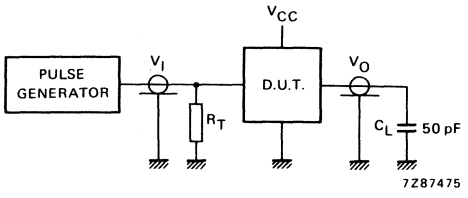


Fig. 9 Test circuit.

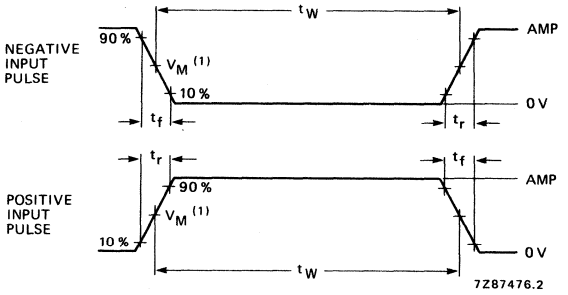


Fig. 10 Input pulse definitions.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})

GENERAL DESCRIPTION

The 54/74HC/HCT423 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT423 are dual retriggerable monostable multivibrators with output pulse width control by two methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown in Fig. 6.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. When $n\overline{R}_D$ is LOW, it forces the nQ output LOW, the $n\overline{Q}$ output HIGH and also inhibits the triggering.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$ $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 5 V R_{EXT} = 5 kΩ C_{EXT} = 0 pF	26 19	26 19	ns ns
C_I	input capacitance		3.5	3.5	pF
t_W	minimum output pulse width nQ, $n\overline{Q}$		75	75	ns

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT423D;
PC74HC/HCT423P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT423D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT423T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset action (active LOW)
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

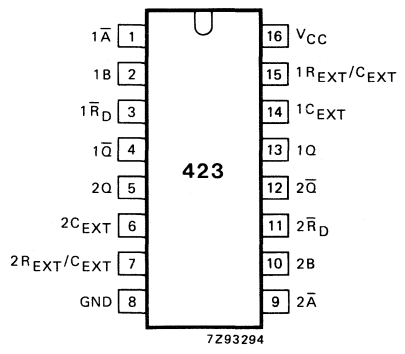


Fig. 1 Pin configuration.

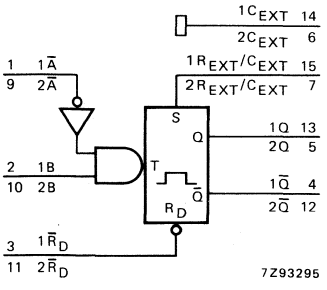


Fig. 2 Logic symbol.

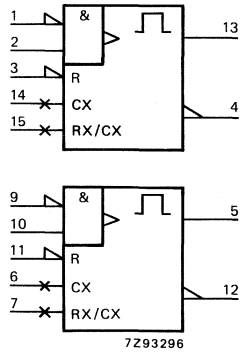


Fig. 3 IEC logic symbol.

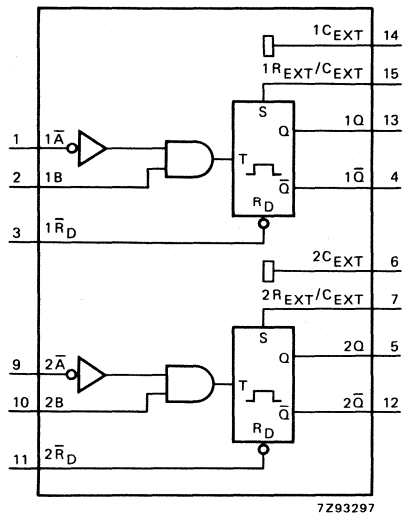


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd)

Figures 7 and 8 illustrate pulse control by reset. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.
For pulse widths, when $C_{EXT} < 10\,000$ pF, see Fig. 9.
When $C_{EXT} > 10\,000$ pF, the typical output pulse width is defined as:

$t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.),

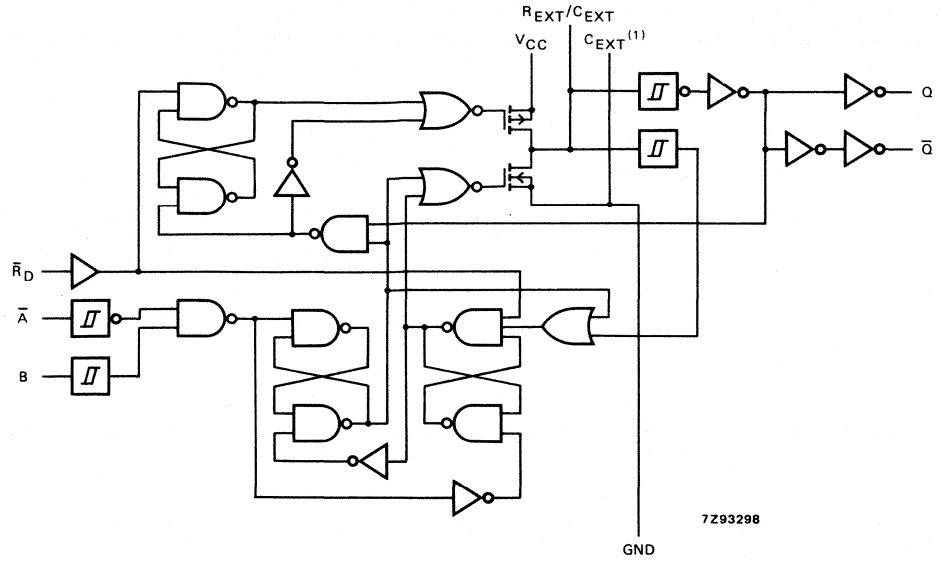
where, t_W = pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF.

Schmitt-trigger action in the nĀ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\bar{R}_D$	$n\bar{A}$	nB	nQ	$n\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎴
H	↓	H	⎍	⎴

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎴ = one LOW level output pulse



(1) It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

Fig. 5 Logic diagram.

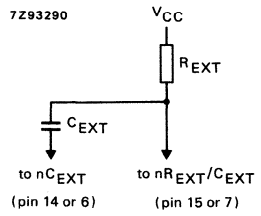


Fig. 6 Timing component connections.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		500	mW	for standard temperature range; −40 to +85 °C; 74HC/HCT above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		500	mW	for extended temperature range; −55 to +125°C; 54HC/HCT above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$n\overline{A}$, nB	0.35
$n\overline{R}_D$	0.35

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS/NOTES
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay nĀ, nB to nQ̄			350 70 60		440 88 75		525 105 89	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay nĀ, nB to nQ			330 66 56		415 83 71		495 99 84	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}	propagation delay nR̄D to nQ			230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay nR̄D to nQ̄			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	
t_W	trigger pulse width nĀ = LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width nB = HIGH	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	reset pulse width nR̄D = LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_W	output pulse width nQ, nQ̄ = HIGH		45		–		–		µs	5.0	C_{EXT} = 10 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ, nQ̄ = HIGH		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time nĀ, nB		50		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 8
R_{EXT}	external timing resistor	2		100	–		–		kΩ	5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 9

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS/NOTES
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay $n\overline{A}$, nB to $n\overline{Q}$			70		88		105	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{A}$, nB to nQ			66		83		99	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ			46		58		69	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$			50		63		75	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	
t_W	trigger pulse width $n\overline{A}$ = LOW	20			25		30		ns	4.5	Fig. 7
t_W	trigger pulse width nB = HIGH	20			25		30		ns	4.5	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	20			25		30		ns	4.5	Fig. 8
t_W	output pulse width nQ, $n\overline{Q}$ = HIGH		45		–		–		μs	5.0	C_{EXT} = 10 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ, $n\overline{Q}$ = HIGH		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		50		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 8
R_{EXT}	external timing resistor	2		100	–		–		kΩ	5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 9

Notes to AC characteristics

1. For other R_{EXT} and C_{EXT} combinations see Fig. 9.

   If $C_{EXT} > 10$ nF, the next formula is valid:

   $$t_W = K \times R_{EXT} \times C_{EXT} \text{ (typ.)}$$

   where, t_W = output pulse width in ns;
   R_{EXT} = external resistor in kΩ; C_{EXT} = external capacitor in pF;
   K = constant = 0.45 for V_{CC} = 5.0 V and 0.48 for V_{CC} = 2.0 V.

   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

2. The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}.

   The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

   If $C_{EXT} > 10$ nF, the next formula (at V_{CC} = 5.0 V) for the set-up time of a retrigger pulse is valid:

   $$t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT}) \text{ (typ.)}$$

   where, t_{rt} = retrigger time in ns;
   C_{EXT} = external capacitor in pF;
   R_{EXT} = external resistor in kΩ.

   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

DEVELOPMENT DATA

AC WAVEFORMS

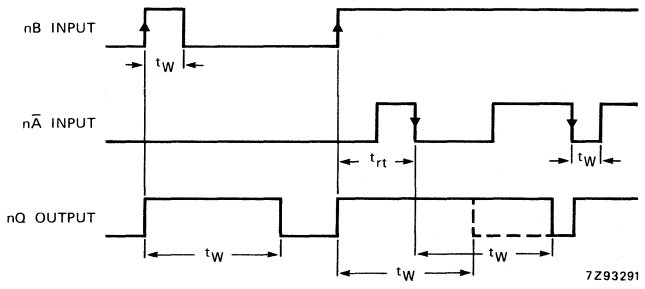


Fig. 7 Output pulse control using retrigger pulse; $n\overline{R}_D$ = HIGH.

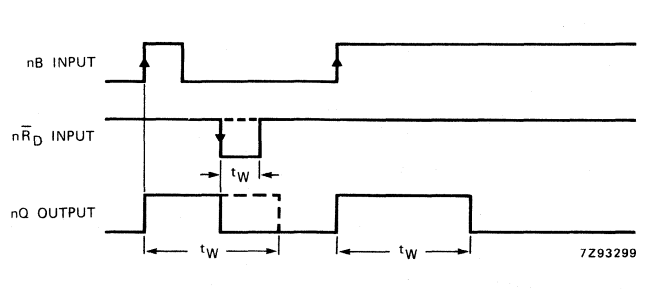


Fig. 8 Output pulse control using reset input $n\overline{R}_D$; $n\overline{A}$ = LOW.

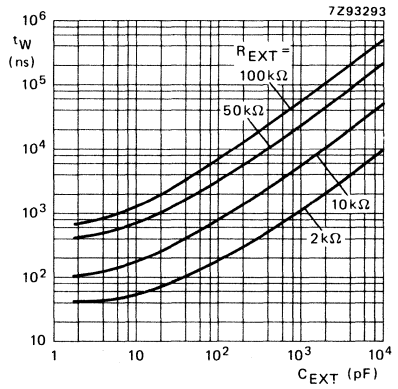


Fig. 9 Typical output pulse width as a function of the external capacitor values at V_{CC} = 5.0 V and T_{amb} = 25 °C.

TEST CIRCUIT AND WAVEFORMS

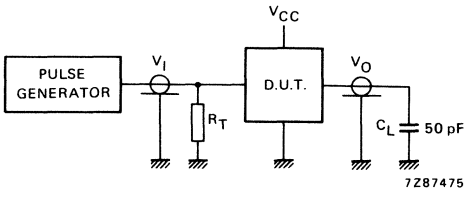


Fig. 10 Test circuit

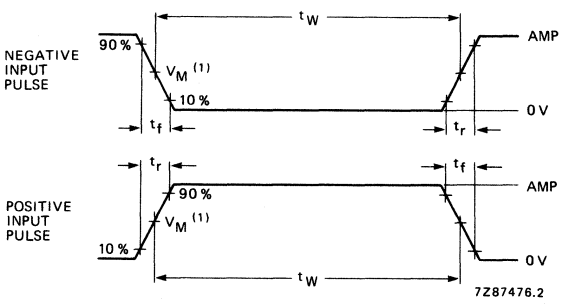


Fig. 11 Input pulse definitions

Definitions for Figs. 10 and 11:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

FEATURES

- **3-state inverting outputs for bus oriented applications**
- **Common 3-state output enable input**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT533 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT533 are octal D-type transparent latches f eaturing separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "533" consists of eight D-type transparent latches with 3-state inverting outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "533" is functionally identical to the "373", "563" and "573", but the "373" and "573" have non-inverted outputs and the "563" and "573" have a different pin arrangement.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay D_n to $\overline{Q}_n$ LE to $\overline{Q}_n$	C_L = 15 pF V_{CC} = 5 V	13 18	14 20	ns ns
t_{PLH}	propagation delay D_n to $\overline{Q}_n$ LE to $\overline{Q}_n$	C_L = 15 pF V_{CC} = 5 V	13 18	15 17	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	34	34	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT533P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT533T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}_0$ to $\overline{Q}_7$	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

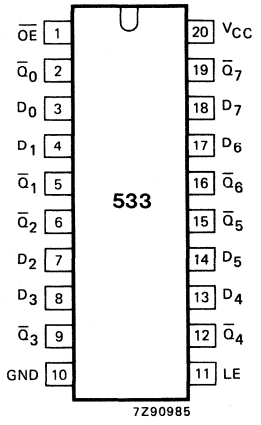


Fig. 1 Pin configuration.

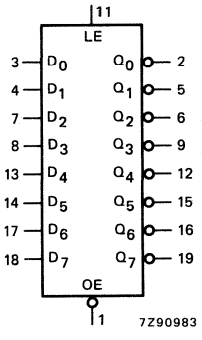


Fig. 2 Logic symbol.

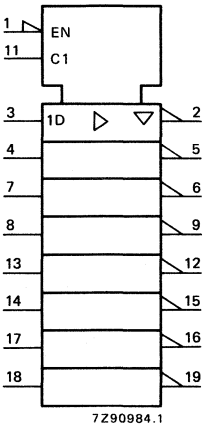


Fig. 3 IEC logic symbol.

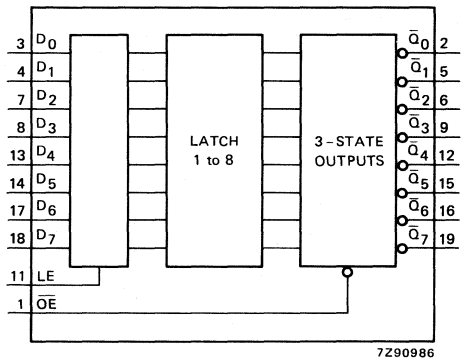


Fig. 4 Functional diagram.

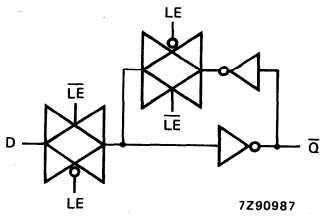


Fig. 5 Logic diagram (one latch).

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
enable and read register (transparent mode)	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	l	L	H
	L	L	h	H	L
latch register and disable outputs	H	X	X	X	Z
	H	X	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition or the HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition or the HIGH-to-LOW $\overline{OE}$ transition
X = don't care
Z = high impedance OFF-state

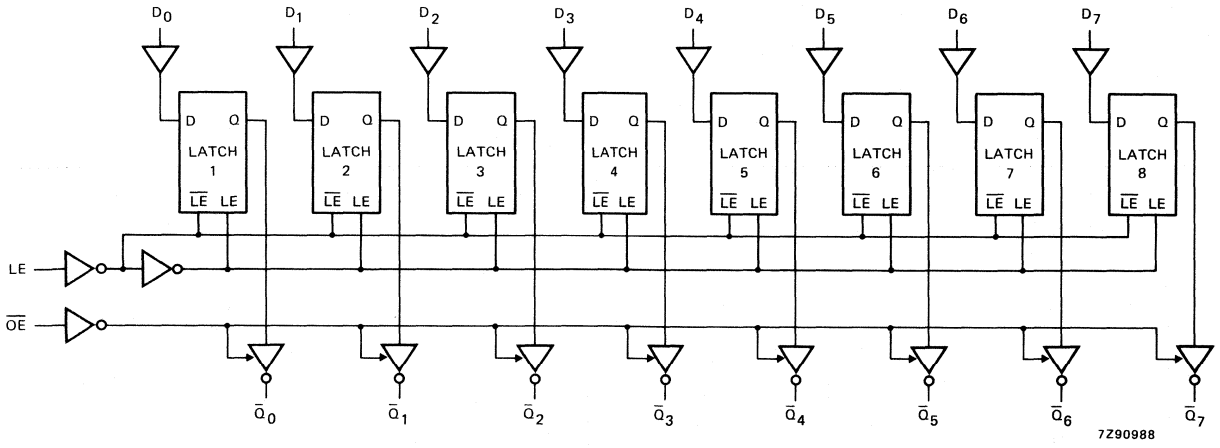


Fig. 6 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_n	0.15
$\overline{LE}$	0.30
$\overline{OE}$	0.55

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$			165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$			220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 7
t_W	LE pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to LE	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D_n to LE	35 7 6			45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 10

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay D_n to $\overline{Q}_n$			34		43		51	ns	4.5	Fig. 7
t_{PLH}	propagation delay D_n to $\overline{Q}_n$			37		46		56	ns	4.5	Fig. 7
t_{PHL}	propagation delay LE to $\overline{Q}_n$			48		60		72	ns	4.5	Fig. 8
t_{PLH}	propagation delay LE to $\overline{Q}_n$			40		50		60	ns	4.5	Fig. 8
t_{PZH}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			32		40		48	ns	4.5	Fig. 9
t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			39		49		59	ns	4.5	Fig. 9
t_{PHZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			33		41		50	ns	4.5	Fig. 9
t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			36		45		54	ns	4.5	Fig. 9
t_{THL}/ t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 7
t_W	LE pulse width HIGH	16			20		24		ns	4.5	Fig. 8
t_{su}	set-up time D_n to LE	12			15		18		ns	4.5	Fig. 10
t_h	hold time D_n to LE	8			10		12		ns	4.5	Fig. 10

AC WAVEFORMS

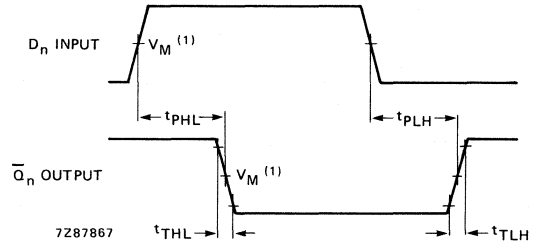


Fig. 7 Waveforms showing the data input (D_n) to output ($\overline{Q}_n$) propagation delays and the output transition times.

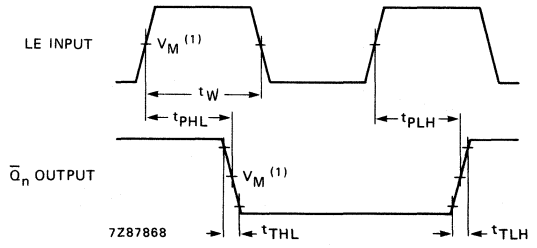


Fig. 8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ($\overline{Q}_n$) propagation delays and the output transition times.

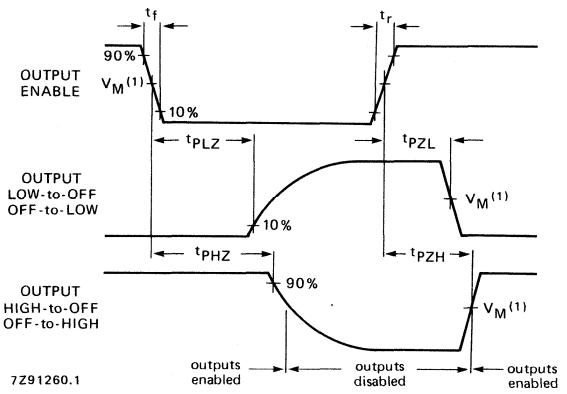


Fig. 9 Waveforms showing the 3-state enable and disable times.

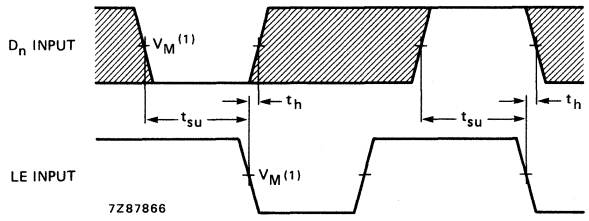


Fig. 10 Waveforms showing the data set-up and hold times for D_n input to LE input.

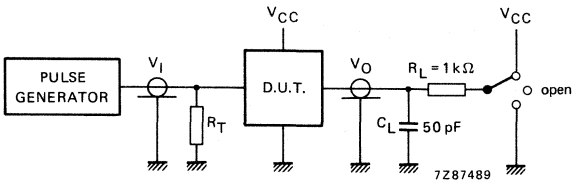
Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 11 Test circuit for 3-state outputs.

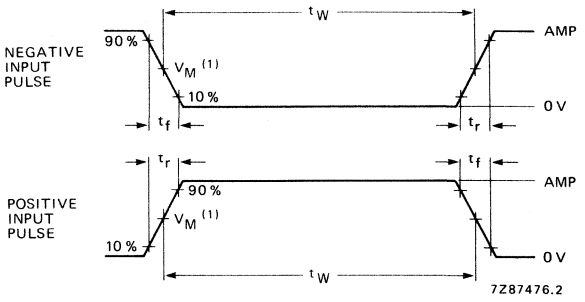


Fig. 12 Input pulse definitions.

Definitions for Figs 11 and 12:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT534 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT534 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops. The "534" is functionally identical to the "374", but has inverted outputs.

The "534" consists of eight flip-flops with individual D-type inputs and 3-state inverting outputs. The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	12	12	ns
f_{max}	maximum clock frequency		60	48	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	19	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT534P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT534T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}_0$ to $\overline{Q}_7$	3-state outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

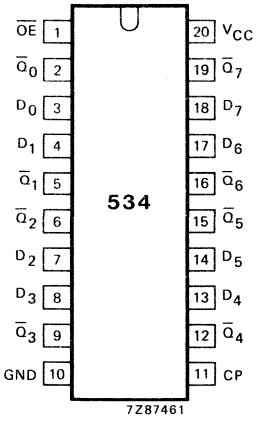


Fig. 1 Pin configuration.

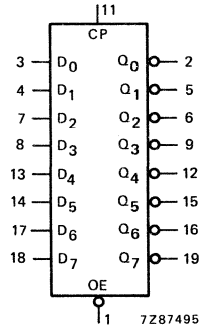


Fig. 2 Logic symbol.

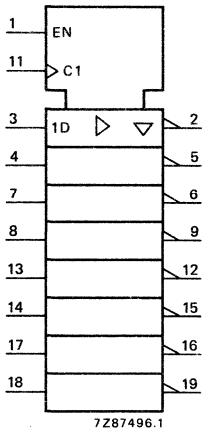


Fig. 3 IEC logic symbol.

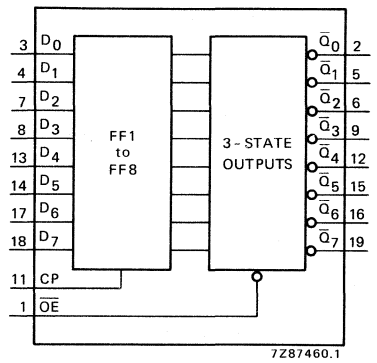


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L	↑	l	L	H
	L	↑	h	H	L
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

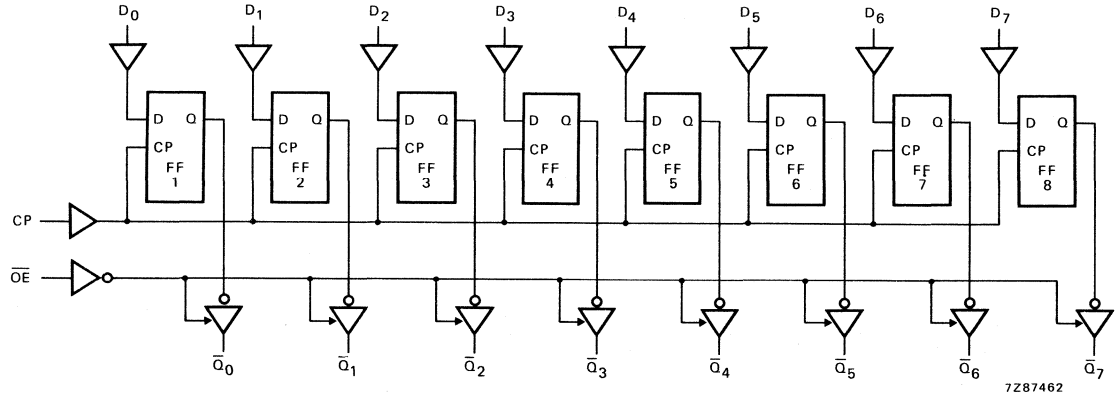


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		500	mW	for standard temperature range; −40 to +85 °C; 74HC/HCT above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		500	mW	for extended temperature range; −55 to +125°C; 54HC/HCT above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
$\overline{OE}$	1.25
CP	0.90
D_n	0.35

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to CP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$			30		38		45	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	25			31		38		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	20			25		30		ns	4.5	Fig. 8
t_h	hold time D_n to CP	5			5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	22			18		15		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

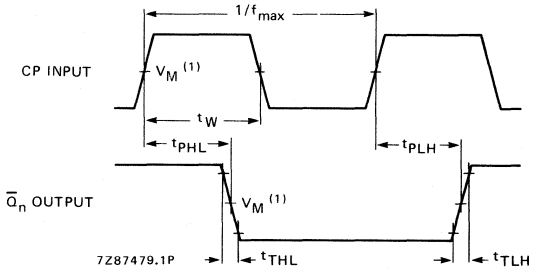


Fig. 6 Waveforms showing the clock (CP) to output ($\overline{Q}_n$) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

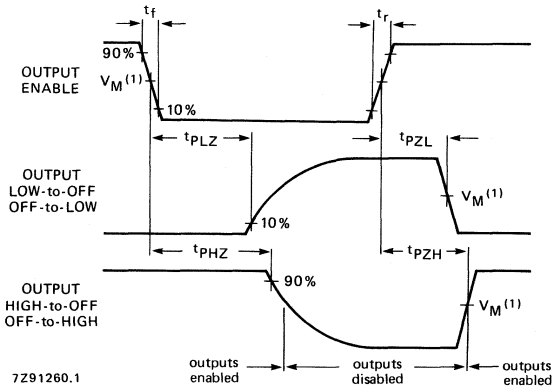


Fig. 7 Waveforms showing the 3-state enable and disable times.

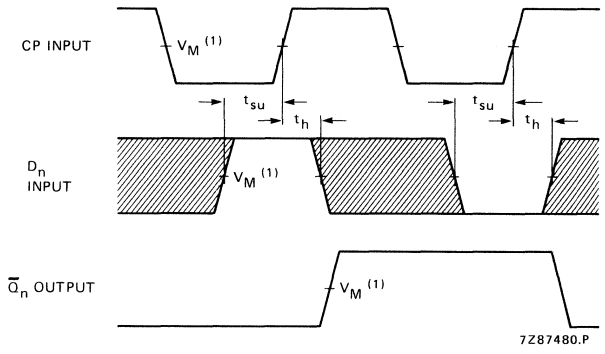


Fig. 8 Waveforms showing the data set-up and hold times for D_n input.

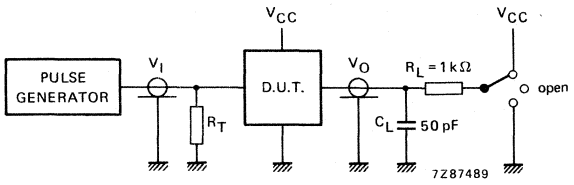
Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 9 Test circuit for 3-state outputs.

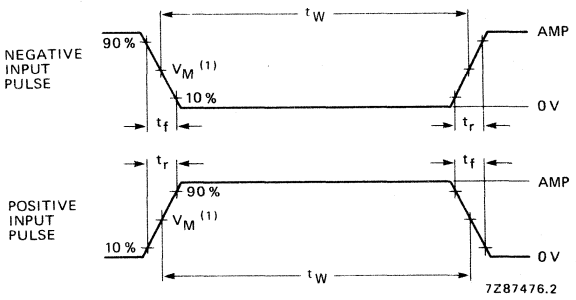


Fig. 10 Input pulse definitions.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- **Inverting outputs**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT540 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$. A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "540" is identical to the "541" but has inverting outputs.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	A_n	$\overline{Y}_n$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF V_{CC} = 5 V	9	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT540P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT540T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}_0$ to $\overline{Y}_7$	bus outputs
20	V_{CC}	positive supply voltage

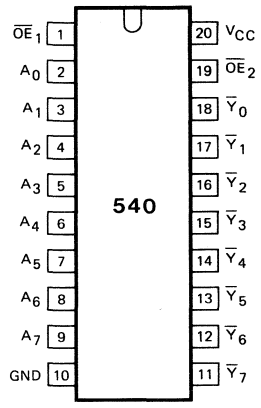


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT541 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT541 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.
A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "541" is identical to the "540" but has non-inverting outputs.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF V_{CC} = 5 V	9	10	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT541P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT541T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_7	bus outputs
20	V_{CC}	positive supply voltage

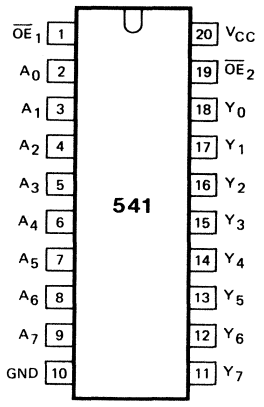


Fig. 1 Pin configuration.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessor
- Common 3-state output enable input
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT563 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT563 are octal D-type transparent latches featuring separate D-type inputs for each latch and inverting 3-state outputs for bus oriented applications.
A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "563" is functionally identical to the "573", but has inverted outputs.

The "563" consists of eight D-type transparent latches with 3-state inverting outputs. The LE and $\overline{OE}$ are common to all latches.
When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.
When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs.
When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n, LE to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	14	14	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT563P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT563T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state latch outputs
20	V_{CC}	positive supply voltage

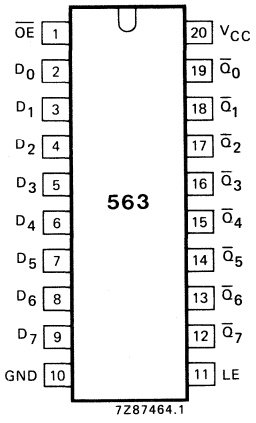


Fig. 1 Pin configuration.

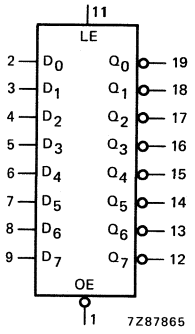


Fig. 2 Logic symbol.

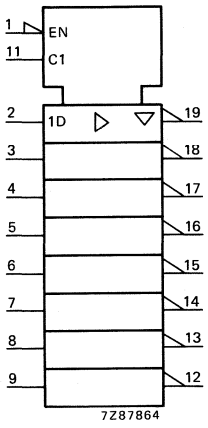


Fig. 3 IEC logic symbol.

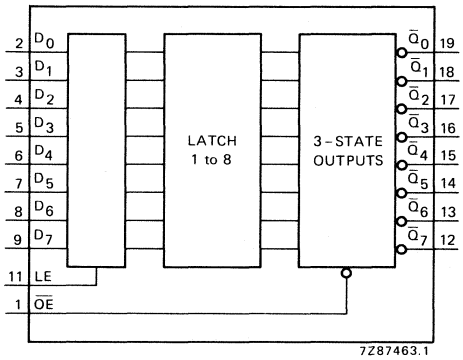


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
enable and read register	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	l	L	H
	L	L	h	H	L
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition

L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition

Z = high impedance OFF-state

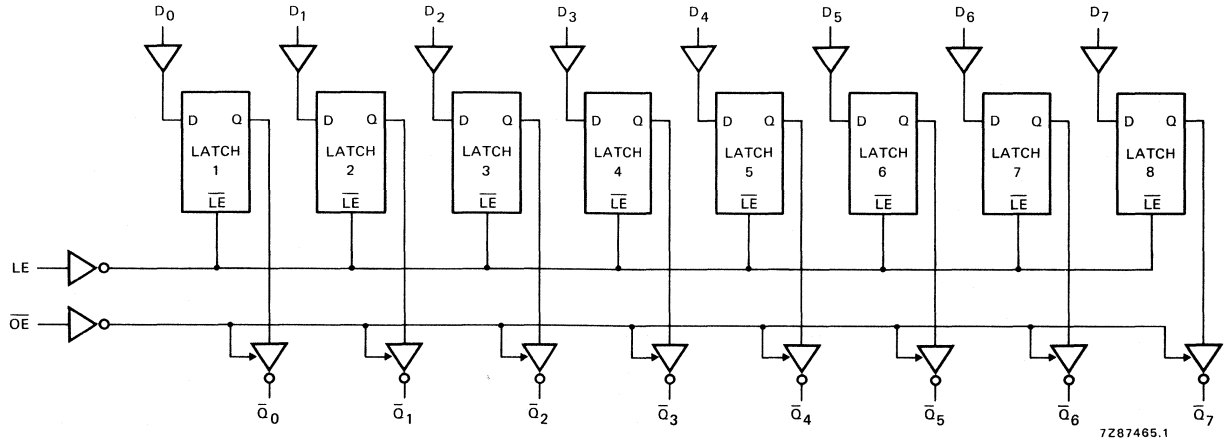


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_n	0.35
$\overline{LE}$	0.65
$\overline{OE}$	1.25

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	enable pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_n to LE	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_n to LE	4 4 4			4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 9

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$			35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$			35		44		53	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			40		50		60	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			40		50		60	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6
t_W	enable pulse width HIGH	16			20		24		ns	4.5	Fig. 7
t_{su}	set-up time D_n to LE	20			25		30		ns	4.5	Fig. 9
t_h	hold time D_n to LE	5			5		5		ns	4.5	Fig. 9

AC WAVEFORMS

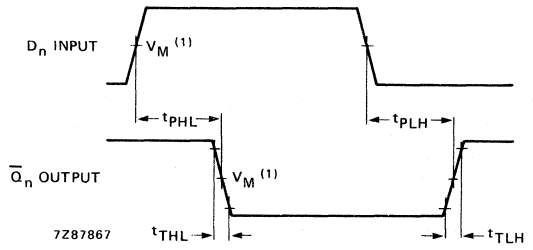


Fig. 6 Waveforms showing the data input (D_n) to output ($\overline{Q}_n$) propagation delays and the output transition times.

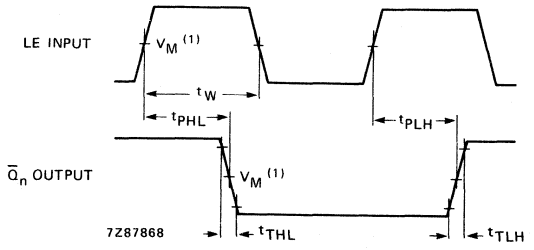


Fig. 7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ($\overline{Q}_n$) propagation delays and the output transition times.

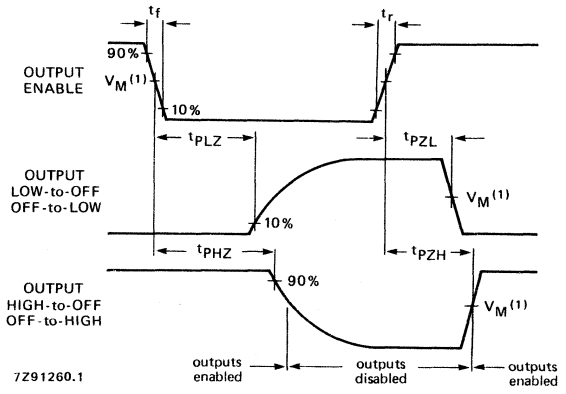


Fig. 8 Waveforms showing the 3-state enable and disable times.

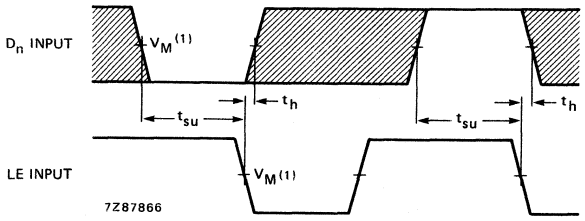


Fig. 9 Waveforms showing the data set-up and hold times for D_n input to LE input

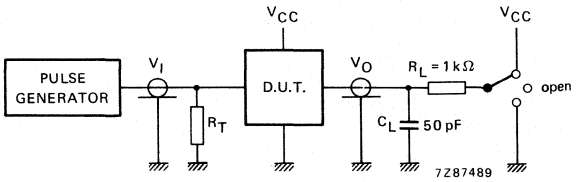
Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 10 Test circuit for 3-state outputs.

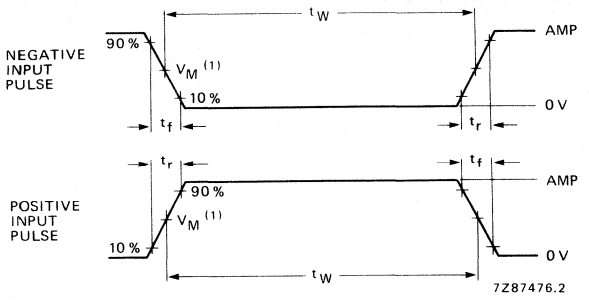


Fig. 11 Input pulse definitions.

Definitions for Figs 10 and 11:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT564 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT564 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "564" is functionally identical to the "574", but has inverting outputs. The "564" is functionally identical to the "534", but has a different pinning.

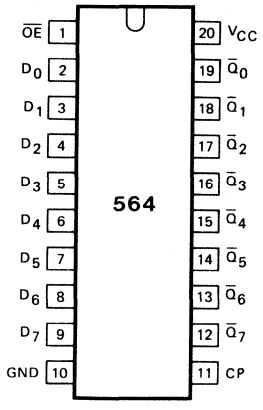


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	12	12	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT564P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT564T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state flip-flop outputs
20	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L	↑	l	L	H
	L	↑	h	H	L
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE

FEATURES

- **Inputs and outputs on opposite sides of package allowing easy interface with microprocessors**
- **Useful as input or output port for microprocessors/microcomputers**
- **3-state non-inverting outputs for bus oriented applications**
- **Common 3-state output enable input**
- **Functionally identical to the "563" and "373"**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$ LE to $\overline{Q}_n$	C_L = 15 pF V_{CC} = 5 V	13 13	17 15	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	26	26	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT573P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT573T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state latch outputs
20	V_{CC}	positive supply voltage

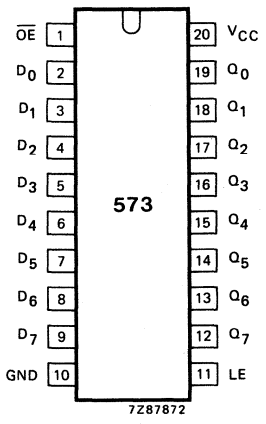


Fig. 1 Pin configuration.

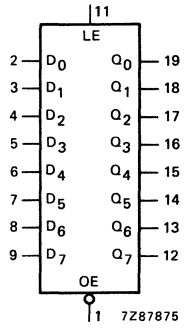


Fig. 2 Logic symbol.

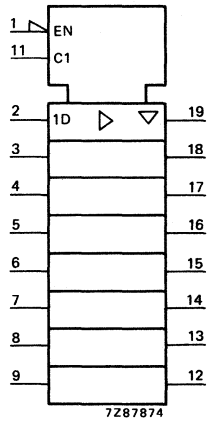


Fig. 3 IEC logic symbol.

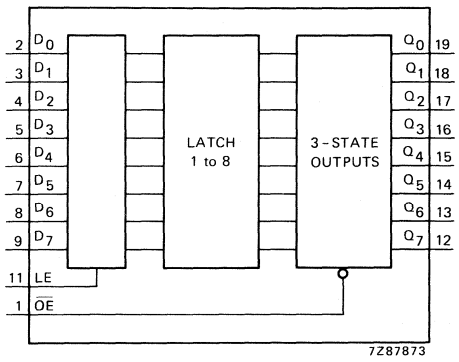


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd.)

The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	L	l	L	L
	L	L	h	H	H
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition

L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition

Z = high impedance OFF-state

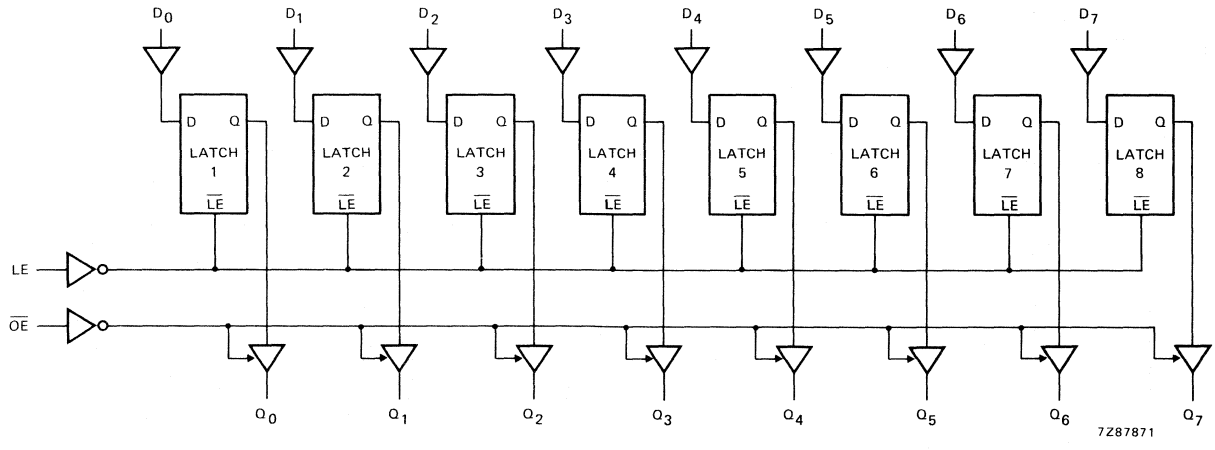


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_n	0.35
LE	0.65
$\overline{OE}$	1.25

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n			190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	enable pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_n to LE	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_n to LE	30 6 5			40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 9

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n			40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n			36		45		54	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n			34		43		51	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n			38		48		57	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6
t_W	enable pulse width HIGH	16			20		24		ns	4.5	Fig. 7
t_{su}	set-up time D_n to LE	14			18		21		ns	4.5	Fig. 9
t_h	hold time D_n to LE	9			11		14		ns	4.5	Fig. 9

AC WAVEFORMS

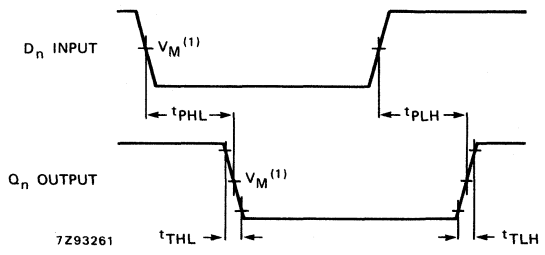


Fig. 6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.

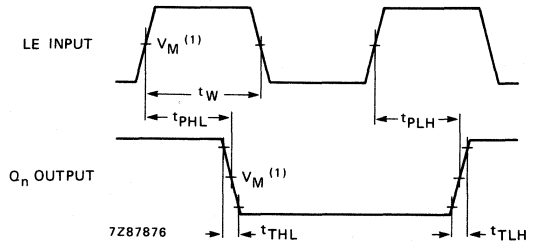


Fig. 7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

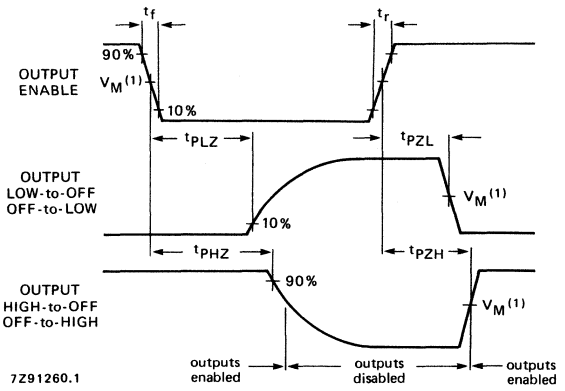


Fig. 8 Waveforms showing the 3-state enable and disable times.

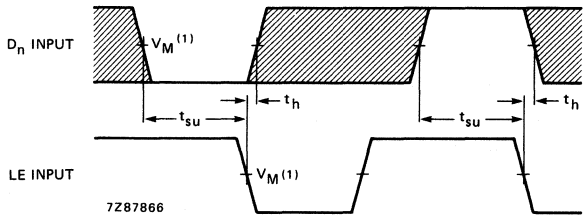


Fig. 9 Waveforms showing the data set-up and hold times for D_n input to LE input.

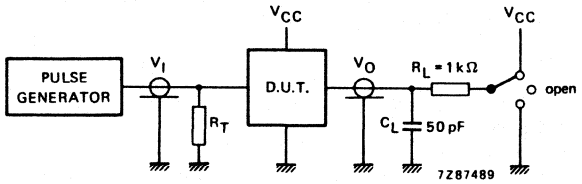
Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 10 Test circuit for 3-state outputs.

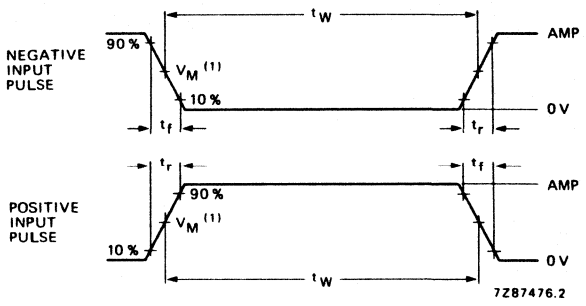


Fig. 11 Input pulse definitions.

Definitions for Figs 10 and 11:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT574 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT574 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "574" is functionally identical to the "564", but has non-inverting outputs. The "574" is functionally identical to the "374", but has a different pinning.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	12	12	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT574P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT574T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state flip-flop outputs
20	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

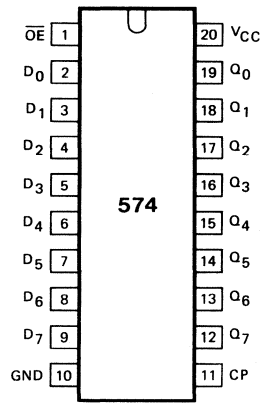


Fig. 1 Pin configuration.

4-BIT FULL ADDER WITH FAST CARRY

FEATURES

- Adds two decimal numbers
- Full internal look-ahead
- Fast ripple carry for economical expansion
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT583 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT583 are high-speed 4-bit BCD full adders with internal carry look-ahead. They accept two 4-bit decimal numbers (A_0 to A_3 and B_0 to B_3) and a carry input (C_{IN}).

The "583" generates the decimal sum outputs (Σ_0 to Σ_3) and a carry output (C_{n+4}) if the sum is greater than 9. See the "283" for the binary version.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n, B_n, C_{IN} to Σ_n C_{IN} to C_{n+4} A_n, B_n to C_{n+4}	C_L = 15 pF V_{CC} = 5 V	 17 10 12	 21 14 17	 ns ns ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT583P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT583D; PC74HC/HCT583D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT583T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5	C_{IN}	carry input
6	C_{n+4}	carry output
8	GND	ground (0 V)
11, 10, 7, 9	Σ_0 to Σ_3	sum outputs
12, 1, 2, 3	B_0 to B_3	B operand inputs
13, 14, 15, 4	A_0 to A_3	A operand inputs
16	V_{CC}	positive supply voltage

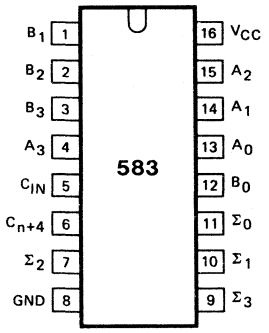


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

8-BIT SHIFT REGISTER WITH INPUT LATCHES

FEATURES

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT597 consist each of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		50	45	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT597D; PC74HC/HCT597P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT597D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT597T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	$\overline{MR}$	asynchronous reset input (active LOW)
11	SH_{CP}	shift clock input (LOW-to-HIGH, edge-triggered)
12	ST_{CP}	storage clock input (LOW-to-HIGH, edge-triggered)
13	$\overline{PL}$	parallel load input (active LOW)
14	D_S	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D_0 to D_7	parallel data inputs
16	V_{CC}	positive supply voltage

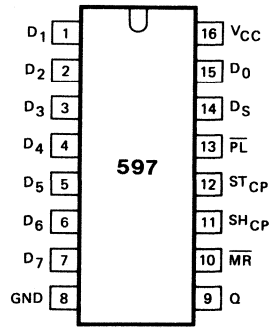


Fig. 1 Pin configuration.

FUNCTION TABLE

ST_{CP}	SH_{CP}	$\overline{PL}$	$\overline{MR}$	FUNCTION
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input latches to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$, $Q_0 = D_S$

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition

OCTAL BUS TRANSCEIVER; 3-STATE; INVERTING

FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

The "640" is similar to the "245" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF; V_{CC} = 5 V	8	9	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT640P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT640T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

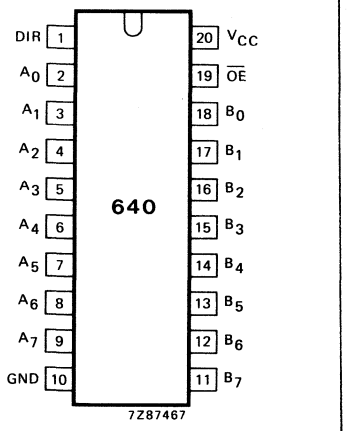


Fig. 1 Pin configuration.

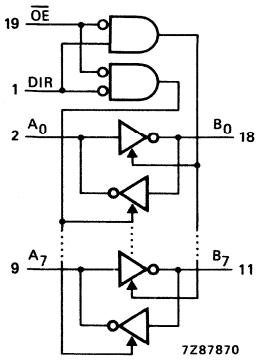


Fig. 2 Logic symbol.

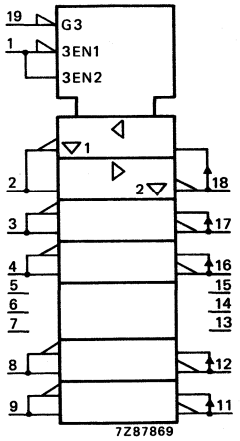


Fig. 3 IEC logic symbol.

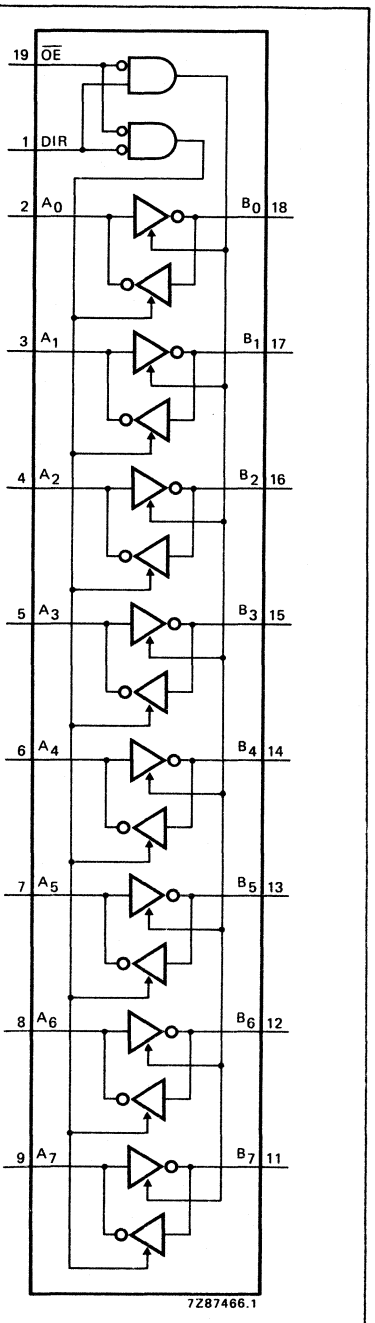


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

FUNCTION TABLE

inputs		inputs/outputs	
$\overline{OE}$	DIR	A_n	B_n
L	L	A=$\overline{B}$	inputs
L	H	inputs	B=$\overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current A_n and B_n			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current (note 1)			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

Note

1. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND. This is because an input stage is connected to the terminal permanently.

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current A_n and B_n			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current (note 2)			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

2. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND.
   This is because an input stage is connected to the terminal permanently.

input	unit load coefficient
A_n	1.50
B_n	1.50
$\overline{OE}$	1.50
DIR	0.90

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n			22		28		33	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n			34		43		51	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n			34		43		51	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

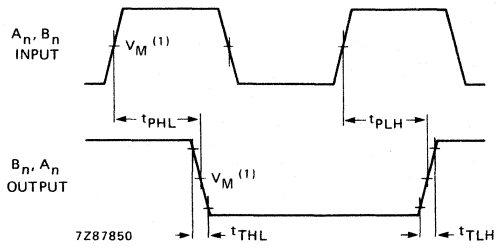


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

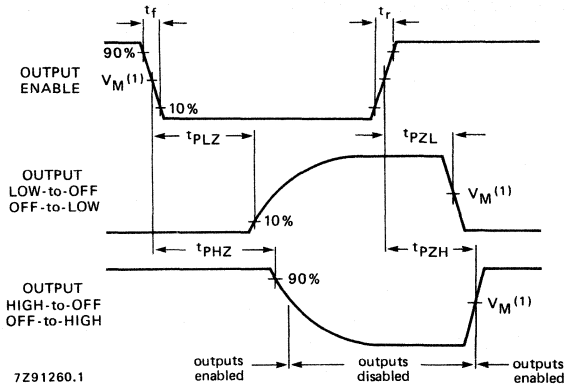
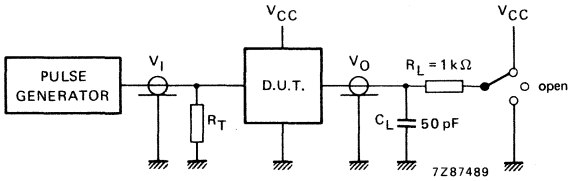


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 7 Test circuit for 3-state outputs.

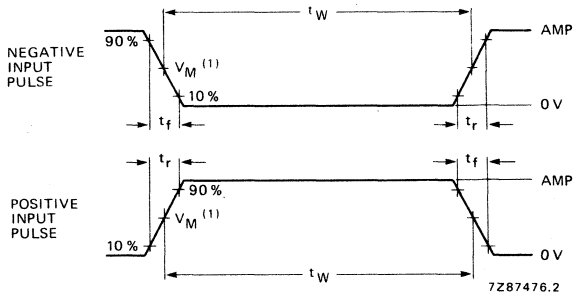


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

OCTAL BUS TRANSCEIVER; 3-STATE; TRUE/INVERTING

FEATURES

- **Octal bidirectional bus interface**
- **True and inverting 3-state outputs**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT643 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT643 are octal transceivers featuring true and inverting 3-state bus compatible outputs in both send and receive directions.

The "643" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; inverting B_n to A_n; true	C_L = 15 pF V_{CC} = 5 V	8 8	8 10	ns ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	42	44	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT643P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT643T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

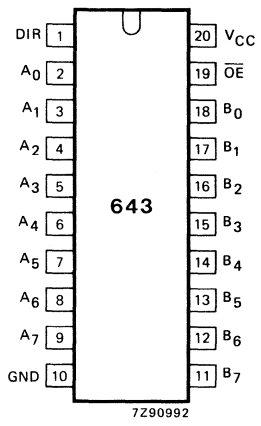


Fig. 1 Pin configuration.

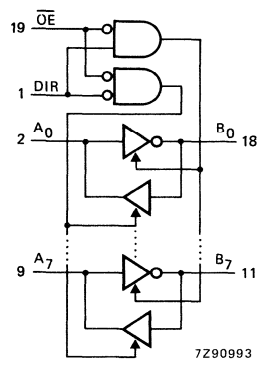


Fig. 2 Logic symbol.

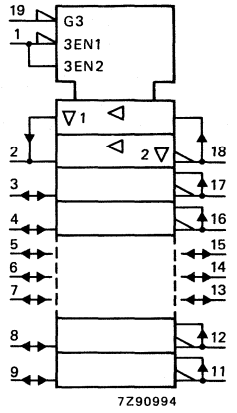


Fig. 3 IEC logic symbol.

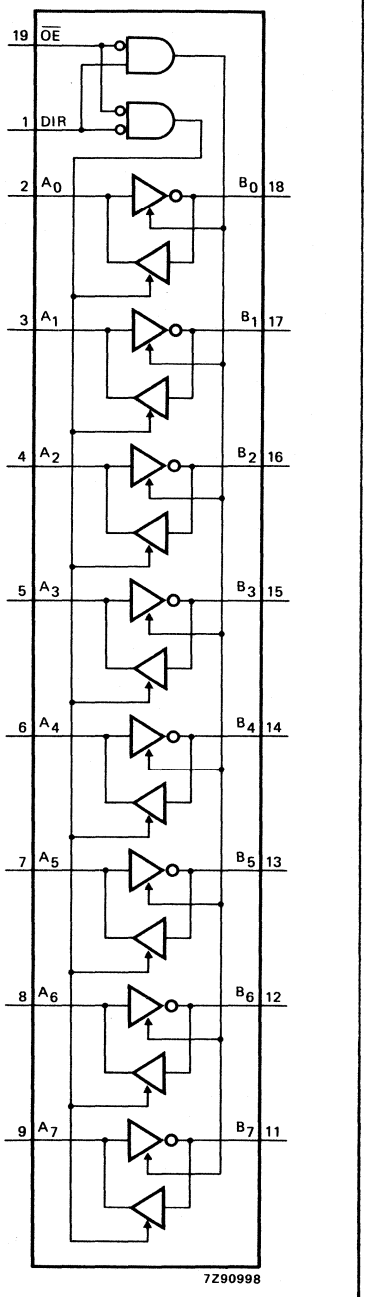


Fig. 4 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60°C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current A_n and B_n			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current (note 1)			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

Note

1. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND. This is because an input stage is connected to the terminal permanently.

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current A_n and B_n			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current (note 2)			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

2. When testing I_{CC}, transceiver outputs in the high-impedance OFF-state (Z) have to be connected to V_{CC} or GND.
   This is because an input stage is connected to the terminal permanently.

input	unit load coefficient
A_n	1.50
B_n	0.40
$\overline{OE}$	1.50
DIR	0.90

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; inverting			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5
t_{PHL}/t_{PLH}	propagation delay B_n to A_n; non-inverting (true)			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 5 and 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; inverting			20		25		30	ns	4.5	Fig. 5
t_{PHL}/t_{PLH}	propagation delay B_n to A_n; non-inverting (true)			26		33		39	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n			36		45		54	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n			36		45		54	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Figs 5 and 6

AC WAVEFORMS

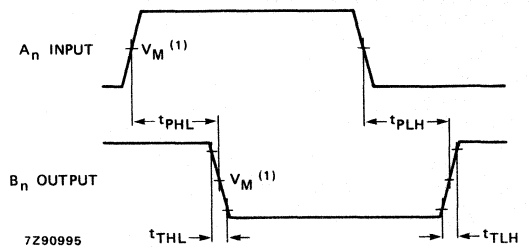


Fig. 5 Waveforms showing the input (A_n) to output (B_n) propagation delays and the output transition times.

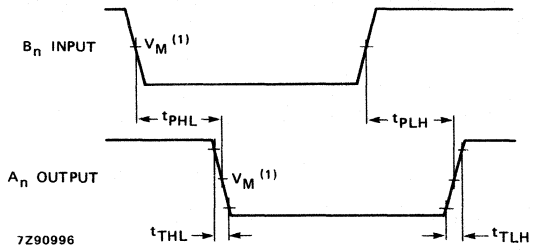


Fig. 6 Waveforms showing the input (B_n) to output (A_n) propagation delays and the output transition times.

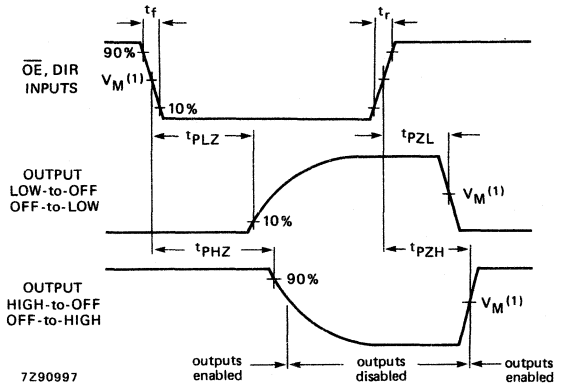


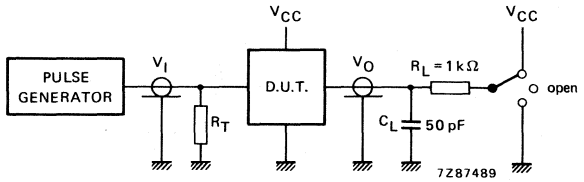
Fig. 7 Waveforms showing the 3-state enable and disable times for $\overline{OE}$ and DIR inputs.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DEVELOPMENT DATA

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 8 Test circuit for 3-state outputs.

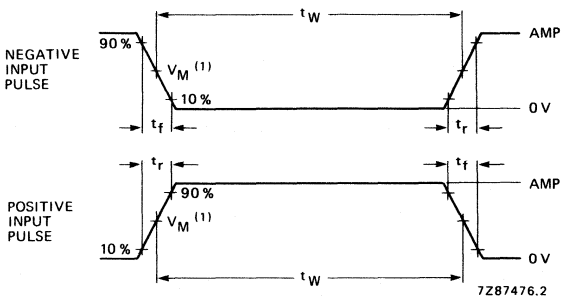


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

OCTAL BUS TRANSCEIVER/REGISTER; 3-STATE

FEATURES

- **Independent register for A and B buses**
- **Multiplexed real-time and stored data**
- **Output capability: bus driver**

GENERAL DESCRIPTION

The 54/74HC/HCT646 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT646 consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CP_{AB} and CP_{BA}) goes to a HIGH logic level. Latch enable ($\overline{LE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{LE}$ is active (LOW). In the isolation mode ($\overline{LE}$ = HIGH), "A" data may be stored in the "B" register and/or "B" data may be stored in the "A" register.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n to A_n	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT646P: 24-lead DIL; plastic (SOT-101A).
PC54HC/HCT646D; PC74HC/HCT646D: 24-lead DIL; ceramic (cerdip) (SOT-94).
PC74HC/HCT646T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	A to B clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	A data inputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	B_0 to B_7	B data inputs
21	$\overline{LE}$	latch enable input (active LOW)
22	S_{BA}	select B to A source input
23	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	positive supply voltage

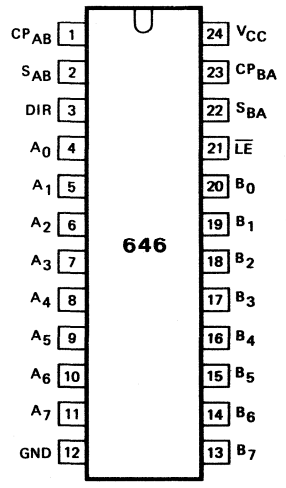


Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The "646" is functionally identical to the "648", but has non-inverting data paths.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{LE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
H H	X X	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
L L	L L	X X	X X	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{LE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

OCTAL BUS TRANSCEIVER/REGISTER; 3-STATE; INVERTING

FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT648 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT648 consist of bus transceiver circuits with 3-state inverting outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CP_{AB} and CP_{BA}) goes to a HIGH logic level. Latch enable ($\overline{LE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{LE}$ is active (LOW). In the isolation mode ($\overline{LE}$ = HIGH), "$\overline{A}$" data may be stored in the "B" register and/or "$\overline{B}$" data may be stored in the "A" register.

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SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$, $\overline{B}_n$ to $\overline{B}_n$ to $\overline{A}_n$	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT648P: 24-lead DIL; plastic (SOT-101A).
PC54HC/HCT648D; PC74HC/HCT648D: 24-lead DIL; ceramic (cerdip) (SOT-94).
PC74HC/HCT648T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	A to B clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	$\overline{A}_0$ to $\overline{A}_7$	$\overline{A}$ data inputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	$\overline{B}_0$ to $\overline{B}_7$	$\overline{B}$ data inputs
21	$\overline{LE}$	latch enable input (active LOW)
22	S_{BA}	select B to A source input
23	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	positive supply voltage

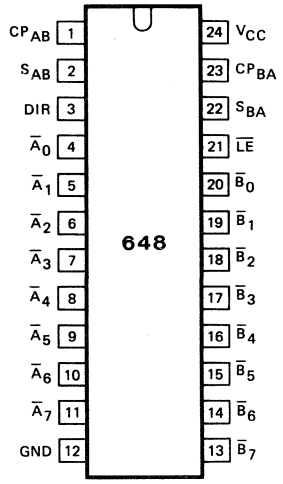

Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The "648" is functionally identical to the "646", but has inverting data paths.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{LE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
H H	X X	H or L ↑	H or L ↑	X X	X X	input	input	isolation store $\overline{A}$ and $\overline{B}$ data
L L	L L	X X	X X	X X	L H	output	input	real-time $\overline{B}$ data to A bus stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time $\overline{A}$ data to B bus stored $\overline{A}$ data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{LE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

4 x 4 REGISTER FILE; 3-STATE

FEATURES

- Simultaneous and independent read and write operations
- Expandable to almost any word size and bit length
- Output capability: standard

GENERAL DESCRIPTION

The 54/74HC/HCT670 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT670 are 16-bit 3-state register files organized as 4 words of 4 bits each. Separated read and write address inputs (R_A, R_B and W_A, W_B) and enable inputs ($\overline{RE}$ and $\overline{WE}$) are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs (D_0 to D_3). The W_A and W_B inputs determine the location of the stored word. When the $\overline{WE}$ input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ input is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs (Q_0 to Q_3). D_n and W_n inputs are inhibited when $\overline{WE}$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual read address inputs (R_A and R_B). The addressed word appears at the four outputs when the $\overline{RE}$ is LOW. Data outputs are in the high impedance OFF-state when $\overline{RE}$ is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

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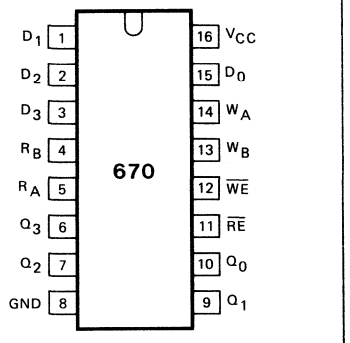


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	22	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT670P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT670D; PC74HC/HCT670D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT670T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4	R_A, R_B	read address inputs
8	GND	ground (0 V)
10, 9, 7, 6	Q_0 to Q_3	data outputs
11	$\overline{RE}$	3-state output read enable input (active LOW)
12	$\overline{WE}$	write enable input (active LOW)
14, 13	W_A, W_B	write address inputs
15, 1, 2, 3	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION (Cont'd)

Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES*
	$\overline{WE}$	D_n	
write data	L L	L H	L H
data latched	H	X	no change

* The write address (W_A and W_B) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT
	$\overline{RE}$	INTERNAL LATCHES**	Q_n
read	L L	L H	L H
disabled	H	X	Z

** The selection of the "internal latches" by read address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

8-BIT MAGNITUDE COMPARATOR

FEATURES

- **Compare two 8-bit words**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT688 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT688 are 8-bit magnitude comparators. They perform comparison of two 8-bit binary or BCD words.
The output provides $\overline{P = Q}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay P_n, Q_n to $\overline{P = Q}$ $\overline{E}$ to $\overline{P = Q}$	C_L = 15 pF V_{CC} = 5 V	14 8	14 8	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT688P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT688T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{E}$	enable input (active LOW)
2, 4, 6, 8, 11, 13, 15, 17	P_0 to P_7	word inputs
3, 5, 7, 9, 12, 14, 16, 18	Q_0 to Q_7	word inputs
10	GND	ground (0 V)
19	$\overline{P = Q}$	equal to output
20	V_{CC}	positive supply voltage

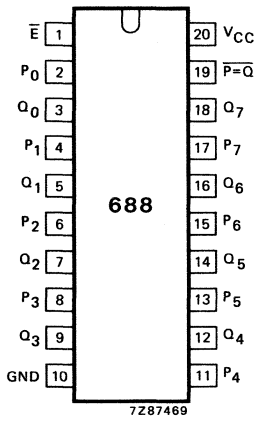


Fig. 1 Pin configuration.

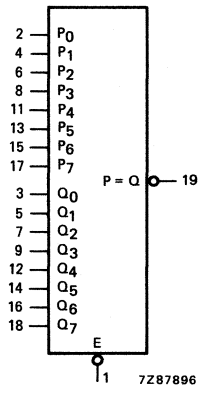


Fig. 2 Logic symbol.

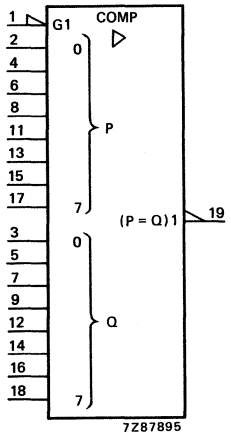


Fig. 3 IEC logic symbol.

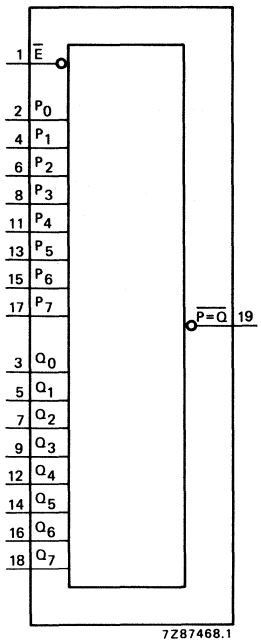


Fig. 4 Functional diagram.

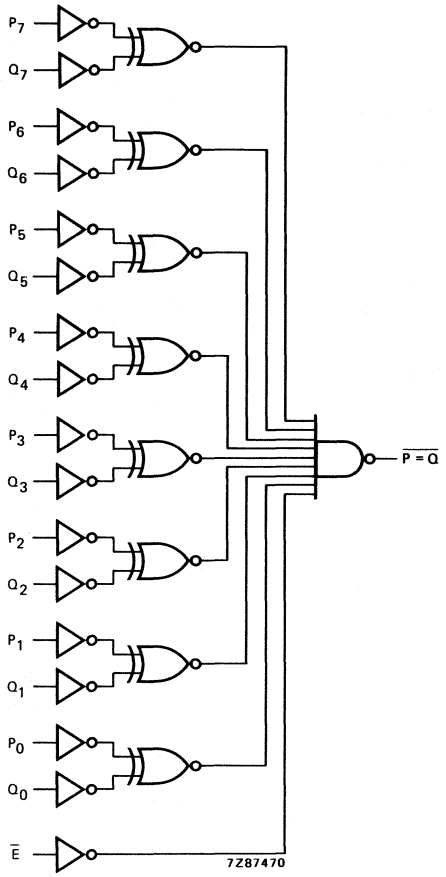


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P_n, Q_n	ENABLE $\overline{E}$	$\overline{P=Q}$
P = Q	L	L
X	H	H
P > Q	L	H
P < Q	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic and ceramic (cerdip) DIL		500	mW	for standard temperature range; −40 to +85 °C; 74HC/HCT above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package ceramic (cerdip) DIL		500	mW	for extended temperature range; −55 to +125°C; 54HC/HCT above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
P_n	0.35
Q_n	0.35
$\overline{E}$	0.70

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay P_n, Q_n to $\overline{P = Q}$			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{P = Q}$			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay P_n, Q_n to $\overline{P = Q}$			34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{P = Q}$			20		25		30	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

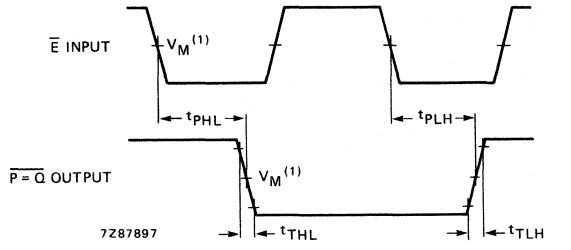


Fig. 6 Waveforms showing the enable input ($\overline{E}$) to the equal to output ($\overline{P = Q}$) propagation delays and the output transition times.

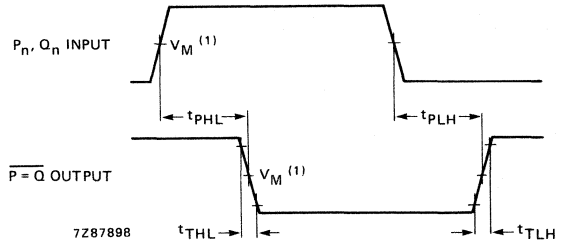


Fig. 7 Waveforms showing the word inputs (P_n, Q_n) to the equal to output ($\overline{P = Q}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

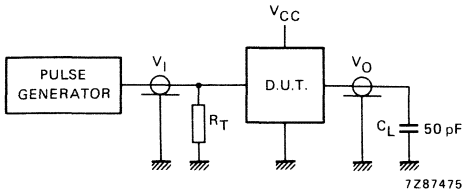


Fig. 8 Test circuit.

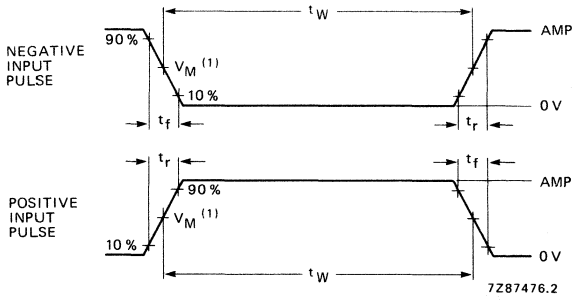


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DUAL 4-INPUT NOR GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4002 are high-speed Si-gate CMOS devices and are pin compatible with "4002" of the "4000B" series. The are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4002 provide the 4-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4002D;
PC74HC/HCT4002P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT4002D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT4002T: 14-lead mini-pack; plastic (SO-14; (SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1Y, 2Y	data outputs
2, 9	1A, 2A	data inputs
3, 10	1B, 2B	data inputs
4, 11	1C, 2C	data inputs
5, 12	1D, 2D	data inputs
6, 8	n.c.	not connected
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

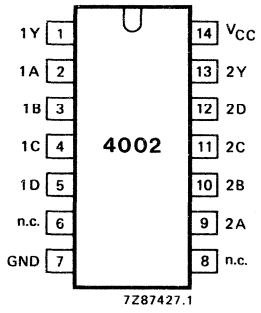


Fig. 1 Pin configuration.

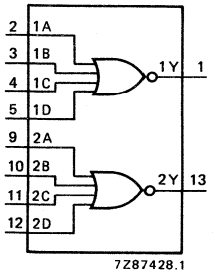


Fig. 2 Logic symbol.

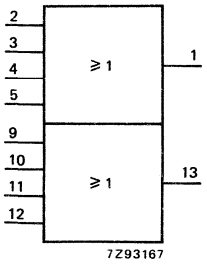


Fig. 3 IEC logic symbol.

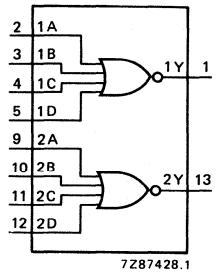


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

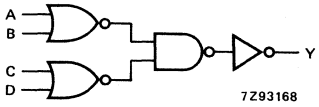


Fig. 5 Logic diagram PC54/74HC4002 (one gate).

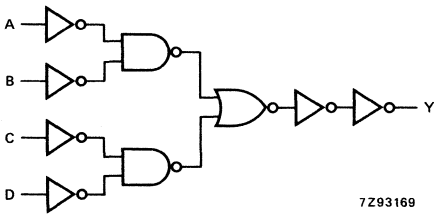


Fig. 6 Logic diagram PC54/74HCT4002 (one gate).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB, nC, nD	0.45

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC, nD to nY			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay nA, nB, nC, nD to nY			27		34		41	ns	4.5	Fig. 7
t_{PLH}	propagation delay nA, nB, nC, nD to nY			24		30		36	ns	4.5	Fig. 7
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS

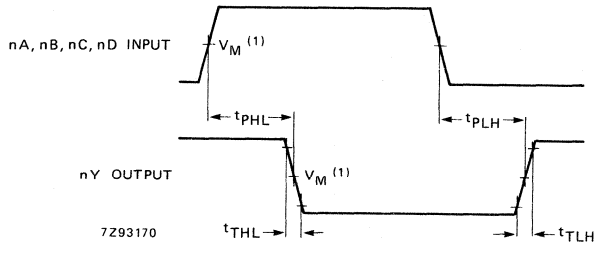


Fig. 7 Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

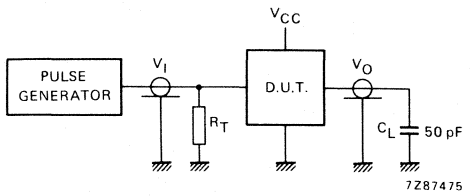


Fig. 8 Test circuit.

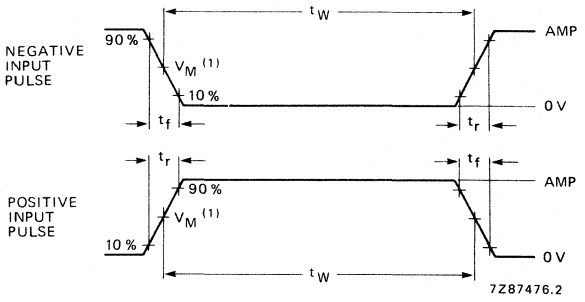


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

DUAL 4-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4015 are high-speed Si-gate CMOS devices and are pin compatible with the "4015" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4015 are dual edge-triggered 4-bit static shift registers (serial-to-parallel converters). Each shift register has a serial data input (1D and 2D), a clock input (1CP and 2CP), four fully buffered parallel outputs ($1Q_0$ to $1Q_3$ and $2Q_0$ to $2Q_3$) and an overriding asynchronous master reset (1MR and 2MR). Information present on nD is shifted to the first register position, and all data in the register is shifted one position to the right on the LOW-to-HIGH transition of nCP. A HIGH on nMR clears the register and forces nQ_0 to nQ_3 to LOW, independent of nCP and nD.

APPLICATIONS

- **Serial-to-parallel converter**
- **Buffer stores**
- **General purpose register**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP to nQ_n	C_L = 15 pF; V_{CC} = 5 V	14	16	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4015D; PC74HC/HCT4015D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4015P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4015T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4, 3, 10	$1Q_0$ to $1Q_3$	flip-flop outputs
6, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
7, 15	1D, 2D	serial data inputs
8	GND	ground (0 V)
9, 1	1CP, 2CP	clock inputs (LOW-to-HIGH, edge-triggered)
13, 12, 11, 2	$2Q_0$ to $2Q_3$	flip-flop outputs
16	V_{CC}	positive supply voltage

FUNCTION TABLE

	INPUTS			OUTPUTS			
n	nCP	nD	nMR	nQ_0	nQ_1	nQ_2	nQ_3
1	↑	D_1	L	D_1	X	X	X
2	↑	D_2	L	D_2	D_1	X	X
3	↑	D_3	L	D_3	D_2	D_1	X
4	↑	D_4	L	D_4	D_3	D_2	D_1
	↓	X	L	no change			
	X	X	H	L	L	L	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition
n = number of clock pulse transitions
D_n = either HIGH or LOW

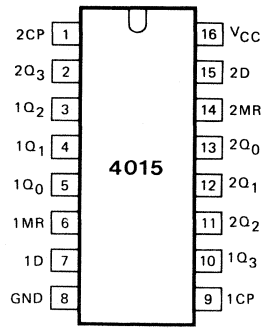


Fig. 1 Pin configuration.

QUAD BILATERAL SWITCHES

FEATURES

- Low "ON" resistance: 160 Ω (typ.) at V_{CC} = 4.5 V
- Individual switch controls

GENERAL DESCRIPTION

The 54/74HC/HCT4016 are high-speed Si-gate CMOS devices and are pin compatible with the "4016" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4016 have four independent analog switches (transmission gates).

Each switch has two input/output terminals (Y_n, Z_n) and an active HIGH enable input (E_n). When E_n is connected to V_{CC}, a low bidirectional path between Y_n and Z_n is established (ON condition). When E_n is connected to ground (GND), the switch is disabled and a high impedance between Y_n and Z_n is established (OFF condition).

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} \geqslant (V_Y, V_Z) \geqslant$ GND. Inputs Y_n and Z_n are electrically equivalent terminals.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	C_L = 15 pF; V_{CC} = 5 V	4	4	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	12	12	pF
C_S	max. switch capacitance		5	5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4016P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT4016D; PC74HC/HCT4016D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT4016T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	Y_0 to Y_3	independent inputs/outputs
7	GND	ground (0 V)
2, 3, 9, 10	Z_0 to Z_3	independent inputs/outputs
13, 5, 6, 12	E_0 to E_3	enable inputs (active HIGH)
14	V_{CC}	positive supply voltage

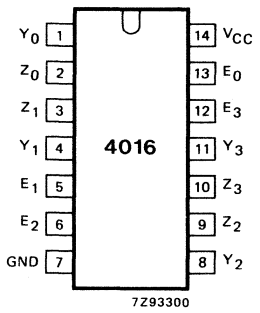


Fig. 1 Pin configuration.

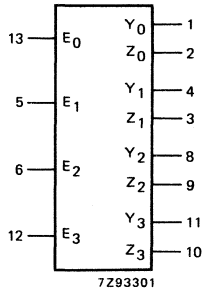


Fig. 2 Logic symbol.

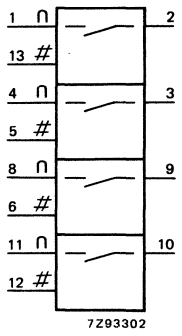


Fig. 3 IEC logic symbol.

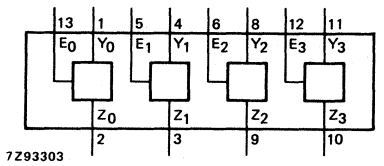


Fig. 4 Functional diagram.

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

FUNCTION TABLE

INPUT E_n	CHANNEL IMPEDANCE
L	high
H	low

H = HIGH voltage level
L = LOW voltage level

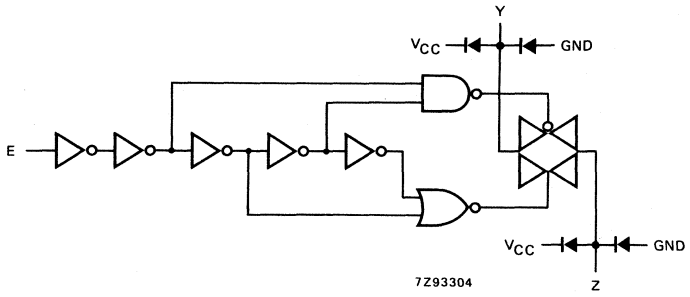


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60 °C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125 °C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_S	DC switch voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC/HCT

For 54/74HC: V_{CC} = 2.0, 4.5 and 6.0 V
For 54/74HCT: V_{CC} = 4.5 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC/HCT			74HC/HCT		54HC/HCT			V_{CC} V	I_S μA	V_{is}
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
R_{ON}	ON resistance		4250 160 120	– 320 240		– 400 300		– 480 360	Ω Ω Ω	2.0 4.5 6.0	100 1000 1000	V_{CC} to GND
R_{ON}	ON resistance		160 80 65	– 160 130		– 200 162		– 240 195	Ω Ω Ω	2.0 4.5 6.0	100 1000 1000	GND
R_{ON}	ON resistance		170 90 75	– 180 150		– 225 187		– 270 225	Ω Ω Ω	2.0 4.5 6.0	100 1000 1000	V_{CC}
ΔR_{ON}	maximum ΔON resistance between any two channels		425 16 12						Ω Ω Ω	2.0 4.5 6.0		V_{CC} to GND
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	6.0	$V_I = V_{IH}$ or V_{IL} $\|V_S\| = V_{CC}$ − GND	
$\pm I_S$	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	6.0	$V_I = V_{IH}$ or V_{IL} $\|V_S\| = V_{CC}$ − GND	
$\pm I_S$	analog switch ON-state current			0.2		2.0		2.0	μA	6.0	$V_I = V_{IH}$ or V_{IL} $\|V_S\| = V_{CC}$ − GND	

Note to DC characteristics

At supply voltages approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is commended that these devices be used to transmit digital signals only, when using these supply voltages.

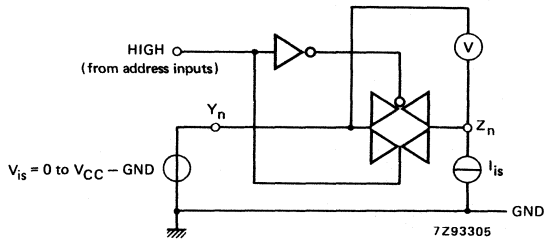


Fig. 6 Test circuit for measuring R_{ON}.

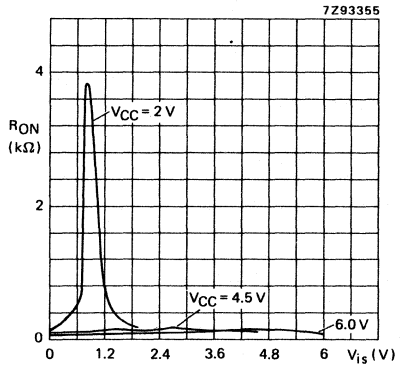


Fig. 7 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC}.

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
E_n	1.00

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	NOTES
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	note 1
t_{PZH}/t_{PZL}	turn "ON" time E_n to V_{os}			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	note 2
t_{PHZ}/t_{PLZ}	turn "OFF" time E_n to V_{os}			145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	note 2

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	NOTES
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}			12		15		18	ns	4.5	note 1
t_{PZH}	turn "ON" time E_n to V_{os}			35		44		53	ns	4.5	note 2
t_{PZL}	turn "ON" time E_n to V_{os}			52		65		78	ns	4.5	note 2
t_{PHZ}/t_{PLZ}	turn "OFF" time E_n to V_{os}			35		44		53	ns	4.5	note 2

AC CHARACTERISTICS FOR 54/74HC/HCT

GND = 0 V; $t_r = t_f$ = 6 ns

For 54/74HC: V_{CC} = 2.0, 4.5 and 6.0 V
For 54/74HCT: V_{CC} = 4.5 V

SYMBOL	PARAMETER	min.	typ.	max.	UNIT	V_{CC} V	NOTES
	distortion, sine-wave response		— 0.8 0.5		% % %	2.0 4.5 6.0	note 3
	crosstalk between any two channels				MHz MHz MHz	2.0 4.5 6.0	note 4
	crosstalk between enable or address input to output				mV mV mV	2.0 4.5 6.0	note 5
	OFF-state feed-through				MHz MHz MHz	2.0 4.5 6.0	note 6
	ON-state frequency response		100		MHz MHz MHz	2.0 4.5 6.0	note 7
C_S	maximum switch capacitance		5		pF		

Notes to AC characteristics

V_{is} is the input voltage at an Y_n or Z_n terminal, whichever is assigned as an input.
V_{os} is the output voltage at an Y_n or Z_n terminal, whichever is assigned as an output.

1. C_L = 50 pF to GND; $E_n = V_{CC}$; $V_{is} = V_{CC}$ (square wave); see Fig. 8.
2. R_L = 1 kΩ; C_L = 50 pF to GND; $E_n = V_{CC}$ (square wave);
   V_{is} = GND and R_L to GND for t_{PZH} and t_{PHZ}; see Fig. 9;
   V_{is} = GND and R_L to V_{CC} for t_{PZL} and t_{PLZ}; see Fig. 9.
3. R_L = 10 kΩ; C_L = 15 pF; $E_n = V_{CC}$; $V_{is} = 1/2V_{CC(p\text{-}p)}$ (sine-wave, symmetrical about $1/2V_{CC}$);
   f_{is} = 1 kHz; see Fig. 12.
4. R_L=10 kΩ; $V_{is} = 1/2V_{CC(p\text{-}p)}$ (sine-wave, symmetrical about $1/2V_{CC}$);
   $20 \log \frac{V_{os}\,(B)}{V_{is}\,(A)} = -50$ dB; E_n (A) = GND; E_n(B) = V_{CC}; see Figs 10 and 11.
5. R_L = 10 kΩ; C_L = 15 pF to GND; $E_n = V_{CC}$ (square wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 12.
6. R_L = 1 kΩ; C_L = 5 pF; E_n = GND; $V_{is} = 1/2V_{CC(p\text{-}p)}$ (sine-wave, symmetrical about $1/2V_{CC}$);
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 12.
7. R_L = 1 kΩ; C_L = 5 pF; $E_n = V_{CC}$; $V_{is} = 1/2V_{CC(p\text{-}p)}$ (sine-wave, symmetrical about $1/2V_{CC}$);
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 12.

AC WAVEFORMS

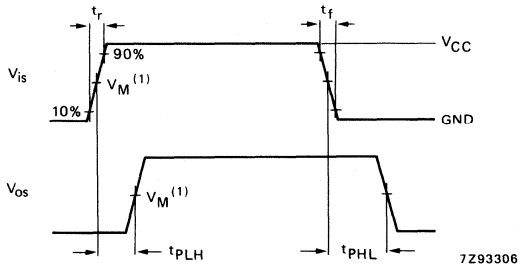


Fig. 8 Waveforms showing the propagation delays from V_{is} to V_{os}.

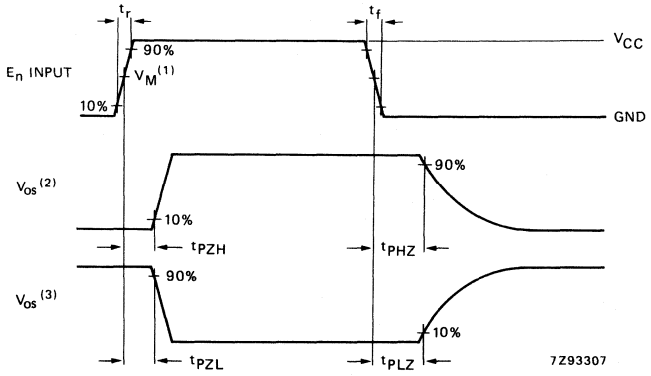


Fig. 9 Waveforms showing the output disable and enable times.

Notes to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

(2) V_{is} at V_{CC}.

(3) V_{is} at GND.

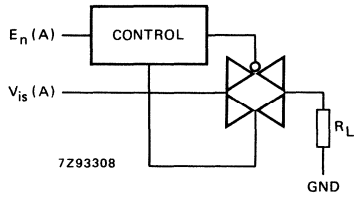


Fig. 10 Switch example "A".

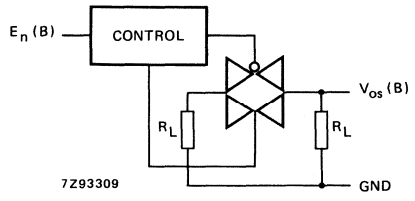
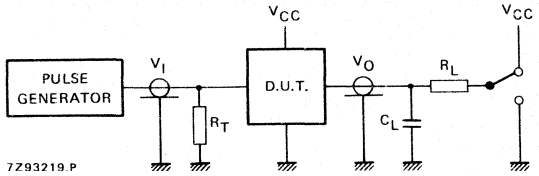


Fig. 11 Switch example "B".

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	GND

Fig. 12 Test circuit for 3-state outputs.

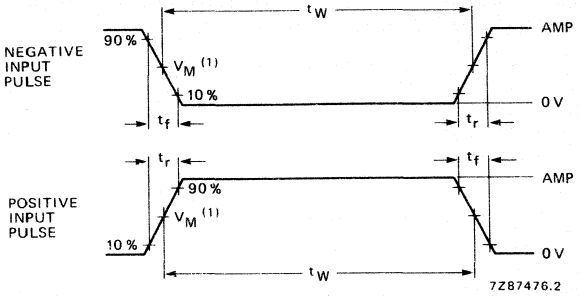


Fig. 13 Input pulse definitions.

Definitions for Figs 12 and 13:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

JOHNSON DECADE COUNTER WITH 10 DECODED OUTPUTS

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the "4017" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs (Q_0 to Q_9), an active LOW output from the most significant flip-flop ($\overline{Q}_{5\text{-}9}$), active HIGH and active LOW clock inputs (CP_0 and $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH-to-LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table).

When cascading counters, the $\overline{Q}_{5\text{-}9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($Q_0 = \overline{Q}_{5\text{-}9}$ = HIGH; Q_1 to Q_9 = LOW) independent of the clock inputs (CP_0 and $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_0, $\overline{CP}_1$ to Q_n	C_L = 15 pF; V_{CC} = 5 V	14	16	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4017P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4017D; PC74HC/HCT4017D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4017T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 3, 7, 10, 1, 5, 6, 9, 11	Q_0 to Q_9	decoded outputs
8	GND	ground (0 V)
12	$\overline{Q}_{5\text{-}9}$	carry output (active LOW)
13	$\overline{CP}_1$	clock input (HIGH-to-LOW, edge-triggered)
14	CP_0	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	OPERATION
H	X	X	$Q_0 = \overline{Q}_{5\text{-}9}$ = H; Q_1 to Q_9 = L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

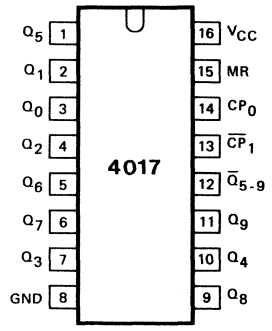


Fig. 1 Pin configuration.

14-STAGE BINARY RIPPLE COUNTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the "4020" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4020 are 14-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0, Q_3 to Q_{13}).

The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_0, Q_3 to Q_{13}
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0	C_L = 15 pF; V_{CC} = 5 V	12	18	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4020D; PC74HC/HCT4020P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4020D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4020T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q_0, Q_3 to Q_{13}	parallel outputs
8	GND	ground (0 V)
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

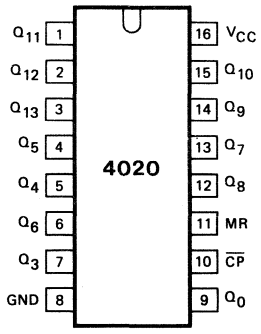


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

7-STAGE BINARY RIPPLE COUNTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4024 are high-speed Si-gate CMOS devices and are pin compatible with the "4024" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4024 are 7-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q_0 to Q_6).

The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

APPLICATIONS

- **Frequency dividing circuits**
- **Time delay circuits**

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_n
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0	C_L = 15 pF; V_{CC} = 5 V	12	18	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4024P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT4024D; PC74HC/HCT4024D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT4024T: 14-lead mini-pack; plastic (SO-16; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
2	MR	master reset input (active HIGH)
12, 11, 9, 6, 5, 4, 3	Q_0 to Q_6	parallel outputs
7	GND	ground (0 V)
8, 10, 13	n.c.	not connected
14	V_{CC}	positive supply voltage

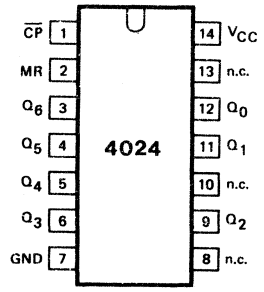


Fig. 1 Pin configuration.

12-STAGE BINARY RIPPLE COUNTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the "4040" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4040 are 12-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0 to Q_{11}).

The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

APPLICATIONS

- **Frequency dividing circuits**
- **Time delay circuits**
- **Control counters**

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_n
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

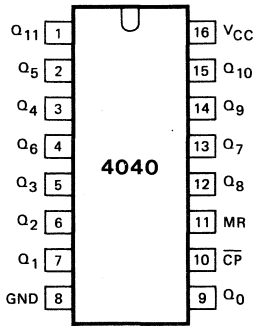


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0	C_L = 15 pF; V_{CC} = 5 V	10	18	ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4040P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4040D; PC74HC/HCT4040D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4040T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q_0 to Q_{11}	parallel outputs
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PHASE-LOCKED-LOOP WITH VCO

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4046 are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4046 are phase-locked-loop circuits that consist of a linear voltage controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

VCO part

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency off-set if required.

The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at pin 10 (SF_{OUT}). If SF_{OUT} is used, a load resistor (R_{SF}) should be connected from SF_{OUT} to GND; if unused, SF_{OUT} should be left open. The VCO output (VCO_{OUT}) can either be connected directly to the comparator input ($COMP_{IN}$) or via a frequency divider.

A LOW level at the inhibit input (INH) enables the VCO and source-follower, while a HIGH level turns off both to minimize stand-by power consumption.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_{max}	maximum clock frequency	C_L = 15 pF V_{CC} = 5 V	15	15	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4046P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4046D; PC74HC/HCT4046D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4046T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	phase comparator pulse output
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	SF_{OUT}	source-follower output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	$SIGN_{IN}$	signal input
15	$PC3_{OUT}$	phase comparator 3 output
16	V_{CC}	positive supply voltage

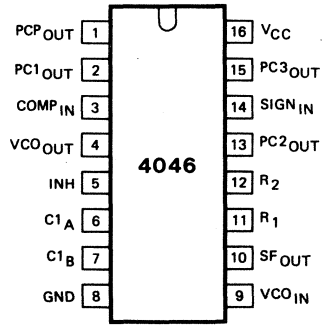


Fig. 1 Pin configuration.

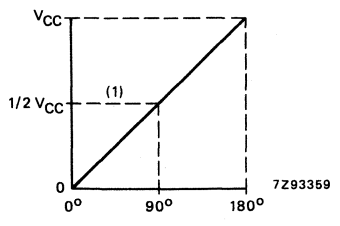
GENERAL DESCRIPTION (Cont'd)

Phase comparators

The phase-comparator signal input ($SIGN_{IN}$) can be direct-coupled, provided the signal swing is between the standard HC/HCT family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at $SIGN_{IN}$ in case of smaller swings.

Phase comparator 1 (PC1) is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50% duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to $1/2V_{CC}$ when there is no signal or noise at $SIGN_{IN}$. The average voltage to the VCO input (VCO_{IN}) is supplied by the low-pass filter connected to the output of PC1 ($PC1_{OUT}$). This also causes the VCO to oscillate at the centre frequency (f_o). The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. PC1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal. A typical behaviour of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO centre frequency. Another typical behaviour is, that the phase angle between the signal and comparator input varies between 0° and 180° and is 90° at the centre frequency. Figure 2 shows the typical phase-to-output response characteristics.



(1) Average output voltage.

Fig. 2 Signal-to-comparator inputs phase difference for PC1;

$PC1_{OUT} = (V_{CC}/\pi)(\phi_{IN} - \phi_{OUT})$.

Figure 3 shows the typical waveforms for PLL employing PC1 in locked condition of f_o.

Phase comparator 2 (PC2) is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers having a common output mode. When the p-type or n-type drivers are "ON", they pull the output up to V_{CC} or down to GND respectively. This type of phase comparator only acts on the positive-going edges of the signals at $SIGN_{IN}$ and $COMP_{IN}$. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained "ON" most of the time, and both the n and p-type drivers are "OFF" (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained "ON" most of the time, and both the n and p-type drivers are "OFF" the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained "ON" for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained "ON" for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to this PC2 is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain "OFF" and thus the phase comparator output ($PC2_{OUT}$) becomes an open circuit and keeps the voltage at C2 constant.

Moreover, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level which can be used for indicating a locked condition. Thus, for PC2 no phase difference exists between $SIGN_{IN}$ and $COMP_{IN}$ over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase

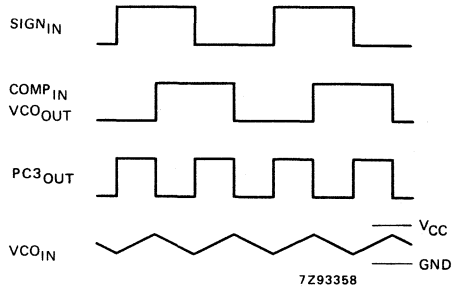


Fig. 3 Typical waveforms for PLL employing PC1 in locked condition of f_o.

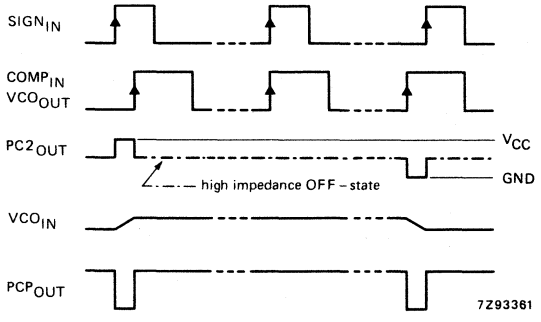


Fig. 4 Typical waveforms for a PLL employing PC2 in locked condition.

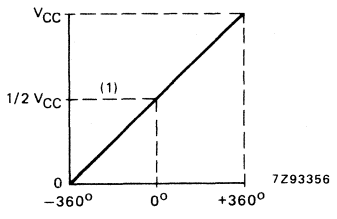
GENERAL DESCRIPTION (Cont'd)

comparator is equal to the capture range, independent of the low-pass filter. With no signal present at $SIGN_{IN}$, the VCO is adjusted to its lowest frequency for PC2. Figure 4 shows typical waveforms for a PLL employing this type of phase comparator in locked condition.

Figure 5 shows the typical phase-to-output response characteristics.

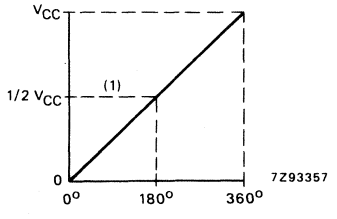
Phase comparator 3 (PC3) is a sequential phase detector with a typical phase characteristic given in Fig. 6. Figure 7 shows the typical waveforms for a PLL employing PC3 in locked condition. PC3 is very similar to PC2, but its phase angle between $SIGN_{IN}$ and $COMP_{IN}$ varies between 0° and 360° and is 180° at the centre frequency.

For proper operation it is recommended that the cut-off frequency of the low-pass filter is less or equal to fo/20.



(1) Average output voltage.

Fig. 5 Signal-to-comparator inputs phase difference for PC2;
$PC2_{OUT} = (V_{CC}/4\pi)(\phi_{IN} - \phi_{OUT})$.



(1) Average output voltage.

Fig. 6 Signal-to-comparator inputs phase difference for PC3;
$PC3_{OUT} = (V_{CC}/2\pi)(\phi_{IN} - \phi_{OUT})$.

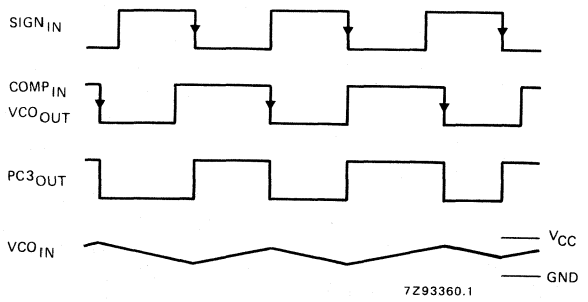


Fig. 7 Typical waveforms for a PLL employing PC3 in locked condition.

PHASE-LOCKED-LOOP WITH LOCK DETECTOR

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4046-1 are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4046-1 are phase-locked-loop circuits that consist of a linear voltage controlled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input. At pin 1 (LD) a lock detector is provided, which gives a HIGH voltage level when the PLL is locked.
The lock detector capacitor must be connected between pin 15 (C_{LD}) and pin 8 (GND). For a frequency range of 100 kHz up to 10 MHz, the lock detector capacitor should vary between 10 pF and 1000 pF respectively.

VCO part

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency off-set if required.
The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at pin 10 (SF_{OUT}). If SF_{OUT} is used, a load resistor (R_{SF}) should be

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SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_{max}	maximum clock frequency	C_L = 15 pF V_{CC} = 5 V	15	15	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4046-1D; PC74HC/HCT4046-1D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4046-1P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4046-1T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	lock detector output (active HIGH)
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	SF_{OUT}	source-follower output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	$SIGN_{IN}$	signal input
15	C_{LD}	lock detector capacitor input
16	V_{CC}	positive supply voltage

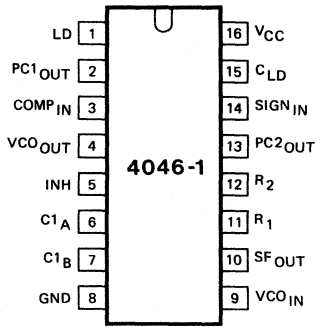


Fig. 1 Pin configuration.

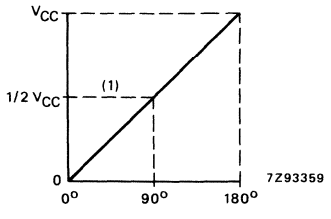
GENERAL DESCRIPTION (Cont'd)

connected from SF_{OUT} to GND; if unused, SF_{OUT} should be left open. The VCO output (VCO_{OUT}) can either be connected directly to the comparator input ($COMP_{IN}$) or via a frequency divider.
A LOW level at the inhibit input (INH) enables the VCO and source-follower, while a HIGH level turns off both to minimize stand-by power consumption.

Phase comparators

The phase-comparator signal input ($SIGN_{IN}$) can be direct-coupled, provided the signal swing is between the standard HC/HCT family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at $SIGN_{IN}$ in case of smaller swings.
Phase comparator 1 (PC1) is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50% duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to $1/2V_{CC}$ when there is no signal or noise at $SIGN_{IN}$. The average voltage to the VCO input (VCO_{IN}) is supplied by the low-pass filter connected to the output of PC1 ($PC1_{OUT}$). This also causes the VCO to oscillate at the centre frequency (f_o).
The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. PC1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal.



(1) Average output voltage.

Fig. 2 Signal-to-comparator inputs phase difference for PC1;
$PC1_{OUT} = (V_{CC}/\pi)(\phi_{IN} - \phi_{OUT})$.

A typical behaviour of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO centre frequency.
Another typical behaviour is, that the phase angle between the signal and comparator input varies between 0° and 180° and is 90° at the centre frequency. Figure 2 shows the typical phase-to-output response characteristics.

Figure 3 shows the typical waveforms for PLL employing PC1 in locked condition of f_o.

Phase comparator 2 (PC2) is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers having a common output mode. When the p-type or n-type drivers are "ON", they pull the output up to V_{CC} or down to GND respectively. This type of phase comparator only acts on the positive-going edges of the signals at $SIGN_{IN}$ and $COMP_{IN}$. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained "ON" most of the time, and both the n and p-type drivers are "OFF" (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained "ON" most of the time, and both the n and p-type drivers are "OFF" the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained "ON" for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained "ON" for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to this PC2 is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain "OFF" and thus the phase comparator output

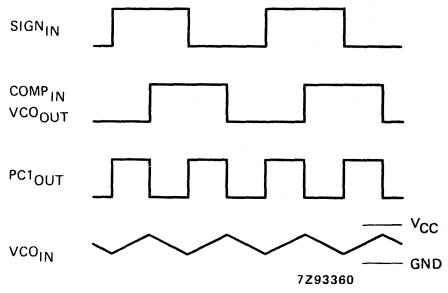


Fig. 3 Typical waveforms for PLL employing PC1 in locked condition of f_o.

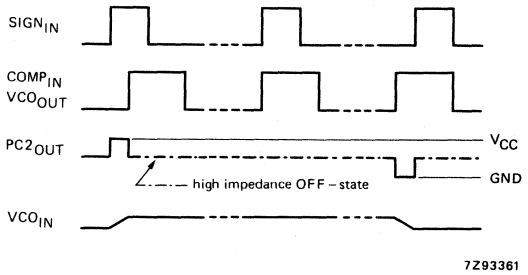


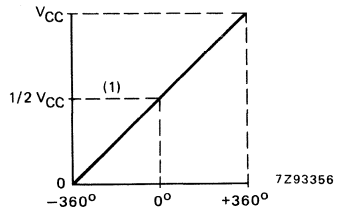
Fig. 4 Typical waveforms for a PLL employing PC2 in locked condition.

GENERAL DESCRIPTION (Cont'd)

($PC2_{OUT}$) becomes an open circuit and keeps the voltage at C2 constant. Thus, for PC2 no phase difference exists between $SIGN_{IN}$ and $COMP_{IN}$ over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at $SIGN_{IN}$, the VCO is adjusted to its lowest frequency for PC2. Figure 4 shows typical waveforms for a PLL employing this type of phase comparator in locked condition.

Figure 5 shows the typical phase-to-output response characteristics.

DEVELOPMENT DATA



(1) Average output voltage.

Fig. 5 Signal-to-comparator inputs phase difference for PC2;
$PC2_{OUT} = (V_{CC}/4\pi)(\phi_{IN} - \phi_{OUT})$.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

HEX INVERTING HIGH-TO-LOW LEVEL SHIFTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC4049 are high-speed Si-gate CMOS devices and are pin compatible with the "4049" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC4049 provide six inverting buffers. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to the standard TTL levels or as low as 2 V.

APPLICATIONS

- **Converting 15 V logic ("4000B" series) down to 2 V logic**

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	7	ns
C_I	input capacitance		3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC4049P: 16-lead DIL; plastic (SOT-38Z).
PC54HC4049D; PC74HC4049D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC4049T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{CC}	positive supply voltage
2, 4, 6, 10, 12, 15	1Y to 6Y	data outputs (active LOW)
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected

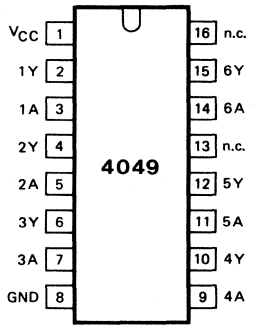


Fig. 1 Pin configuration.

HEX HIGH-TO-LOW LEVEL SHIFTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC4050 are high-speed Si-gate CMOS devices and are pin compatible with the "4050" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC4050 provide six non-inverting buffers. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to the standard TTL levels or as low as 2 V.

APPLICATIONS

- **Converting 15 V logic ("4000B" series) down to 2 V logic**

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	L
H	H

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	7	ns
C_I	input capacitance		3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC4050D; PC74HC4050P: 16-lead DIL; plastic (SOT-38Z).
PC74HC4050D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC4050T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{CC}	positive supply voltage
2, 4, 6, 10, 12, 15	1Y to 6Y	data outputs (active HIGH)
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected

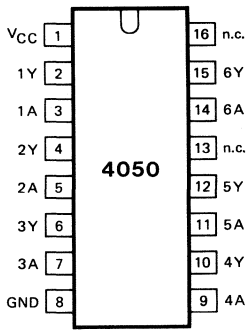


Fig. 1 Pin configuration.

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Low "ON" resistance:
  90 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
- Voltage level translation:
  2.0 to 6.0 V vice versa

GENERAL DESCRIPTION

The 54/74HC/HCT4051 are high-speed Si-gate CMOS devices and are pin compatible with the "4051" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4051 are 8-channel analog multiplexers/demultiplexers with three address inputs (S_0 to S_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The "4051" contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S_0 to S_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 6.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	C_L = 15 pF; V_{CC} = 5 V	4	4	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	22	24	pF
C_S	max. switch capacitance input common		 5 25	 5 25	 pF pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4051P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4051D; PC74HC/HCT4051D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4051T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	Z	common input/output
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S_0 to S_2	address inputs
13, 14, 15, 12, 1, 5, 2, 4	Y_0 to Y_7	independent inputs/outputs
16	V_{CC}	positive supply voltage

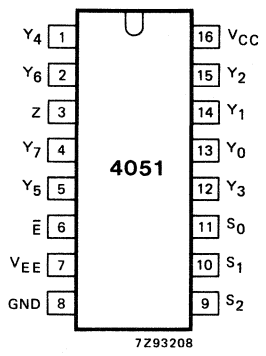


Fig. 1 Pin configuration.

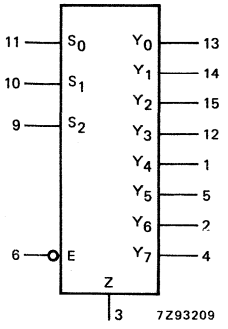


Fig. 2 Logic symbol.

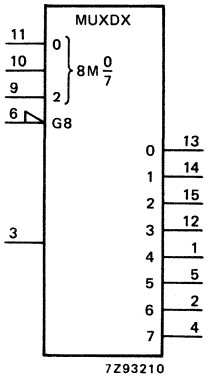


Fig. 3 IEC logic symbol.

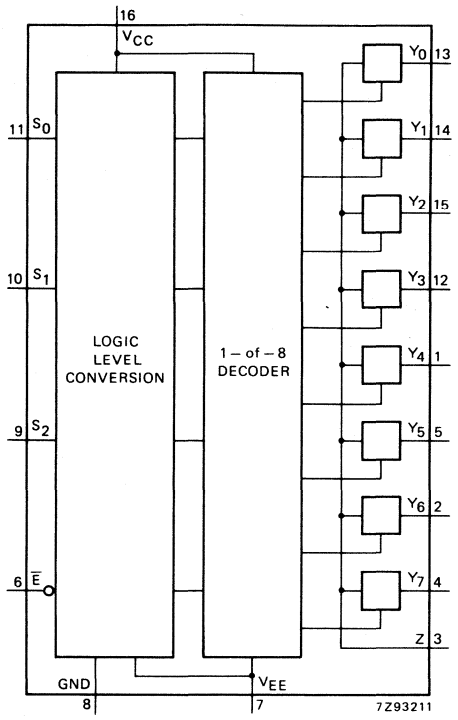


Fig. 4 Functional diagram.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

FUNCTION TABLE

INPUTS				channel ON
$\overline{E}$	S_2	S_1	S_0	
L	L	L	L	$Y_0 - Z$
L	L	L	H	$Y_1 - Z$
L	L	H	L	$Y_2 - Z$
L	L	H	H	$Y_3 - Z$
L	H	L	L	$Y_4 - Z$
L	H	L	H	$Y_5 - Z$
L	H	H	L	$Y_6 - Z$
L	H	H	H	$Y_7 - Z$
H	X	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

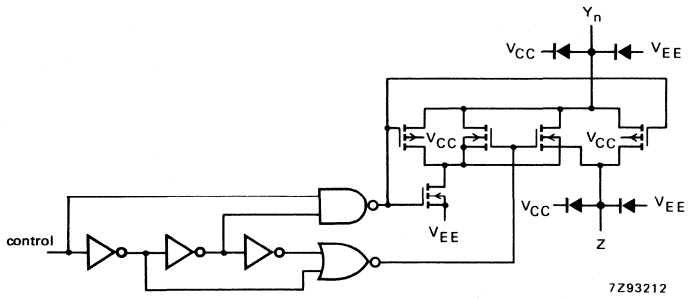


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60 °C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125 °C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n, in this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

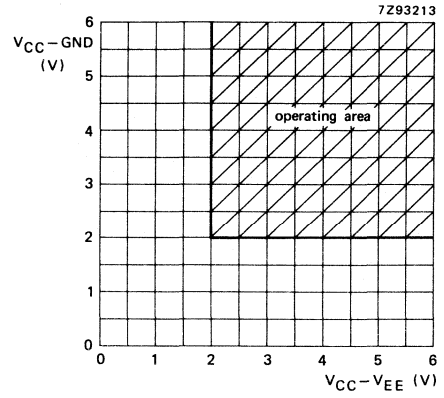


Fig. 6 Operating area as a function of the supply voltages for PC54/74HC4051.

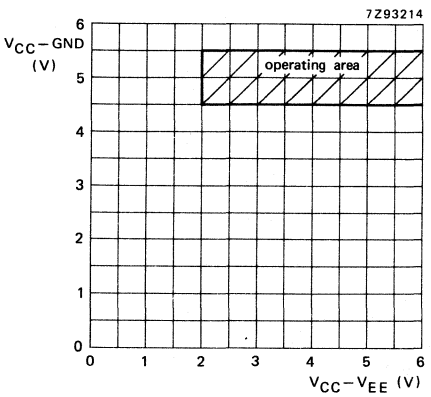


Fig. 7 Operating area as a function of the supply voltages for PC54/74HCT4051.

DC CHARACTERISTICS FOR 54/74HC/HCT

For 54/74HC: V_{CC} – GND or V_{CC} – V_{EE} = 2.0, 4.5 and 6.0 V
For 54/74HCT: V_{CC} – GND = 4.5 and 5.5 V; V_{CC} – V_{EE} = 2.0, 4.5 and 6.0 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC/HCT			74HC/HCT		54HC/HCT			V_{CC}–V_{EE} V	I_S μA	V_{is}
		+25			–40 to +85		–55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
R_{ON}	ON resistance		450 90 80	– 180 160		– 225 200		– 270 240	Ω Ω Ω	2.0 4.5 6.0	100 1000 1000	V_{CC} to V_{EE}
R_{ON}	ON resistance		150 70 60	– 140 120		– 175 150		– 210 180	Ω Ω Ω	2.0 4.5 6.0	100 1000 1000	V_{EE}
R_{ON}	ON resistance		150 80 70	– 160 140		– 200 175		– 240 210	Ω Ω Ω	2.0 4.5 6.0	100 1000 1000	V_{CC}
ΔR_{ON}	maximum ΔON resistance between any two channels		45 9 8						Ω Ω Ω	2.0 4.5 6.0		V_{CC} to V_{EE}
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	6.0	$V_I = V_{IH}$ or V_{IL} $\|V_S\| = V_{CC} - V_{EE}$	
$\pm I_S$	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	6.0	$V_I = V_{IH}$ or V_{IL} $\|V_S\| = V_{CC} - V_{EE}$	
$\pm I_S$	analog switch ON-state current			0.2		2.0		2.0	μA	6.0	$V_I = V_{IH}$ or V_{IL} $\|V_S\| = V_{CC} - V_{EE}$	

Note to DC characteristics

At supply voltage (V_{CC} – V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V); V_{EE} = GND

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V); V_{EE} = GND

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
S_n	0.50
$\overline{E}$	0.50

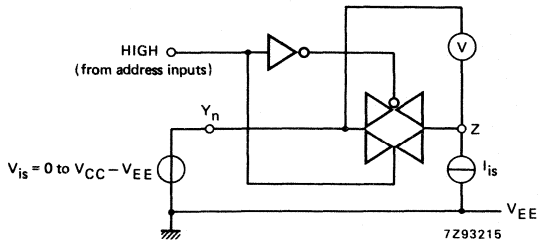


Fig. 8 Test circuit for measuring R_{ON}.

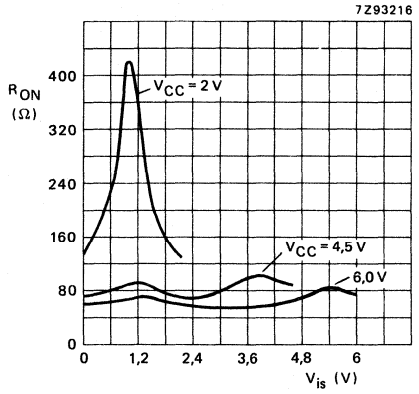


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

AC CHARACTERISTICS FOR 54/74HC

V_{EE} = GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC				
		+25			−40 to +85		−55 to +125			V_{CC} V	NOTES
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	note 1
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	notes 2 and 3
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	notes 2 and 3

AC CHARACTERISTICS FOR 54/74HCT

V_{EE} = GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT				
		+25			−40 to +85		−55 to +125			V_{CC} V	NOTES
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}			12		15		18	ns	4.5	note 1
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}			60		75		90	ns	4.5	notes 2 and 3
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}			50		63		75	ns	4.5	notes 2 and 3

AC CHARACTERISTICS FOR 54/74HC/HCT

V_{EE} = GND = 0 V; $t_r = t_f$ = 6 ns; T_{amb} = 25 °C
For 54/74HC: V_{CC} = 2.0, 4.5 and 6.0 V
For 54/74HCT: V_{CC} = 4.5 V

SYMBOL	PARAMETER	min.	typ.	max.	UNIT	V_{CC} V	NOTES
	distortion, sine-wave response		– 0.1 0.07		% % %	2.0 4.5 6.0	note 4
	crosstalk between any two channels				MHz MHz MHz	2.0 4.5 6.0	note 5
	crosstalk between enable or address input to output				mV mV mV	2.0 4.5 6.0	note 6
	OFF-state feed-through				MHz MHz MHz	2.0 4.5 6.0	note 7
	ON-state frequency response		100		MHz MHz MHz	2.0 4.5 6.0	note 8
C_S	maximum switch capacitance input common		 5 25		 pF pF		

Notes to AC characteristics

V_{is} is the input voltage at an Y_n or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at an Y_n or Z terminal, whichever is assigned as an output.

1. C_L = 50 pF to V_{EE}; $\overline{E}$ = GND; $V_{is} = V_{CC}$ (square wave); $R_L = \infty$; see Fig. 11.
2. R_L = 1 kΩ; C_L = 50 pF to V_{EE}; $S_n = V_{CC}$ (square wave); $\overline{E}$ = GND;
   $V_{is} = V_{CC}$ and R_L to V_{EE} for t_{PZH} and t_{PHZ}; see Fig. 12;
   $V_{is} = V_{EE}$ and R_L to V_{CC} for t_{PZL} and t_{PLZ}; see Fig. 12.
3. R_L = 1 kΩ; C_L = 50 pF to V_{EE}; $\overline{E} = V_{CC}$ (square wave);
   $V_{is} = V_{CC}$ and R_L to V_{EE} for t_{PZH} and t_{PHZ}; see Fig. 12;
   $V_{is} = V_{EE}$ and R_L to V_{CC} for t_{PZL} and t_{PLZ}; see Fig. 12.
4. R_L = 10 kΩ; C_L = 50 pF; channel ON; $V_{is} = V_{CC(p\text{-}p)}$ (sine-wave, symmetrical about V_{CC});
   f_{is} = 1 kHz; see Fig. 13.
5. R_L = 1 kΩ; $V_{is} = V_{CC(p\text{-}p)}$ (sine-wave, symmetrical about V_{CC});
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 10.
6. R_L = 10 kΩ; C_L = 50 pF to V_{EE}; $\overline{E}$ = GND; $S_n = V_{CC}$ (square wave); crosstalk is $|V_{os}|$ (peak value);
   see Fig. 13.
7. R_L = 10 kΩ; C_L = 50 pF; channel OFF; $V_{is} = V_{CC(p\text{-}p)}$ (sine-wave, symmetrical about V_{CC});
   f_{is} = 1 kHz; $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 13.
8. R_L = 1 kΩ; C_L = 5 pF; $V_{is} = V_{CC(p\text{-}p)}$ (sine-wave, symmetrical about V_{CC});
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 13.

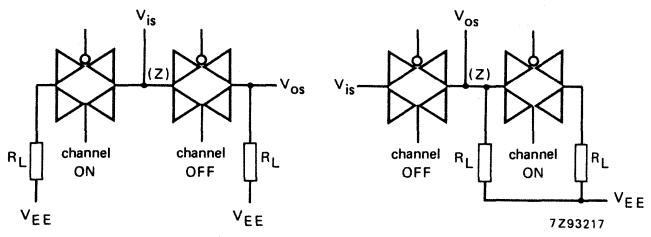


Fig. 10 Test circuit for measuring crosstalk between any two channels.

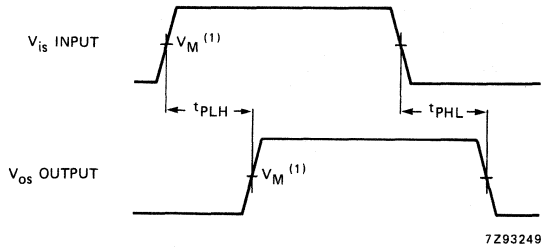


Fig. 11 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

AC WAVEFORMS

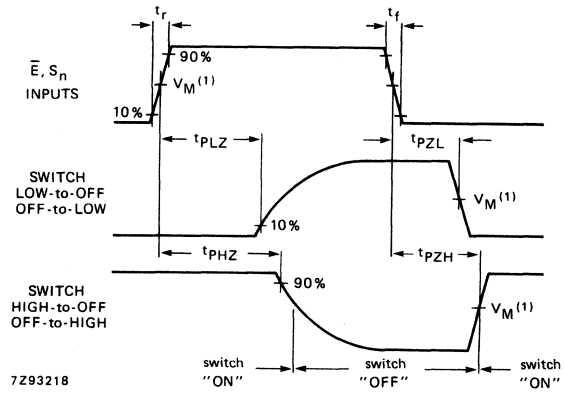
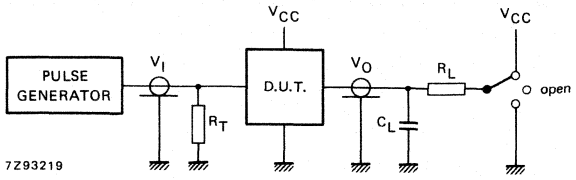


Fig. 12 Waveforms showing the turn-ON and turn—OFF times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	V_{EE}
t_{PZL}	V_{CC}
t_{PHZ}	V_{EE}
t_{PLZ}	V_{CC}
others	V_{EE}

Fig. 13 Test circuit for measuring AC performance.

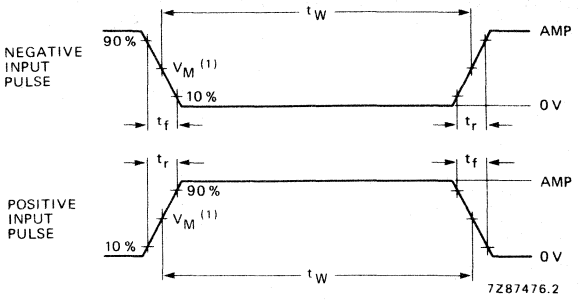


Fig. 14 Input pulse definitions.

Definitions for Figs 13 and 14:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- **Low "ON" resistance:**
  90 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
- **Voltage level translation:**
  2.0 to 6.0 V vice versa

GENERAL DESCRIPTION

The 54/74HC/HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the "4052" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4052 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ). The common channel select logics include two select inputs (S_0 and S_1) and an active LOW enable input ($\overline{E}$).

Both multiplexers/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent input/output (nY_0 to nY_3) and the other side connected to a common input/output (nZ).

With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by S_0 and S_1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 and S_1.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 and S_1, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 6.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 to nY_3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	propagation delay turn-on time	R_L = 1 kΩ, C_L = 50 pF, V_{CC} = 5 V	20	22	ns
t_{PLZ}/ t_{PHZ}	propagation delay turn-off time		18	20	ns
C_I	input capacitance		3.5	3.5	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4052D; PC74HC/HCT4052P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4052D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4052T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4	$2Y_0$ to $2Y_3$	independent inputs/outputs
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
10, 9	S_0, S_1	address inputs
12, 14, 15, 11	$1Y_0$ to $1Y_3$	independent inputs/outputs
13, 3	1Z, 2Z	common inputs/outputs
16	V_{CC}	positive supply voltage

APPLICATIONS

- **Analog multiplexing and demultiplexing**
- **Digital multiplexing and demultiplexing**
- **Signal gating**

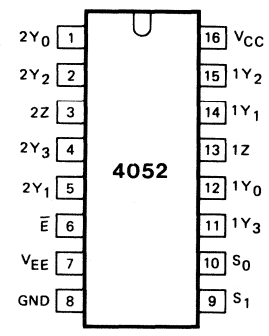


Fig. 1 Pin configuration.

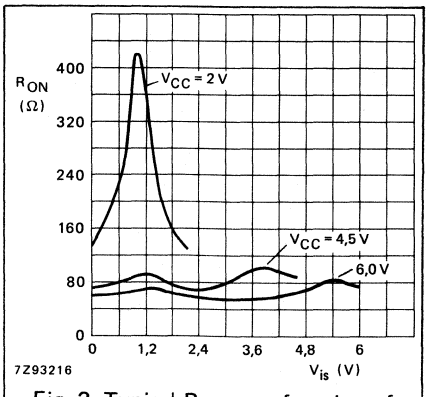


Fig. 2 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

FUNCTION TABLE

INPUTS			CHANNEL ON
$\overline{E}$	S_1	S_0	
L	L	L	$nY_0 - nZ$
L	L	H	$nY_1 - nZ$
L	H	L	$nY_2 - nZ$
L	H	H	$nY_3 - nZ$
H	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

TRIPPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- **Low "ON" resistance:**
  90 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
- **Voltage level translation:**
  2.0 to 6.0 V vice versa

GENERAL DESCRIPTION

The 54/74HC/HCT4053 are high-speed Si-gate CMOS devices and are pin compatible with the "4053" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4053 are tripple 2-channel analog multiplexers/demultiplexers with a common enable input ($\overline{E}$). Each multiplexer has two independent inputs/outputs (nY_0 and nY_1), a common input/output (nZ) and select inputs (S_0 to S_2).

Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an independent input/output (nY_0 and nY_1) and the other side connected to a common input/output (nZ).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_0 to S_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 6.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 and nY_1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	propagation delay turn-on time	R_L = 1 kΩ C_L = 50 pF V_{CC} = 5 V	19	21	ns
t_{PLZ}/ t_{PHZ}	propagation delay turn-off time		17	19	ns
C_I	input capacitance		3.5	3.5	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4053D; PC74HC/HCT4053P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4053D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4053T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1	$2Y_0$, $2Y_1$	independent inputs/outputs
5, 3	$3Y_0$, $3Y_1$	independent inputs/outputs
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S_0 to S_2	address inputs
12, 13	$1Y_0$, $1Y_1$	independent inputs/outputs
14, 15, 4	1Z to 3Z	common inputs/outputs
16	V_{CC}	positive supply voltage

APPLICATIONS

- **Analog multiplexing and demultiplexing**
- **Digital multiplexing and demultiplexing**
- **Signal gating**

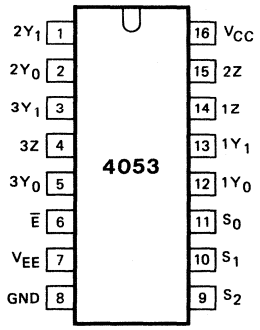


Fig. 1 Pin configuration.

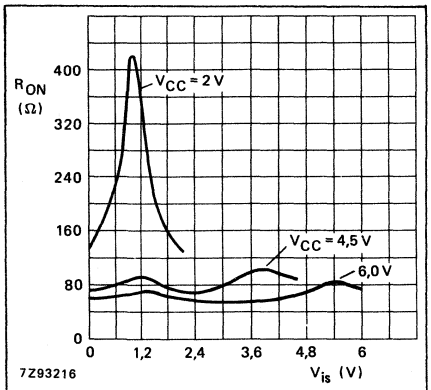


Fig. 2 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

FUNCTION TABLE

INPUTS		CHANNEL ON
$\overline{E}$	S_n	
L	L	$nY_0 - nZ$
L	H	$nY_1 - nZ$
H	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PROGRAMMABLE DIVIDE-BY-N COUNTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4059 are high-speed Si-gate CMOS devices and are pin compatible with the "4059" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4059 are divide-by-n counters which can be programmed to divide an input frequency by any number (n) from 3 to 15 999. The output signal is a one clock-cycle wide pulse and occurs at a rate equal to the input frequency divided by n. The down counter is preset by means of 16 jam inputs (J_1 to J_{16}). The three mode selection inputs (S_1 to S_3) determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the function table. Every time the first (fastest) counting section goes through one cycle, it reduces by 1, the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section (which consists of flip-flops that are not needed for operating the first counting section).

For example, in divide-by-2 mode, only one flip-flop is needed in the first counting section. Therefore the last (5th) counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands.

This counting mode is selected when S_1, S_2 and S_3 are set HIGH. In this case input J_1 is used to preset the first counting section and J_2 to J_4 are used to preset the last (5th) counting section.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4059P: 24-lead DIL; plastic (SOT-101A).
PC54HC/HCT4059D; PC74HC/HCT4059D: 24-lead DIL; ceramic (cerdip) (SOT-94).
PC74HC/HCT4059T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	LE	latch enable (active HIGH)
3, 4, 5, 6, 22, 21, 20, 19, 18, 17, 16, 15, 10, 9, 8, 7	J_1 to J_{16}	programmable jam inputs (BCD)
12	GND	ground (0 V)
14, 13, 11	S_1 to S_3	mode select inputs
23	Q	divide-by-n output
24	V_{CC}	positive supply voltage

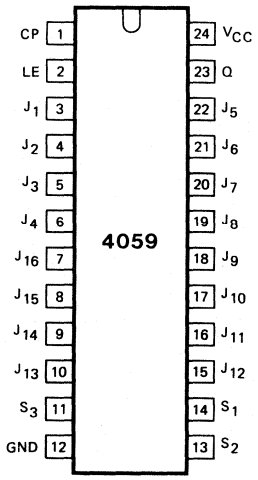


Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

If divide-by 10 mode is desired for the first section, S_1 is set HIGH, S_2 HIGH and S_3 LOW. The jam inputs J_1 to J_4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (divide-by-10) counters, presettable by means of the jam inputs J_5 to J_{16}.

When clock pulses are applied to the clock input (CP) after a number "n" has been preset into the counter, the counter counts down until the DETECTION circuit detects the zero state. At this time the PRESET ENABLE circuit is enabled to preset again the number "n" into the counter and to produce an output pulse.

The preset of the counter to a desired divide-by-n is achieved as follows:

n = (MODE*) (1000 x decade 5 preset +
+ 100 x decade 4 preset +
+ 10 x decade 3 preset +
+ 1 x decade 2 preset) +
+ decade 1 preset

* MODE = first counting section divider (10, 8, 5, 4 or 2).

To calculate preset values for any "n" count, divide the "n" count by the selected mode. The resultant is the corresponding preset value of the 5th to the 2nd decade with the remainder being equal to the 1ste decade value; preset value = n/mode.

If n = 8479, and the selected mode = 5, the preset value = 8479/5 = 1695 with a remainder of 4, thus the jam inputs must be set as shown in Table 1.

The mode select inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25 and 50 parts. These inputs set the maximum value of "n" at 9999 (when the first counting section divides by 5 or 10) or at 15 999 (when the first counting section divides by 8, 4 or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9. In this case the first cycle of a counter consists of 15 count pulses, the next cycles consisting of 10 counting pulses. Thus the place value of the three decades are still 1, 10 and 100. For example, in the divide-by-8 mode, the number from which the intermediate counting section begins to count-down can be preset to:

3rd decade: 1500
2nd decade: 150
1st decade: 15
1665

The last counting section can be preset to a maximum of 1, with a place value of 1000. The total of these numbers (2665) times 8 equals 21 320. The first counting section can be preset to a maximum of 7. Therefore, 21 327 is the maximum possible count in the divide-by-8 mode. The highest count of the various modes is shown in the function table, in the column entitled "extended counter range". Control inputs S_2 and S_3 can be used to initiate and lock the counter in the "master preset" mode. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that mode as long as S_2 and S_3 both remain LOW. The counter begins to run down from the preset state when a counting mode other than the "master preset" mode is selected. Whenever the "master preset" mode is used, control signals $S_2 = S_3$ = LOW must be applied for at least 3 full clock pulses. After the master preset mode inputs have been changed to one of the counting modes, the next positive-going clock transition changes an internal flip-flop so that the count-down can begin at the second positive-going clock transition. Thus, after a "master preset" mode, there is always one extra count before the output goes HIGH. Figure 2 illustrates the operation of the counter in the divide-by-8 mode starting from the preset state 3.

If the "master preset" mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the "master preset" mode is not used the counter is preset in accordance with the jam inputs when the output pulse appears. A HIGH level at the latch enable input (LE) will cause the counter output to remain in the HIGH state until the LE input returns to LOW. If the LE input is LOW, the output pulse will remain HIGH for only one cycle of the clock input signal.

When S_1 = LOW, S_2 = HIGH, S_3 = LOW and LE = LOW, the counter operates in the "preset inhibit" mode, with which the dividend of the counter is fixed to 10 000, independent of the state of the jam inputs.

When in the same state of mode select inputs LE = HIGH, the counter operates in the normal divide-by-10 mode, however, without the latch operation at the output.

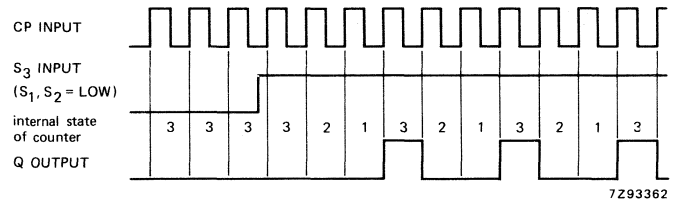


Fig. 2 Total count of 3.

Table 1

4			1	5				9				6			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L

FUNCTION TABLE

LATCH ENABLE INPUT	MODE SELECT INPUTS			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
LE	S_1	S_2	S_3	MODE DIVIDES BY	MAX. PRESET STATE	JAM INPUTS USED	MODE DIVIDES BY	MAX. PRESET STATE	JAM INPUTS USED	DESIGN MAX.	EXTENDED MAX.
X	H	H	H	2	1	J_1	8	7	$J_2J_3J_4$	15 999	17 331
X	L	H	H	4	3	J_1J_2	4	3	J_3J_4	15 999	18 663
X	H	L	H	5	4	$J_1J_2J_3$	2	1	J_4	9 999	13 329
X	L	L	H	8	7	$J_1J_2J_3$	2	1	J_4	15 999	21 327
X	H	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659
H	L	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659
L	L	H	L	preset inhibited			preset inhibited			fixed 10 000	–
X	X	L	L	master preset			master preset			–	–

H = HIGH voltage level
L = LOW voltage level
X = don't care

14-STAGE BINARY RIPPLE COUNTER WITH OSCILLATOR

FEATURES

- All active components on chip
- RC or crystal oscillator configuration
- Output capability: standard (except for R_{TC} and C_{TC})

GENERAL DESCRIPTION

The 54/74HC/HCT4060 are high-speed Si-gate CMOS devices and are pin compatible with "4060" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (Q_3 to Q_9 and Q_{11} to Q_{13}) and an overriding asynchronous master reset (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS.

In this case keep the other oscillator pins (R_{TC} and C_{TC}) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q_3 to Q_9 and Q_{11} to Q_{13} = LOW), independent of other input conditions.

In the HCT version, the MR input is TTL compatible, but the RS input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to V_{CC}.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay RS to Q_3	C_L = 15 pF; V_{CC} = 5 V	28	28	ns
	Q_n to Q_{n+1}		6	6	ns
t_{PHL}	MR to Q_n		17	18	ns
f_{max}	maximum clock frequency		60	60	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1, 2 and 3	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V
3. For formula on dynamic power dissipation see next page.

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4060P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4060D; PC74HC/HCT4060D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4060T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q_{11} to Q_{13}	counter outputs
7, 5, 4, 6, 14, 13, 15	Q_3 to Q_9	counter outputs
8	GND	ground (0 V)
9	C_{TC}	external capacitor connection
10	R_{TC}	external resistor connection
11	RS	clock input/oscillator pin
12	MR	master reset
16	V_{CC}	positive supply voltage

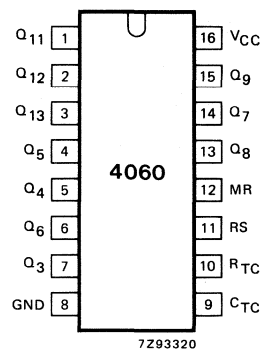


Fig. 1 Pin configuration.

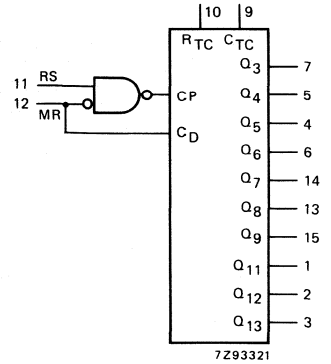


Fig. 2 Logic symbol.

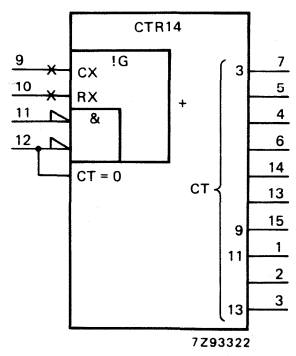


Fig. 3 IEC logic symbol.

DYNAMIC POWER DISSIPATION FOR 54/74HC

PARAMETER	V_{CC} V	TYPICAL FORMULA FOR P_D (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P_D)	2.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 60 \times V_{CC}$
	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$
	6.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 3\,800 \times V_{CC}$

GND = 0 V; T_{amb} = 25 °C

DYNAMIC POWER DISSIPATION FOR 54/74HCT

PARAMETER	V_{CC} V	TYPICAL FORMULA FOR P_D (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P_D)	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$

GND = 0 V; T_{amb} = 25 °C

Notes

1. Where: f_o = output frequency in MHz
   f_{osc} = oscillator frequency in MHz
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   C_t = timing capacitance in pF
   V_{CC} = supply voltage in V

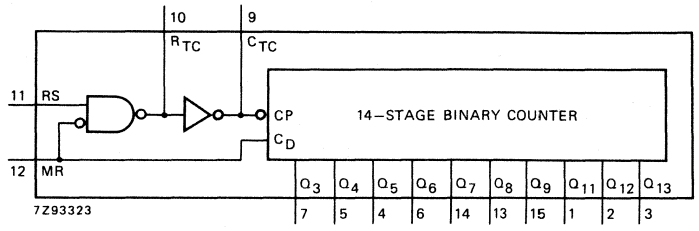


Fig. 4 Functional diagram.

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

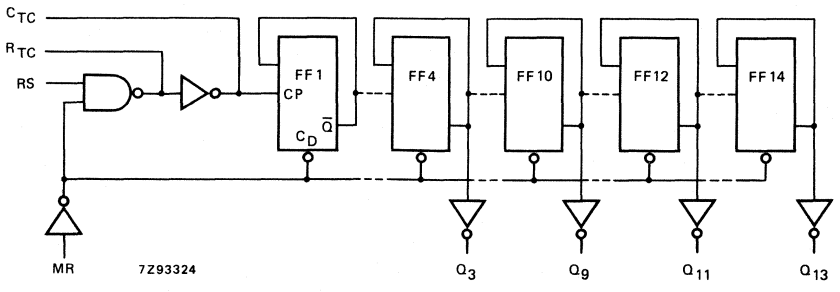


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage MR input	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage MR input		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{IH}	HIGH level input voltage RS input	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage RS input			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage R_{TC} output	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=GND and MR=GND	$-I_O$ = 2.6 mA $-I_O$ = 3.3 mA
		3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 0.65 mA $-I_O$ = 0.85 mA
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	RS=GND and MR=GND	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage C_{TC} output	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=V_{IH} and MR=V_{IL}	$-I_O$ = 3.2 mA $-I_O$ = 4.2 mA
V_{OH}	HIGH level output voltage except R_{TC} output	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage except R_{TC} and C_{TC} outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage R_{TC} output			0.26 0.26		0.33 0.33		0.4 0.4		4.5 6.0	RS=V_{CC} and MR=GND	I_O = 2.6 mA I_O = 3.3 mA
			0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	RS=V_{CC} and MR=GND	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage C_{TC} output			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	RS=V_{IL} and MR=V_{IH}	I_O = 3.2 mA I_O = 4.2 mA

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DC CHARACTERISTICS FOR 54/74HC (continued)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{OL}	LOW level output voltage except R_{TC} output		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage except R_{TC} and C_{TC} outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		note 2
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		note 2
V_{OH}	HIGH level output voltage R_{TC} output	3.98			3.84		3.7		V	4.5	RS=GND and MR=GND	$-I_O$ = 2.6 mA
		3.98			3.84		3.7		V	4.5	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 0.65 mA
		4.4	4.5		4.4		4.4		V	4.5	RS=GND and MR=GND	$-I_O$ = 20 μA
		4.4	4.5		4.4		4.4		V	4.5	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage C_{TC} output	3.98			3.84		3.7		V	4.5	RS=V_{IH} and MR=V_{IL}	$-I_O$ = 3.2 mA
V_{OH}	HIGH level output voltage except R_{TC} output	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage except R_{TC} and C_{TC} outputs	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage R_{TC} output			0.26		0.33		0.4	V	4.5	RS=V_{CC} and MR=GND	I_O = 2.6 mA
			0	0.1		0.1		0.1	V	4.5	RS=V_{CC} and MR=GND	I_O = 20 μA
V_{OL}	LOW level output voltage C_{TC} output			0.26		0.33		0.4	V	4.5	RS=V_{IL} and MR=V_{IH}	I_O = 3.2 mA
V_{OL}	LOW level output voltage except R_{TC} output		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage except R_{TC} and C_{TC} outputs			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0

(continued on next page)

DC CHARACTERISTICS FOR 54/74HCT (continued)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT					
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.		V_{CC} V	V_I	OTHER
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.
2. Only input MR (pin 12) has TTL input switching levels for the HCT version.

input	unit load coefficient
MR	0.40

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC				
		+25			−40 to +85		−55 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay RS to Q_3			330 66 56		415 83 70		495 99 84	ns	2.0 4.5 6.0	Fig. 11
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}			80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 13
t_{PHL}	propagation delay MR to Q_n			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 12
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 11
t_W	clock pulse width RS; HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 11
t_W	master reset pulse width MR; HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 12
t_{rem}	removal time MR to RS	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 12
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 11

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay RS to Q_3			66		83		99	ns	4.5	Fig. 11
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}			16		20		24	ns	4.5	Fig. 13
t_{PHL}	propagation delay MR to Q_n			44		55		66	ns	4.5	Fig. 12
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 11
t_W	clock pulse width RS; HIGH or LOW	16			20		24		ns	4.5	Fig. 11
t_W	master reset pulse width MR; HIGH	16			20		24		ns	4.5	Fig. 12
t_{rem}	removal time MR to RS	26			33		39		ns	4.5	Fig. 12
f_{max}	maximum clock pulse frequency	30			24		20		MHz	4.5	Fig. 11

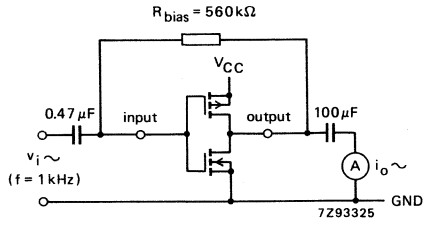


Fig. 6 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 7); MR = LOW.

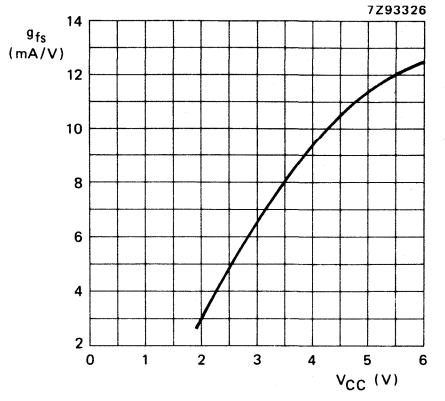


Fig. 7 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

DEVELOPMENT DATA

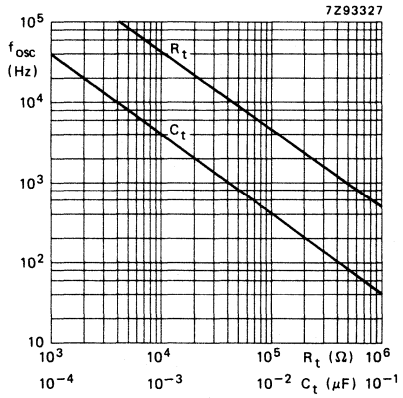


Fig. 8 RC oscillator frequency as a function of R_t and C_t at V_{CC} = 2.0 to 6.0 V; T_{amb} = 25 °C.
C_t curve at R_t = 100 kΩ; R2 = 200 kΩ.
R_t curve at C_t = 1 nF; R2 = 2 x R_t.

RC OSCILLATOR

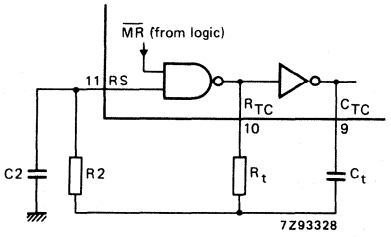


Fig. 9 Example of a RC oscillator.
Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$$

TIMING COMPONENT LIMITATIONS

The oscillator frequency is mainly determined by R_tC_t, provided R2 ≈ $2R_t$ and R2C2 ≪ R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the "ON" resistance in series with it, which typically is 280 Ω at V_{CC} = 2.0 V, 130 Ω at V_{CC} = 4.5 V and 100 Ω at V_{CC} = 6.0 V.
The recommended values for these components to maintain agreement with the typical oscillation formula are:

C_t > 50 pF, up to any practical value,

10 kΩ < R_t < 1 MΩ.

TYPICAL CRYSTAL OSCILLATOR

In Fig. 10, R2 is the power limiting resistor.
For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

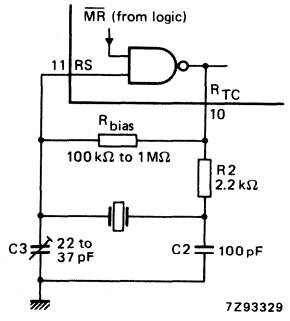


Fig. 10 External components connection for a crystal oscillator.

AC WAVEFORMS

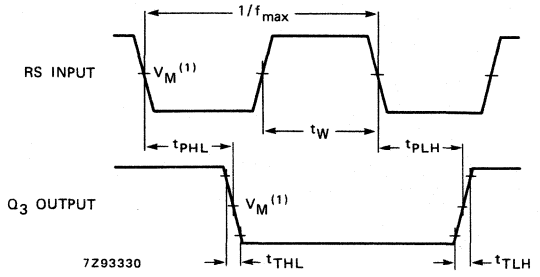


Fig. 11 Waveforms showing the clock (RS) to output (Q_3) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

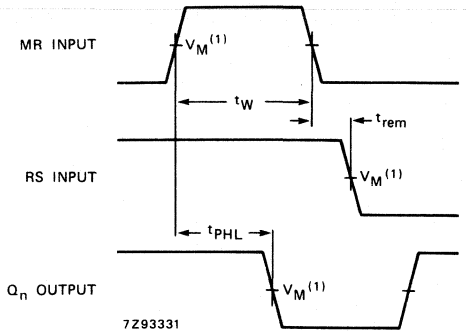


Fig. 12 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (RS) removal time.

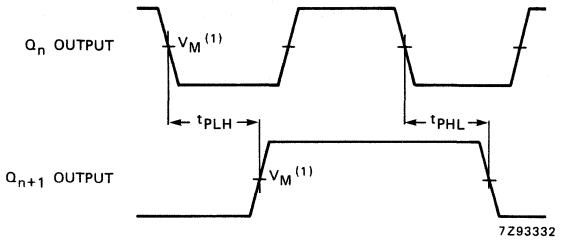


Fig. 13 Waveforms showing the output (Q_n) to Q_{n+1} propagation delays.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

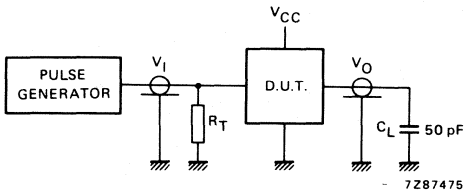


Fig. 14 Test circuit.

Definitions for Figs 14 and 15:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

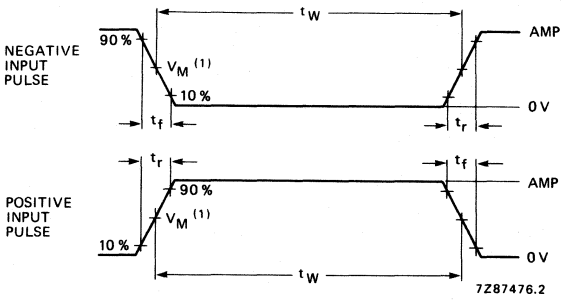


Fig. 15 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

QUAD BILATERAL SWITCH

FEATURES

- **Very low "ON" resistance:**
  45 Ω (typ.) at V_{CC} = 4.5 V
  35 Ω (typ.) at V_{CC} = 6.0 V

GENERAL DESCRIPTION

The 54/74HC/HCT4066 are high-speed Si-gate CMOS devices and are pin compatible with the "4066" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4066 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the belonging analog switch is turned off.

The "4066" is pin compatible with the "4016" but exhibits a much lower "ON" resistance. In addition, the "ON" resistance is relatively constant over the full input signal range.

FUNCTION TABLE

INPUT nE	SWITCH
L	off
H	on

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	propagation delay turn-on time	R_L = 1 kΩ C_L = 50 pF V_{CC} = 5 V	17	19	ns
t_{PLZ}/ t_{PHZ}	propagation delay turn-off time		15	17	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4066P: 14-lead DIL; plastic (SOT-27).
PC54HC/HCT4066D; PC74HC/HCT4066D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT4066T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1Y to 4Y	independent inputs/outputs
2, 3, 9, 10	1Z to 4Z	independent inputs/outputs
7	GND	ground (0 V)
13, 5, 6, 12	1E to 4E	enable inputs (active HIGH)
14	V_{CC}	positive supply voltage

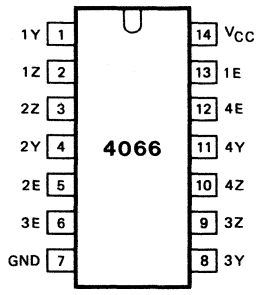


Fig. 1 Pin configuration.

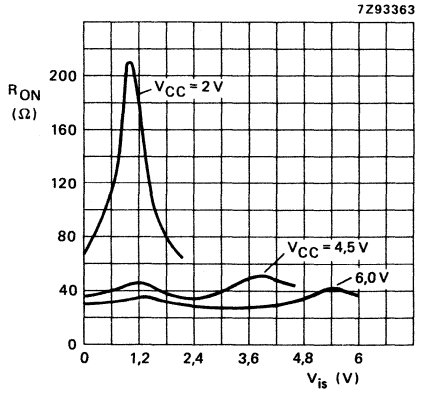


Fig. 2 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC}.

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- **Low "ON" resistance:**
  90 Ω (typ.) at V_{CC} = 4.5 V
  80 Ω (typ.) at V_{CC} = 6.0 V

GENERAL DESCRIPTION

The 54/74HC/HCT4067 are high-speed Si-gate CMOS devices and are pin compatible with the "4067" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4067 are 16-channel analog multiplexers/demultiplexers with four address inputs (S_0 to S_3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The "4067" contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the sixteen switches is selected (low impedance ON-state) by S_0 to S_3. All unselected switches are in the high impedance OFF-state. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_3.

The analog inputs/outputs (Y_0 to Y_{15}, and Z) can swing between V_{CC} as a positive limit and GND as a negative limit. V_{CC} to GND may not exceed 6.0 V.

APPLICATIONS

- **Analog multiplexing and demultiplexing**
- **Digital multiplexing and demultiplexing**
- **Signal gating**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	propagation delay turn-on time	R_L = 1 kΩ C_L = 50 pF V_{CC} = 5 V	27	29	ns
t_{PLZ}/ t_{PHZ}	propagation delay turn-off time		25	27	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4067D; PC74HC/HCT4067P: 24-lead DIL; plastic (SOT-101A).
PC74HC/HCT4067D: 24-lead DIL; ceramic (cerdip) (SOT-94).
PC74HC/HCT4067T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	Z	common input/output
9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	Y_0 to Y_{15}	independent inputs/outputs
10, 11, 14, 13	S_0 to S_3	address inputs
12	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
24	V_{CC}	positive supply voltage

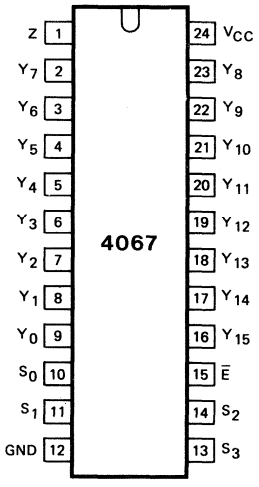


Fig. 1 Pin configuration.

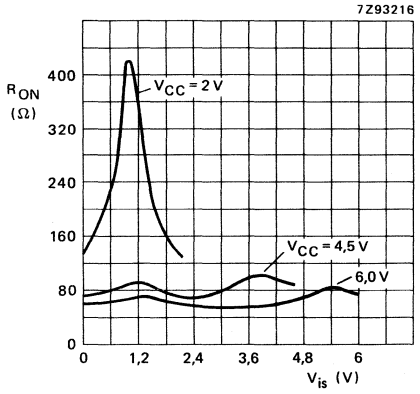


Fig. 2 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC}.

FUNCTION TABLE

INPUTS					CHANNEL ON
$\overline{E}$	S_3	S_2	S_1	S_0	
L	L	L	L	L	Y_0 – Z
L	L	L	L	H	Y_1 – Z
L	L	L	H	L	Y_2 – Z
L	L	L	H	H	Y_3 – Z
L	L	H	L	L	Y_4 – Z
L	L	H	L	H	Y_5 – Z
L	L	H	H	L	Y_6 – Z
L	L	H	H	H	Y_7 – Z
L	H	L	L	L	Y_8 – Z
L	H	L	L	H	Y_9 – Z
L	H	L	H	L	Y_{10} – Z
L	H	L	H	H	Y_{11} – Z
L	H	H	L	L	Y_{12} – Z
L	H	H	L	H	Y_{13} – Z
L	H	H	H	L	Y_{14} – Z
L	H	H	H	H	Y_{15} – Z
H	X	X	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

TRIPLE 3-INPUT OR GATE

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4075 are high-speed Si-gate CMOS devices and are pin compatible with the "4075" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4075 provide the 3-input OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 5 V	8	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	28	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4075D;
PC74HC/HCT4075P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT4075D: 14-lead DIL; ceramic (cerdip) (SOT-73).
PC74HC/HCT4075T: 14-lead mini-pack; plastic (SO-14; (SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 11	1A to 3A	data inputs
4, 2, 12	1B to 3B	data inputs
5, 8, 13	1C to 3C	data inputs
6, 9, 10	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

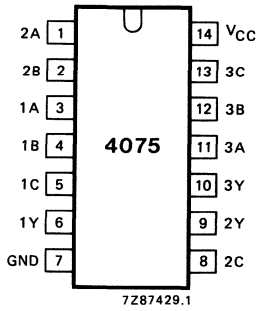


Fig. 1 Pin configuration.

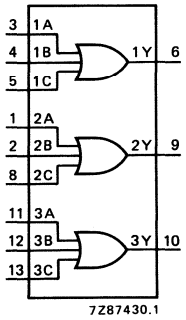


Fig. 2 Logic symbol.

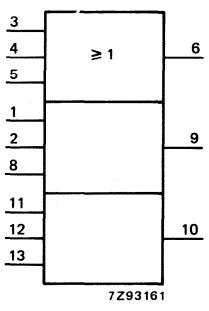


Fig. 3 IEC logic symbol.

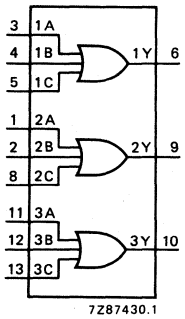


Fig. 4 Functional diagram.

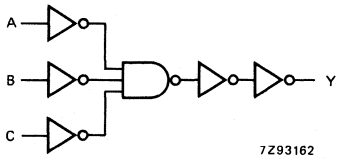


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB, nC	1.60

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY			24		30		36	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

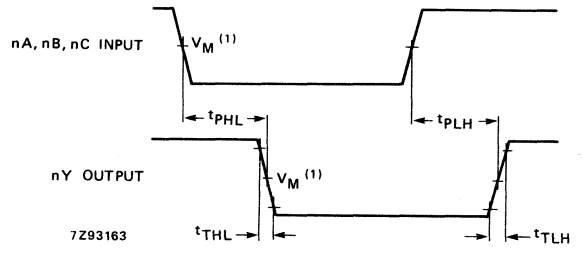


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

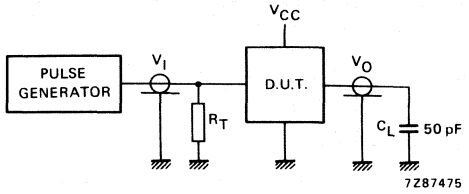


Fig. 7 Test circuit.

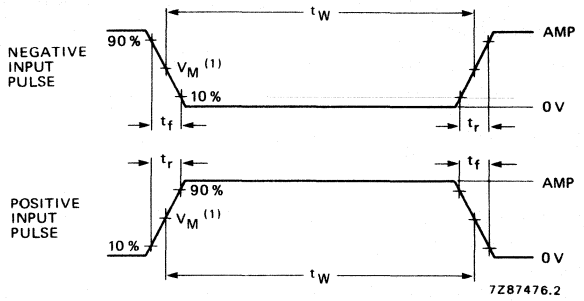


Fig. 8 Input pulse definitions.

Definitions for Figs 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

8-STAGE SHIFT-AND-STORE BUS REGISTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4094 are high-speed Si-gate CMOS devices and are pin compatible with the "4094" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP_0 to QP_7). The parallel outputs may be connected directly in common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.

Two serial outputs (QS_1 and QS_2) are available for cascading a number of "4094" devices. Data is available at QS_1 on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS_2 on the next negative-going clock edge and provides cascading "4094" devices when the clock rise time is slow.

APPLICATIONS

- **Serial-to-parallel data conversion**
- **Remote control holding register**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to QP_n, QS_n	C_L = 15 pF; V_{CC} = 5 V	10	12	ns
f_{max}	maximum clock frequency		60	54	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4094P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4094D; PC74HC/HCT4094D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4094T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	serial input
3	CP	clock input
4, 5, 6, 7, 14, 13, 12, 11	QP_0 to QP_7	parallel outputs
8	GND	ground (0 V)
9, 10	QS_1, QS_2	serial outputs
15	OE	output enable input
16	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP_0	QP_n	QS_1	QS_2
↑	L	X	X	Z	Z	Q'_6	NC
↓	L	X	X	Z	Z	NC	QP_7
↑	H	L	X	NC	NC	Q'_6	NC
↑	H	H	L	L	QP_{n-1}	Q'_6	NC
↑	H	H	H	H	QP_{n-1}	Q'_6	NC
↓	H	H	H	NC	NC	NC	QP_7

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state
NC = no change
↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Q'_6 = the information in the seventh register stage is transferred to the 8th register stage and QS_n output at the positive clock edge

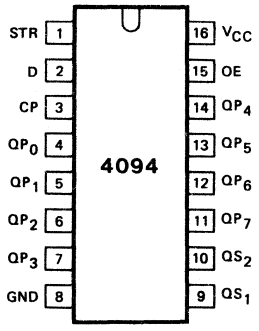


Fig. 1 Pin configuration.

QUAD BILATERAL SWITCHES

FEATURES

- **Low "ON" resistance:**
  160 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  120 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
- **Voltage level translation:**
  2.0 to 6.0 V vice versa

GENERAL DESCRIPTION

The 54/74HC/HCT4316 are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4316 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input ($\overline{E}$) is HIGH, all four analog switches are turned off.

V_{CC} and GND are the supply voltage pins for the digital control inputs ($\overline{E}$ and nS). The V_{CC} to GND ranges are 2.0 to 6.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

APPLICATIONS

- **Signal gating**
- **Modulation**
- **Demodulation**
- **Chopper**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	propagation delay turn-on time	R_L = 1 kΩ C_L = 50 pF V_{CC} = 5 V	19	21	ns
t_{PLZ}/ t_{PHZ}	propagation delay turn-off time		17	19	ns
C_I	input capacitance		3.5	3.5	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4316P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4316D; PC74HC/HCT4316D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4316T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Z to 4Z	independent inputs/outputs
2, 3, 11, 12	1Y to 4Y	independent inputs/outputs
7	$\overline{E}$	enable input (active LOW)
8	GND	ground (0 V)
9	V_{EE}	negative supply voltage
15, 5, 6, 14	1S to 4S	select inputs (active HIGH)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS		SWITCH
$\overline{E}$	nS	
L	L	off
L	H	on
H	X	off

H = HIGH voltage level
L = LOW voltage level
X = don't care

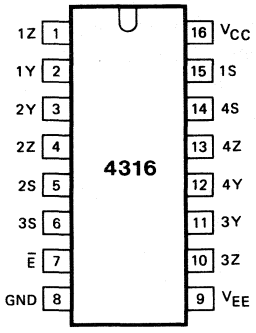


Fig. 1 Pin configuration.

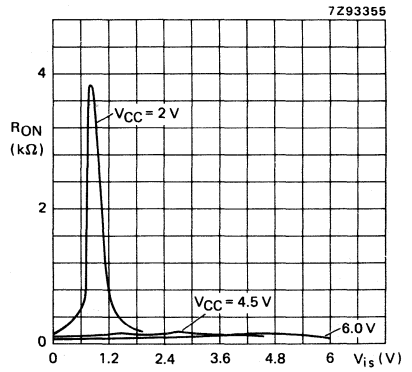


Fig. 2 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES

- **Low "ON" resistance:**
  90 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
- **Voltage level translation:**
  2.0 to 6.0 V vice versa
- **Address latches provided**

GENERAL DESCRIPTION

The 54/74HC/HCT4351 are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4351 are 8-channel analog multiplexers/demultiplexers with three address inputs (S_0 to S_2), two enable inputs ($\overline{E}_1$ and E_2), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The "4351" contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With $\overline{E}_1$ LOW and E_2 is HIGH, one of the eight switches is selected (low impedance ON-state) by S_0 to S_2. The data at the select inputs may be latched by using the active LOW latch enable input ($\overline{LE}$). When $\overline{LE}$ is HIGH, the latch is transparent. When either of the two enable inputs, $\overline{E}_1$ (active LOW) and E_2 (active HIGH), is inactive, all 8 analog switches are turned off.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, $\overline{LE}$, $\overline{E}_1$ and E_2). The V_{CC} to GND ranges are 2.0 to 6.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	propagation delay turn-on time	R_L = 1 kΩ C_L = 50 pF V_{CC} = 5 V	25	27	ns
t_{PLZ}/ t_{PHZ}	propagation delay turn-off time		23	25	ns
C_I	input capacitance		3.5	3.5	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4351D; PC74HC/HCT4351D: 18-lead DIL; ceramic (cerdip) (SOT-133).
PC74HC/HCT4351P: 18-lead DIL; plastic (SOT-102A).
PC74HC/HCT4351T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3 (3)	Z	common input/output
(5)	n.c.	not connected
6 (7)	$\overline{E}_1$	enable input (active LOW)
7 (8)	E_2	enable input (active HIGH)
8 (9)	V_{EE}	negative supply voltage
9 (10)	GND	ground (0 V)
10 (11)	$\overline{LE}$	latch enable input (active LOW)
13, 12, 11 (14, 13, 12)	S_0 to S_2	address inputs
15, 16, 17, 14, 1, 5, 2, 4 (17, 18, 19, 16, 1, 6, 2, 4)	Y_0 to Y_7	independent inputs/outputs
(15)	n.c.	not connected
18 (20)	V_{CC}	positive supply voltage

Note

The pin numbers between parenthesis are for the "4351" in SO-20 package.

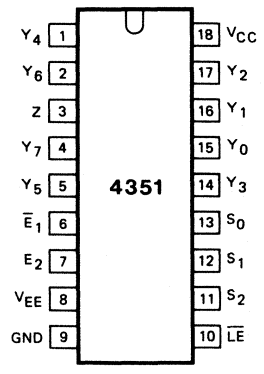


Fig. 1 Pin configuration (DIL package).

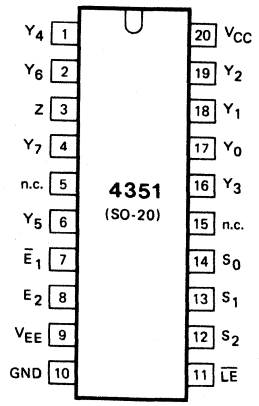


Fig. 2 Pin configuration (SO-20 package).

APPLICATIONS

- **Analog multiplexing and demultiplexing**
- **Digital multiplexing and demultiplexing**
- **Signal gating**

FUNCTION TABLE

INPUTS						CHANNEL ON
$\overline{E}_1$	E_2	$\overline{LE}$	S_2	S_1	S_0	
H	X	X	X	X	X	none
X	L	X	X	X	X	none
L	H	H	L	L	L	Y_0
L	H	H	L	L	H	Y_1
L	H	H	L	H	L	Y_2
L	H	H	L	H	H	Y_3
L	H	H	H	L	L	Y_4
L	H	H	H	L	H	Y_5
L	H	H	H	H	L	Y_6
L	H	H	H	H	H	Y_7
L	H	L	X	X	X	*
X	X	↓	X	X	X	**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↓ = HIGH-to-LOW $\overline{LE}$ transition

* Last selected channel "ON".
** Selected channels latched.

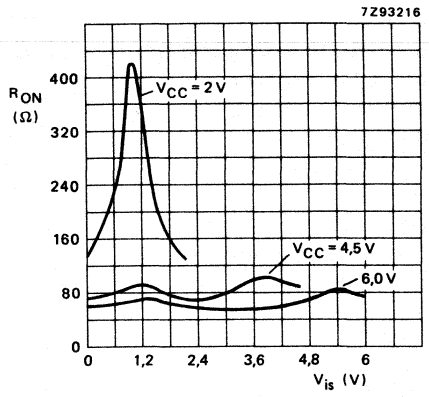


Fig. 3 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES

- **Low "ON" resistance:**
  90 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
- **Voltage level translation:**
  2.0 to 6.0 V vice versa
- **Address latches provided**

GENERAL DESCRIPTION

The 54/74HC/HCT4352 are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4352 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ). The common channel select logics include two select inputs (S_0 and S_1) and an active LOW enable input ($\overline{E}_1$) and an active HIGH enable input (E_2).
Both multiplexers/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent input/output (nY_0 to nY_3) and the other side connected to a common input/output (nZ).

With $\overline{E}_1$ LOW and E_2 HIGH, one of the four switches is selected (low impedance ON-state) by S_0 and S_1.
The data at the select inputs may be latched by using the active LOW latch enable input ($\overline{LE}$). When $\overline{LE}$ is HIGH, the latch is transparent. When either of the two enable inputs, $\overline{E}_1$ (active LOW) and E_2 (active HIGH), is inactive, all analog switches are turned off.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	propagation delay turn-on time	R_L = 1 kΩ C_L = 50 pF V_{CC} = 5 V	22	24	ns
t_{PLZ}/ t_{PHZ}	propagation delay turn-off time		20	22	ns
C_I	input capacitance		3.5	3.5	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4352P: 18-lead DIL; plastic (SOT-102A).
PC54HC/HCT4352D; PC74HC/HCT4352D: 18-lead DIL; ceramic (cerdip) (SOT-133).
PC74HC/HCT4352T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4 (1, 6, 2, 4)	$2Y_0$ to $2Y_3$	independent inputs/outputs
(5)	n.c.	not connected
6 (7)	$\overline{E}_1$	enable input (active LOW)
7 (8)	E_2	enable input (active HIGH)
8 (9)	V_{EE}	negative supply voltage
9 (10)	GND	ground (0 V)
10 (11)	$\overline{LE}$	latch enable input (active LOW)
12, 11 (13, 12)	S_0, S_1	address inputs
14, 16, 17, 13 (16, 18, 19, 14)	$1Y_0$ to $1Y_3$	independent inputs/outputs
15, 3 (17, 3)	1Z, 2Z	common inputs/outputs
(15)	n.c.	not connected
18 (20)	V_{CC}	positive supply voltage

Note

The pin numbers between parenthesis are for the "4352" in SO-20 package.

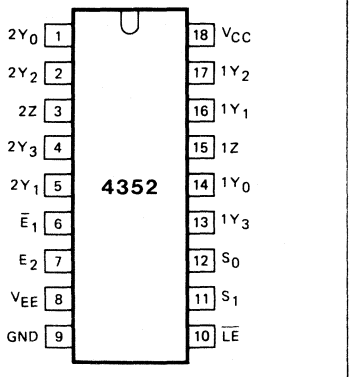


Fig. 1 Pin configuration (DIL package).

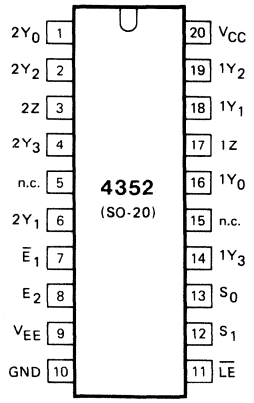


Fig. 2 Pin configuration (SO-20 package).

APPLICATIONS

- **Analog multiplexing and demultiplexing**
- **Digital multiplexing and demultiplexing**
- **Signal gating**

GENERAL DESCRIPTION (Cont'd)

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0, S_1, $\overline{LE}$, $\overline{E}_1$ and E_2). The V_{CC} to GND ranges are 2.0 to 6.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 to nY_3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

FUNCTION TABLE

INPUTS					CHANNEL ON
$\overline{E}_1$	E_2	$\overline{LE}$	S_1	S_0	
H	X	X	X	X	none
X	L	X	X	X	none
L	H	H	L	L	nY_0 – nZ
L	H	H	L	H	nY_1 – nZ
L	H	H	H	L	nY_2 – nZ
L	H	H	H	H	nY_3 – nZ
L	H	L	X	X	*
X	X	↓	X	X	**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↓ = HIGH-to-LOW $\overline{LE}$ transition

* Last selected channel "ON".
** Selected channels latched.

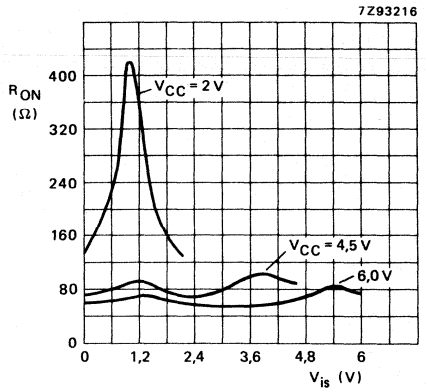


Fig. 3 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

TRIPPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES

- **Low "ON" resistance:**
  90 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
- **Voltage level translation:**
  2.0 to 6.0 V vice versa
- **Address latches provided**

GENERAL DESCRIPTION

The 54/74HC/HCT4353 are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4353 are tripple 2-channel analog multiplexers/demultiplexers with two common enable inputs ($\overline{E}_1$ and E_2). Each multiplexer has two independent inputs/outputs (nY_0 and nY_1), a common input/output (nZ) and select inputs (S_0 to S_2).

Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an independent input/output (nY_0 and nY_1) and the other side connected to a common input/output (nZ).

With $\overline{E}_1$ LOW and E_2 is HIGH, one of the two switches is selected (low impedance ON-state) by S_0 to S_2.
The data at the select inputs may be latched by using the active LOW latch enable input ($\overline{LE}$). When $\overline{LE}$ is HIGH, the latch is transparent. When either of the two enable inputs, $\overline{E}_1$ (active LOW) and E_2 (active HIGH), is inactive, all analog switches are turned off.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, $\overline{LE}$, $\overline{E}_1$ and E_2). The V_{CC} to GND ranges are 2.0 to 6.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 and nY_1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

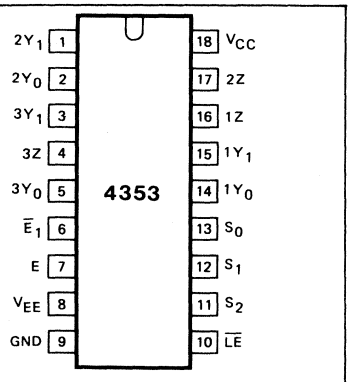


Fig. 1 Pin configuration (DIL package).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	propagation delay turn-on time	R_L = 1 kΩ C_L = 50 pF V_{CC} = 5 V	21	23	ns
t_{PLZ}/ t_{PHZ}	propagation delay turn-off time		19	21	ns
C_I	input capacitance		3.5	3.5	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4353P: 18-lead DIL; plastic (SOT-102A).
PC54HC/HCT4353D; PC74HC/HCT4353D: 18-lead DIL; ceramic (cerdip) (SOT-133).
PC74HC/HCT4353T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1 (2, 1)	$2Y_0$, $2Y_1$	independent inputs/outputs
4 (4)	3Z	common input/output
5, 3 (6, 3)	$3Y_0$, $3Y_1$	independent inputs/outputs
(5)	n.c.	not connected
6 (7)	$\overline{E}_1$	enable input (active LOW)
7 (8)	E_2	enable input (active HIGH)
8 (9)	V_{EE}	negative supply voltage
9 (10)	GND	ground (0 V)
10 (11)	$\overline{LE}$	latch enable input (active LOW)
13, 12, 11 (14, 13, 12)	S_0 to S_2	address inputs
14, 15 (16, 17)	$1Y_0$, $1Y_1$	independent inputs/outputs
16 (18)	1Z	common input/output
17 (19)	2Z	common input/output
18 (20)	V_{CC}	positive supply voltage

Note

The pin numbers between parenthesis are for the "4353" in SO-20 package.

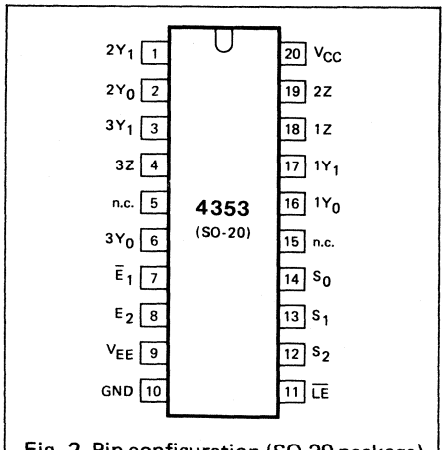


Fig. 2 Pin configuration (SO-20 package).

APPLICATIONS

- **Analog multiplexing and demultiplexing**
- **Digital multiplexing and demultiplexing**
- **Signal gating**

FUNCTION TABLE

INPUTS				CHANNEL ON
$\overline{E}_1$	E_2	$\overline{LE}$	S_n	
H	X	X	X	none
X	L	X	X	none
L	H	H	L	$nY_0 - nZ$
L	H	H	H	$nY_1 - nZ$
L	H	L	X	*
X	X	↓	X	**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↓ = HIGH-to-LOW $\overline{LE}$ transition

* Last selected channel "ON".
** Selected channels latched.

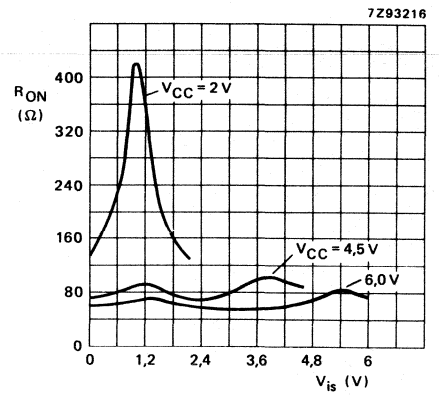


Fig. 3 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BCD UP/DOWN COUNTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4510 are high-speed Si-gate CMOS devices and are pin compatible with the "4510" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4510 are edge-triggered synchronous up/down BCD counters with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D_0 to D_3), four parallel outputs (Q_0 to Q_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW-to-HIGH transition of CP if $\overline{CE}$ is LOW. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when Q_0 and Q_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when Q_0 to Q_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (Q_0 to Q_3 = = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE} \,.\, \{ (UP/\overline{DN}) \,.\, Q_0 \,.\, Q_3 + \overline{(UP/\overline{DN}) \,.\, \overline{Q}_0 \,.\, \overline{Q}_1 \,.\, \overline{Q}_2 \,.\, \overline{Q}_3}\}}$$

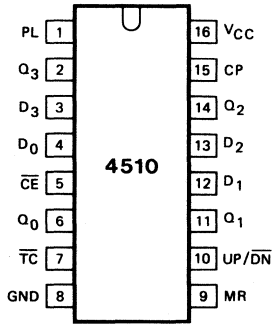


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
f_{max}	maximum clock frequency		45	45	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4510P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4510D; PC74HC/HCT4510D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4510T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D_0 to D_3	parallel inputs
5	$\overline{CE}$	count enable input (active LOW)
6, 11, 14, 2	Q_0 to Q_3	parallel outputs
7	$\overline{TC}$	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/$\overline{DN}$	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

FEATURES

- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output

GENERAL DESCRIPTION

The 54/74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with "4511" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D_1 to D_4), an active LOW latch enable input ($\overline{LE}$), an active LOW ripple blanking input ($\overline{BI}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH segment outputs (Q_a to Q_g).

When $\overline{LE}$ is LOW, the state of the segment outputs (Q_a to Q_g) is determined by the data on D_1 to D_4.
When $\overline{LE}$ goes HIGH, the last data present on D_1 to D_4 are stored in the latches and the segment outputs remain stable.
When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.

APPLICATIONS

- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	C_L = 15 pF; V_{CC} = 5 V	22	25	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4511D; PC74HC/HCT4511D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4511P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4511T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	$\overline{LT}$	lamp test input (active LOW)
4	$\overline{BI}$	ripple blanking input (active LOW)
5	$\overline{LE}$	latch enable input (active LOW)
7, 1, 2, 6	D_1 to D_4	BCD address inputs
8	GND	ground (0 V)
13, 12, 11, 10, 9, 15, 14	Q_a to Q_g	segments outputs
16	V_{CC}	positive supply voltage

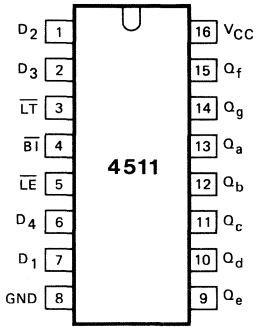


Fig. 1 Pin configuration.

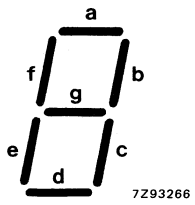


Fig. 2 Segment designation.

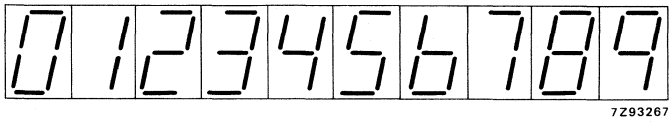


Fig. 3 Display.

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D_4	D_3	D_2	D_1	Q_a	Q_b	Q_c	Q_d	Q_e	Q_f	Q_g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	*							*

* Depends upon the BCD-code applied during the LOW-to-HIGH transition of $\overline{LE}$.

H = HIGH voltage level
L = LOW voltage level
X = don't care

4-TO-16 LINE DECODER/DEMULTIPLEXER WITH INPUT LATCHES

FEATURES

- **Non-inverting outputs**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with "4514" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4514 are 1-of-16 decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3), a latch enable input (LE), and an active LOW enable input ($\overline{E}$). The 16 outputs (Q_0 to Q_{15}) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input ($\overline{E}$) does not affect the state of the latch.

When the "4514" is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

APPLICATIONS

- **Digital multiplexing**
- **Address decoding**
- **Hexadecimal/BCD decoding**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n	C_L = 15 pF; V_{CC} = 5 V	21	23	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4514P: 24-lead DIL; plastic (SOT-101A).
PC54HC/HCT4514D; PC74HC/HCT4514D: 24-lead DIL; ceramic (cerdip) (SOT-94).
PC74HC/HCT4514T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A_0 to A_3	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	Q_0 to Q_{15}	multiplexer outputs (active HIGH)
12	GND	ground (0 V)
23	$\overline{E}$	enable input (active LOW)
24	V_{CC}	positive supply voltage

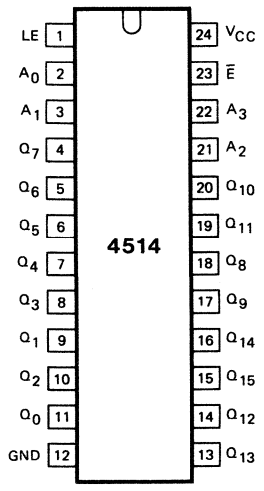


Fig. 1 Pin configuration.

FUNCTION TABLE

INPUTS					OUTPUTS														
$\overline{E}$	A_0	A_1	A_2	A_3	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

LE = HIGH
H = HIGH voltage level
L = LOW voltage level
X = don't care

4-TO-16 LINE DECODER/DEMULTIPLEXER WITH INPUT LATCHES

FEATURES

- **Inverting outputs**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4515 are high-speed Si-gate CMOS devices and are pin compatible with "4515" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4515 are 1-of-16 decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3), a latch enable input (LE), and an active LOW enable input ($\overline{E}$). The 16 inverting outputs ($\overline{Q}_0$ to $\overline{Q}_{15}$) are mutually exclusive active LOW. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input ($\overline{E}$) does not affect the state of the latch.

When the "4515" is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

APPLICATIONS

- **Digital multiplexing**
- **Address decoding**
- **Hexadecimal/BCD decoding**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	21	23	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4515P: 24-lead DIL; plastic (SOT-101A).
PC54HC/HCT4515D; PC74HC/HCT4515D: 24-lead DIL; ceramic (cerdip) (SOT-94).
PC74HC/HCT4515T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A_0 to A_3	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	$\overline{Q}_0$ to $\overline{Q}_{15}$	multiplexer outputs (active HIGH)
12	GND	ground (0 V)
23	$\overline{E}$	enable input (active LOW)
24	V_{CC}	positive supply voltage

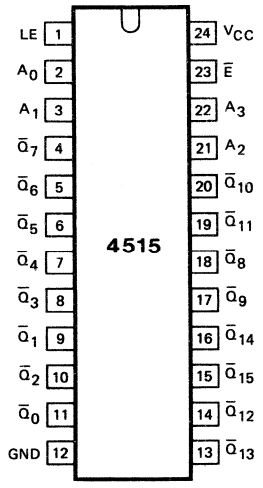


Fig. 1 Pin configuration.

FUNCTION TABLE

INPUTS					OUTPUTS														
$\overline{E}$	A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$	$\overline{O}_{10}$	$\overline{O}_{11}$	$\overline{O}_{12}$	$\overline{O}_{13}$	$\overline{O}_{14}$	$\overline{O}_{15}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

LE = HIGH
H = HIGH voltage level
L = LOW voltage level
X = don't care

BINARY UP/DOWN COUNTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4516 are high-speed Si-gate CMOS devices and are pin compatible with the "4516" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4516 are edge-triggered synchronous up/down 4-bit binary counters with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D_0 to D_3), four parallel outputs (Q_0 to Q_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL and $\overline{CE}$ are LOW, the counter changes on the LOW-to-HIGH transition of CP. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when Q_0 to Q_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when Q_0 to Q_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (Q_0 to Q_3 = = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE} \,.\, \{(UP/\overline{DN}) \,.\, Q_0 \,.\, Q_1 \,.\, Q_2 \,.\, Q_3 + \overline{(UP/\overline{DN})} \,.\, \overline{Q}_0 \,.\, \overline{Q}_1 \,.\, \overline{Q}_2 \,.\, \overline{Q}_3\}}$$

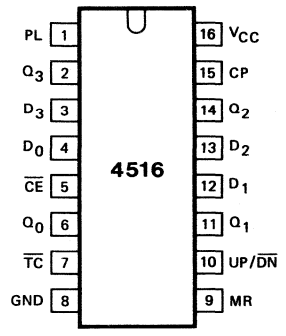


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	19	19	ns
f_{max}	maximum clock frequency		45	45	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4516D; PC74HC/HCT4516D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4516P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4516T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D_0 to D_3	parallel inputs
5	$\overline{CE}$	count enable input (active LOW)
6, 11, 14, 2	Q_0 to Q_3	parallel outputs
7	$\overline{TC}$	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/$\overline{DN}$	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

DUAL SYNCHRONOUS BCD COUNTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4518 are high-speed Si-gate CMOS devices and are pin compatible with the "4518" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4518 are dual 4-bit internally synchronous BCD counters with an active HIGH clock input (nCP_0) and an active LOW clock input ($n\overline{CP}_1$), buffered outputs from all four bit positions (nQ_0 to nQ_3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP_0 if $n\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of $n\overline{CP}_1$ if nCP_0 is LOW. Either nCP_0 or $n\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ_0 to nQ_3 = LOW) independent of nCP_0 and $n\overline{CP}_1$.

APPLICATIONS

- **Multistage synchronous counting**
- **Multistage asynchronous counting**
- **Frequency dividers**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_0	C_L = 15 pF; V_{CC} = 5 V	12	14	ns
f_{max}	maximum clock frequency		50	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4518P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4518D; PC74HC/HCT4518D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4518T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1CP_0$, $2CP_0$	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	$1\overline{CP}_1$, $2\overline{CP}_1$	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	$1Q_0$ to $1Q_3$	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	$2Q_0$ to $2Q_3$	data outputs
16	V_{CC}	positive supply voltage

FUNCTION TABLE

nCP_0	$n\overline{CP}_1$	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q_0 to Q_3 = LOW

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

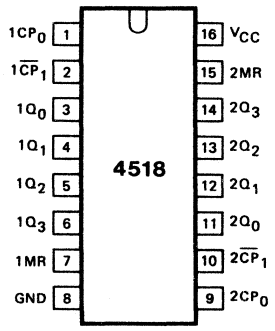


Fig. 1 Pin configuration.

DUAL 4-BIT SYNCHRONOUS BINARY COUNTER

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4520 are high-speed Si-gate CMOS devices and are pin compatible with the "4520" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4520 are dual 4-bit internally synchronous binary counters with an active HIGH clock input (nCP_0) and an active LOW clock input ($n\overline{CP}_1$), buffered outputs from all four bit positions (nQ_0 to nQ_3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP_0 if $n\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of $n\overline{CP}_1$ if nCP_0 is LOW. Either nCP_0 or $n\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ_0 to nQ_3 = LOW) independent of nCP_0 and $n\overline{CP}_1$.

APPLICATIONS

- **Multistage synchronous counting**
- **Multistage asynchronous counting**
- **Frequency dividers**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_0	C_L = 15 pF; V_{CC} = 5 V	12	14	ns
f_{max}	maximum clock frequency		50	50	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4520P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4520D; PC74HC/HCT4520D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4520T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1CP_0$, $2CP_0$	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	$1\overline{CP}_1$, $2\overline{CP}_1$	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	$1Q_0$ to $1Q_3$	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	$2Q_0$ to $2Q_3$	data outputs
16	V_{CC}	positive supply voltage

FUNCTION TABLE

nCP_0	$n\overline{CP}_1$	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q_0 to Q_3 = LOW

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

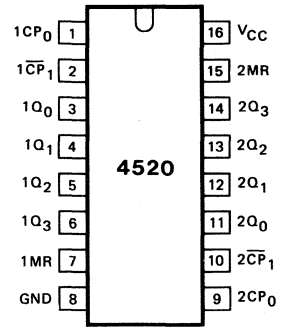


Fig. 1 Pin configuration.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR

FEATURES

- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with "4538" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input ($n\overline{A}_0$), an active HIGH trigger/retrigger input (nA_1), an overriding active LOW direct reset input ($n\overline{R}_D$), an output (nQ) and its complement ($n\overline{Q}$), and two pins (nC_{TC} and nRC_{TC}) for connecting the external timing components C_t and R_t. Typical pulse width variation over temperature range is ± 0.2%.

The "4538" may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t. The output pulse width (T) is equal to $R_t \times C_t$. The linear design techniques guarantee precise control of the output pulse width.

A LOW level at $n\overline{R}_D$ terminates the output pulse immediately. The minimum reset pulse width depends on the value of the external timing capacitor C_t.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}_0$, nA_1 to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	23	25	ns
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4538P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT4538D; PC74HC/HCT4538D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4538T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1C_{TC}$, $2C_{TC}$	external capacitor connections
2, 14	$1RC_{TC}$, $2RC_{TC}$	external resistor/capacitor connections
3, 13	$1\overline{R}_D$, $2\overline{R}_D$	direct reset inputs (active LOW)
4, 12	$1A_1$, $2A_1$	trigger inputs (LOW-to-HIGH, edge-triggered)
5, 11	$1\overline{A}_0$, $2\overline{A}_0$	trigger inputs (HIGH-to-LOW, edge-triggered)
6, 10	1Q, 2Q	pulse outputs
7, 9	$1\overline{Q}$, $2\overline{Q}$	complementary pulse outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{A}_0$	nA_1	$n\overline{R}_D$	nQ	$n\overline{Q}$
↓	L	H	⎍	⎍
H	↑	H	⎍	⎍
X	X	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎍ = one LOW level output pulse

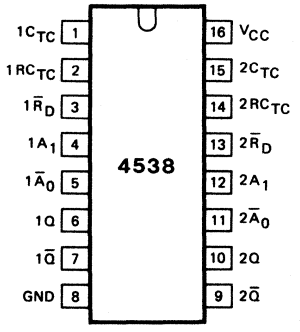


Fig. 1 Pin configuration.

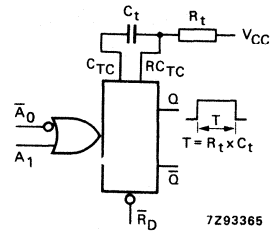


Fig. 2 Connection of the external timing components R_t and C_t.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER FOR LCDs

FEATURES

- Latch storage of BCD inputs
- Blanking inputs
- Output capability: non-standard

GENERAL DESCRIPTION

The 54/74HC/HCT4543 are high-speed Si-gate CMOS devices and are pin compatible with "4543" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT4543 are BCD to 7-segment latch/decoder/drivers for liquid crystal displays. They have four address inputs (D_0 to D_3), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (Q_a to Q_g).

The "4543" provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder driver. The "4543" can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the "4543" are directly connected to the segments of the liquid crystal.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n LD to Q_n BI to Q_n	C_L = 15 pF V_{CC} = 5 V	 29 32 23	 35 37 28	 ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	42	42	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC54HC/HCT4543D; PC74HC/HCT4543P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4543D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT4543T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	latch disable input (active HIGH)
5, 3, 2, 4	D_0 to D_3	address (data) inputs
6	PH	phase input (active HIGH)
7	BI	blanking input (active HIGH)
8	GND	ground (0 V)
9, 10, 11, 12 13, 15, 14	Q_a to Q_g	segment outputs
16	V_{CC}	positive supply voltage

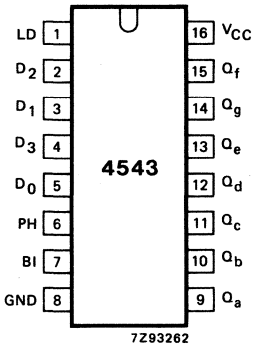


Fig. 1 Pin configuration.

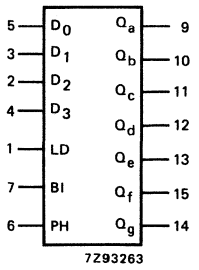


Fig. 2 Logic symbol.

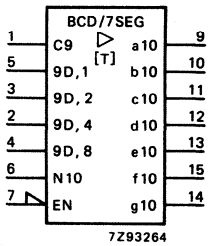


Fig. 3 IEC logic symbol.

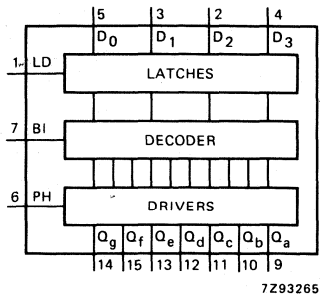


Fig. 4 Functional diagram.

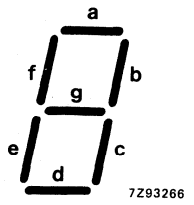


Fig. 5 Segment designation.

APPLICATIONS

- Driving LCD displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
LD	BI	PH*	D_3	D_2	D_1	D_0	Q_a	Q_b	Q_c	Q_d	Q_e	Q_f	Q_g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				**				**
as above		H	as above				inverse of above							as above

* For liquid crystal displays, apply a square-wave to PH.

** Depends upon the BCD-code previously applied when LD = HIGH.

H = HIGH voltage level
L = LOW voltage level
X = don't care

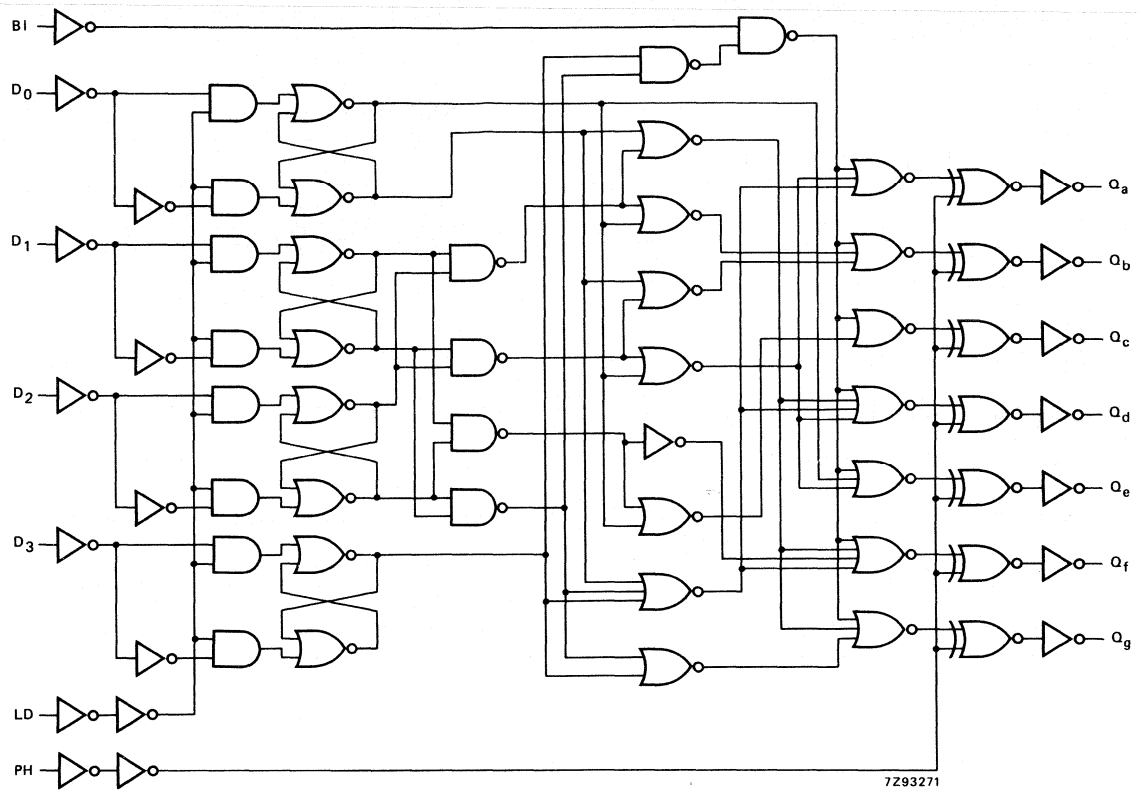


Fig. 6 Logic diagram.

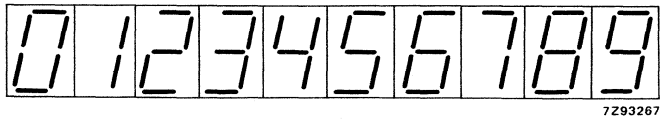


Fig. 7 Display.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 1.0$ mA $-I_O = 1.3$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 1.0$ mA $I_O = 1.3$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_0, D_1, D_2	1.00
D_3	0.50
BI	0.50
LD	1.50
PH	1.25

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n			340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay LD to Q_n			370 74 63		465 93 79		555 111 94	ns	2.0 4.5 6.0	Fig. 13
t_{PHL}/t_{PLH}	propagation delay BI to Q_n			265 53 45		330 66 56		495 99 84	ns	2.0 4.5 6.0	Fig. 14
t_{THL}/t_{TLH}	output transition time			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	35 7 6			45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 13
t_{su}	set-up time D_n to LD	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 15
t_h	hold time D_n to LD	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 15

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			−40 to +85		−55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n			80		100		120	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay LD to Q_n			86		108		129	ns	4.5	Fig. 13
t_{PHL}/t_{PLH}	propagation delay BI to Q_n			66		83		125	ns	4.5	Fig. 14
t_{THL}/t_{TLH}	output transition time			50		63		75	ns	4.5	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 13
t_{su}	set-up time D_n to LD	12			15		18		ns	4.5	Fig. 15
t_h	hold time D_n to LD	8			10		12		ns	4.5	Fig. 15

DEVELOPMENT DATA

APPLICATION DIAGRAMS

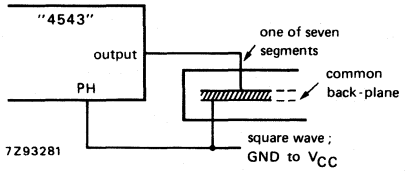


Fig. 8 Connection to liquid crystal (LCD) display readout.

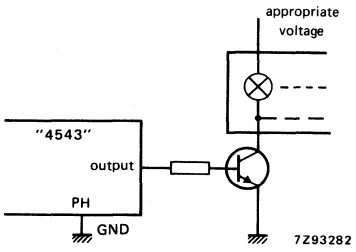


Fig. 9 Connection to incandescent display readout.

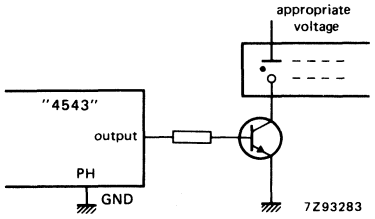


Fig. 10 Connection to gas discharge display readout.

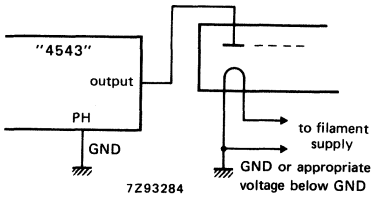


Fig. 11 Connection to fluorescent display readout.

AC WAVEFORMS

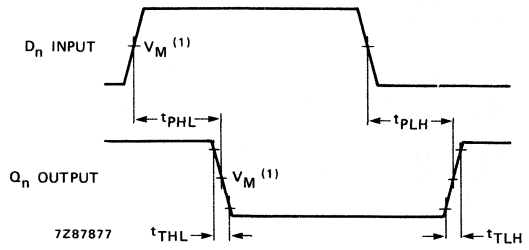


Fig. 12 Waveforms showing the address input (D_n) to output (Q_n) propagation delays and the output transition times.

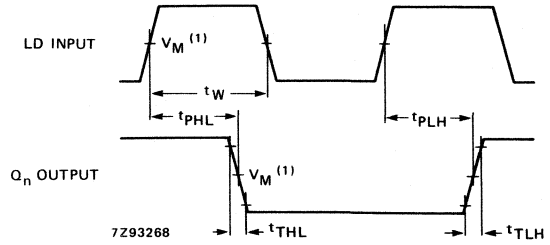


Fig. 13 Waveforms showing the latch disable input (LD) to output (Q_n) propagation delays and the output transition times.

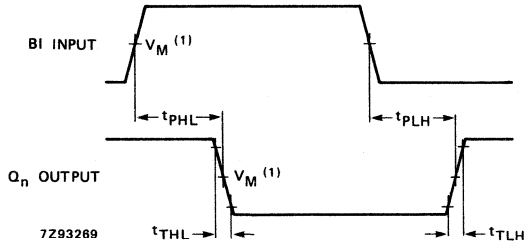


Fig. 14 Waveforms showing the blanking (BI) to output (Q_n) propagation delays and the output transition times.

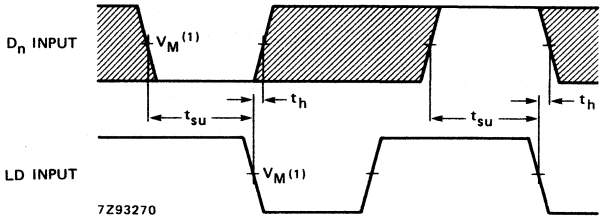


Fig. 15 Waveforms showing the address (D_n) to latch disable (LD) input set-up and hold times.

Note to Fig. 15

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

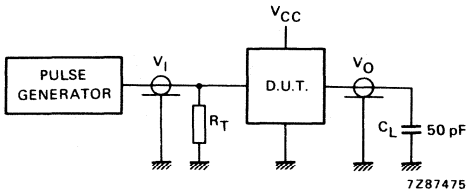


Fig. 16 Test circuit.

Definitions for Figs 16 and 17:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

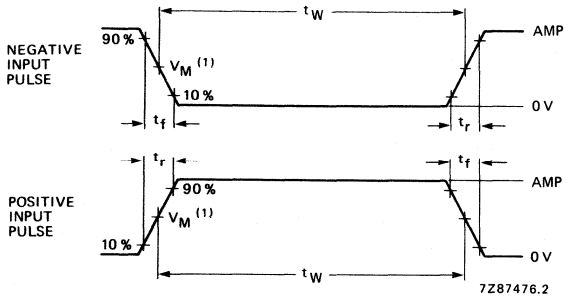


Fig. 17 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

8-BIT SYNCHRONOUS BCD DOWN COUNTER

FEATURES

- **Cascadable**
- **Synchronous or asynchronous preset**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT40102 are high-speed Si-gate CMOS devices and are pin compatible with the "40102" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT40102 consist each of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The "40102" is configured as two cascaded 4-bit BCD counters and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P_0 to P_7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$.
When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P_0 to P_7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P_0 to P_7) represent two 4-bit BCD words.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	C_L = 15 pF; V_{CC} = 5 V	25	26	ns
f_{max}	maximum clock frequency		16	15	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40102P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT40102D; PC74HC/HCT40102D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT40102T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	$\overline{MR}$	asynchronous master reset inputs (active LOW)
3	$\overline{TE}$	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P_0 to P_7	jam inputs
8	GND	ground (0 V)
9	$\overline{PL}$	asynchronous preset enable input (active LOW)
14	$\overline{TC}$	terminal count output (active LOW)
15	$\overline{PE}$	synchronous preset enable input (active LOW)
16	V_{CC}	positive supply voltage

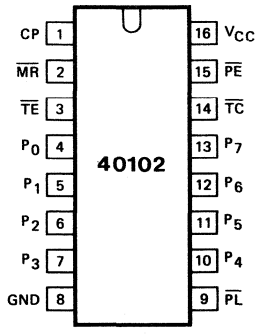


Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 99) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 clock pulses long.

The "40102" may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

APPLICATIONS

- **Divide-by-n counters**
- **Programmable timers**
- **Interrupt timers**
- **Cycle/program counters**

FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X		preset on next LOW-to HIGH clock transition
H	L	X	X	asynchronous	preset asynchronously
L	X	X	X		clear to maximum count

Notes to function table

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P_7, LSD = P_0.

H = HIGH voltage level
L = LOW voltage level
X = don't care

8-BIT BINARY DOWN COUNTER

FEATURES

- **Cascadable**
- **Synchronous or asynchronous preset**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT40103 are high-speed Si-gate CMOS devices and are pin compatible with the "40103" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT40103 consist each of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The "40103" contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P_0 to P_7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$.
When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P_0 to P_7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P_0 to P_7) represent a single 8-bit binary word.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	C_L = 15 pF; V_{CC} = 5 V	25	26	ns
f_{max}	maximum clock frequency		16	15	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40103P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT40103D; PC74HC/HCT40103D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT40103T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	$\overline{MR}$	asynchronous master reset inputs (active LOW)
3	$\overline{TE}$	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P_0 to P_7	jam inputs
8	GND	ground (0 V)
9	$\overline{PL}$	asynchronous preset enable input (active LOW)
14	$\overline{TC}$	terminal count output (active LOW)
15	$\overline{PE}$	synchronous preset enable input (active LOW)
16	V_{CC}	positive supply voltage

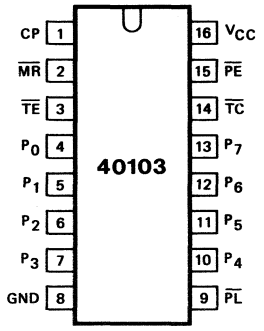


Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.

The "40103" may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

APPLICATIONS

- **Divide-by-n counters**
- **Programmable timers**
- **Interrupt timers**
- **Cycle/program counters**

FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X		preset on next LOW-to HIGH clock transition
H	L	X	X	asynchronous	preset asynchronously
L	X	X	X		clear to maximum count

Notes to function table

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P_7, LSD = P_0.

H = HIGH voltage level
L = LOW voltage level
X = don't care

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER; 3-STATE

FEATURES

- Synchronous parallel or serial operating
- 3-state outputs
- Output capability: bus driver

GENERAL DESCRIPTION

The 54/74HC/HCT40104 are high-speed Si-gate CMOS devices and are pin compatible with the "40104" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT40104 are universal shift registers featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs and 3-state outputs allowing the devices to be used in bus-organized systems.

In the parallel-load mode (S_0 and S_1 are HIGH), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP).

During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right (D_{SR}) and shift-left (D_{SL}) serial inputs, respectively.

Clearing the register is accomplished by setting both mode controls (S_0 and S_1) LOW and clocking the register.
When the output enable input (OE) is LOW, all outputs assume the high-impedance OFF-state (Z).

APPLICATIONS

- Arithmetic unit bus registers
- Serial/parallel conversion
- General-purpose register for bus organized systems
- General-purpose registers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	14	14	ns
f_{max}	maximum clock frequency		54	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	75	75	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40104P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT40104D; PC74HC/HCT40104D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT40104T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	OE	3-state output enable input (active HIGH)
2	D_{SR}	serial data shift-right input
3, 4, 5, 6	D_0 to D_3	parallel data inputs
7	D_{SL}	serial data shift-left input
8	GND	ground (0 V)
9, 10	S_0, S_1	mode control inputs
11	CP	clock input (LOW-to-HIGH, edge-triggered)
15, 14, 13, 12	Q_0 to Q_3	3-state parallel outputs
16	V_{CC}	positive supply voltage

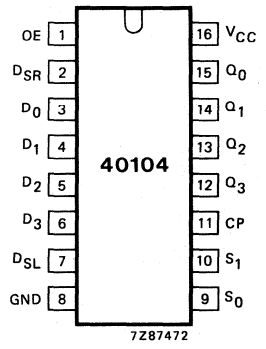


Fig. 1 Pin configuration.

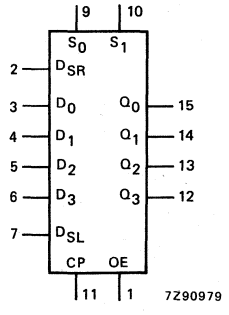


Fig. 2 Logic symbol.

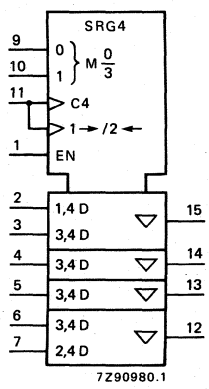


Fig. 3 IEC logic symbol.

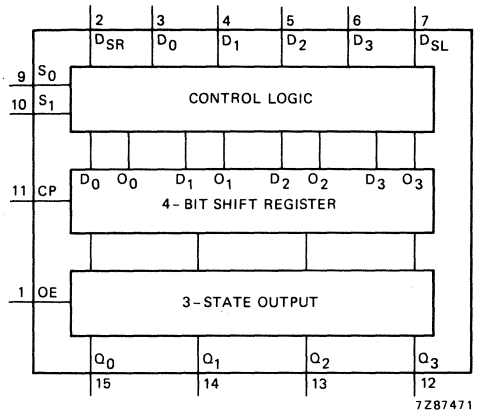


Fig. 4 Functional diagram.

FUNCTION TABLE

H = HIGH voltage level
L = LOW voltage level
X = don't care
t_{n+1} = state after next LOW-to-HIGH transition of CP

OPERATING MODES	INPUTS (OE = HIGH)					OUTPUTS at t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	D_0 to D_3	Q_0	Q_1	Q_2	Q_3
reset	L	L	X	X	X	L	L	L	L
shift left	H	L	X	L	X	Q_1	Q_2	Q_3	L
	H	L	X	H	X	Q_1	Q_2	Q_3	H
shift right	L	H	L	X	X	L	Q_0	Q_1	Q_2
	L	H	H	X	X	H	Q_0	Q_1	Q_2
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

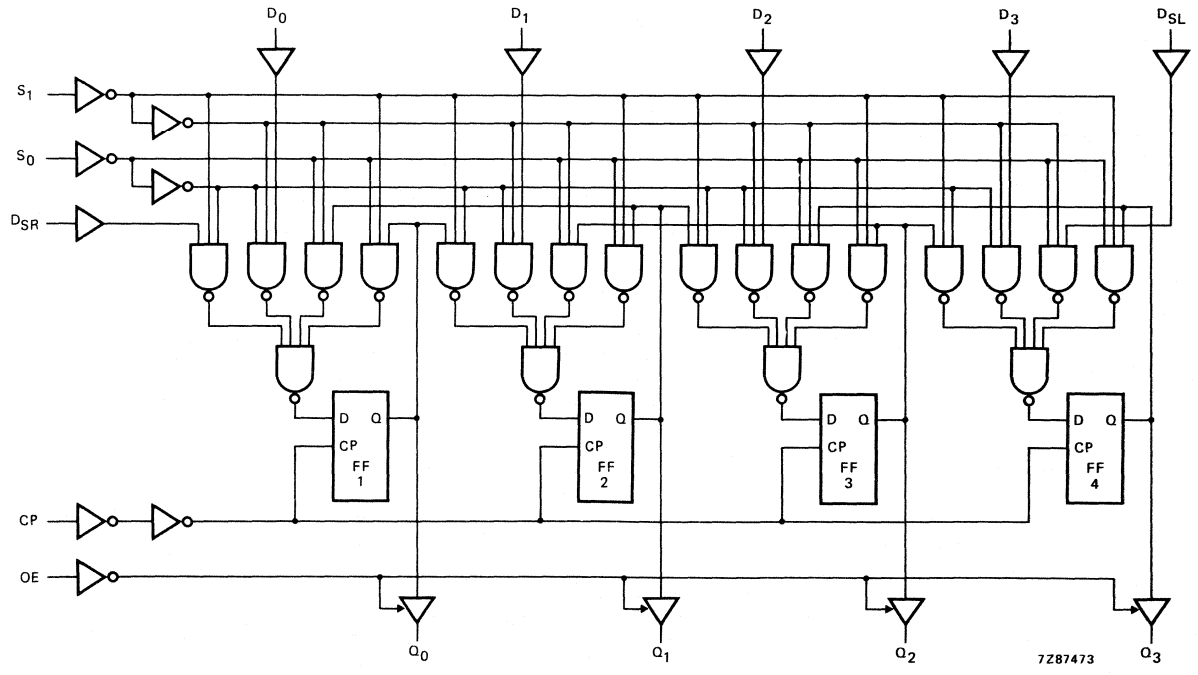


Fig. 5 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		35	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for standard temperature range; −40 to +85 °C; 74HC/HCT
	plastic and ceramic (cerdip) DIL		500	mW	above +60° C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		300	mW	above +60°C: derate linearly with 5 mW/K
P_{tot}	power dissipation per package				for extended temperature range; −55 to +125°C; 54HC/HCT
	ceramic (cerdip) DIL		500	mW	above +100°C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54/74HC			54/74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	74HC/HCT
T_{amb}	operating ambient temperature range	−55		+125	−55		+125	°C	54HC/HCT
t_r, t_f	input rise and fall times		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

DC CHARACTERISTICS FOR 54/74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HC			74HC		54HC			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

DC CHARACTERISTICS FOR 54/74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		54/74HCT			74HCT		54HCT			V_{CC} V	V_I	OTHER
		+25			−40 to +85		−55 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
D_0 to D_3	0.35
D_{SR}, D_{SL}	0.35
CP	0.35
S_0, S_1	0.70
OE	1.40

AC CHARACTERISTICS FOR 54/74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HC			74HC		54HC			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time OE to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time OE to Q_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n, D_{SR}, D_{SL} to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time S_0, S_1 to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n, D_{SR}, D_{SL} to CP	2 2 2			2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time S_0, S_1 to CP	2 2 2			2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	5 25 29			4 20 24		3 16 19		MHz	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 54/74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		54/74HCT			74HCT		54HCT			V_{CC} V	WAVEFORMS
		+25			-40 to +85		-55 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			34		43		51	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time OE to Q_n			30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time OE to Q_n			35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 6
t_{su}	set-up time D_n, D_{SR}, D_{SL} to CP	20			25		30		ns	4.5	Fig. 8
t_{su}	set-up time S_0, S_1 to CP	20			25		30		ns	4.5	Fig. 8
t_h	hold time D_n, D_{SR}, D_{SL} to CP	2			2		2		ns	4.5	Fig. 8
t_h	hold time S_0, S_1 to CP	2			2		2		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	25			19		16		MHz	4.5	Fig. 6

DEVELOPMENT DATA

AC WAVEFORMS

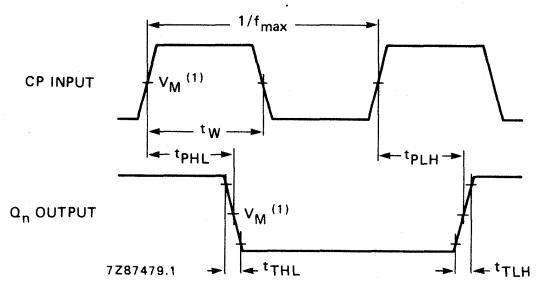


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

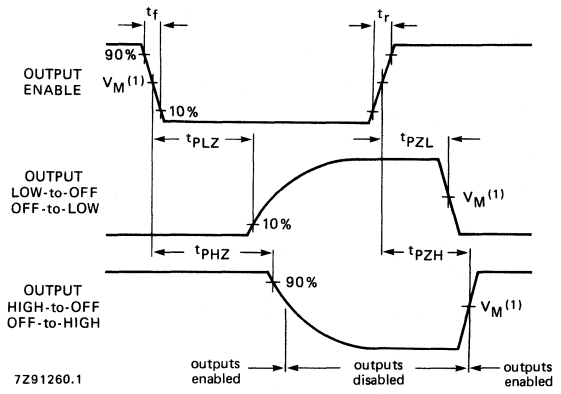


Fig. 7 Waveforms showing the 3-state enable and disable times.

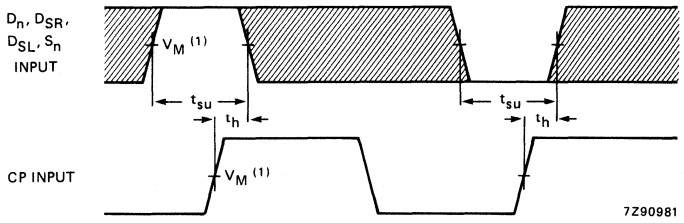


Fig. 8 Waveforms showing the set-up and hold times from the D_n, D_{SR}, D_{SL} and S_n inputs to the clock (CP).

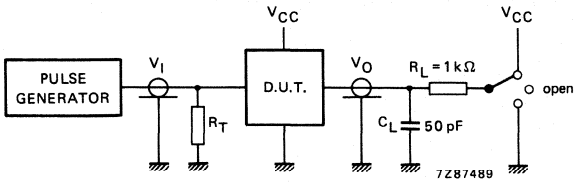
Note to Fig 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}
others	open

Fig. 9 Test circuit for 3-state outputs.

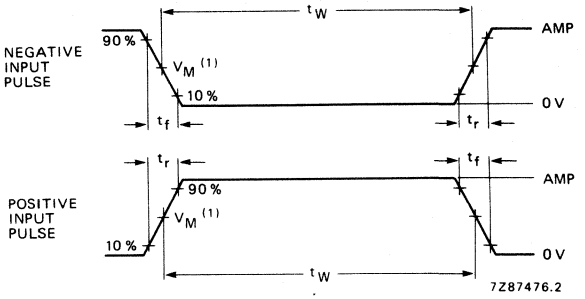


Fig. 10 Input pulse definitions.

Definitions for Figs 9 and 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
54/74HC	V_{CC}	$V_{CC}/2$	< 2 ns	6 ns
54/74HCT	3.0 V	1.3 V	< 2 ns	6 ns

4-BIT X 16-WORD FIFO REGISTER

FEATURES

- **Independent asynchronous inputs and outputs**
- **Expandable in either direction**
- **Reset capability**
- **Status indicators on inputs and outputs**
- **3-state outputs**
- **Output capability: standard**

GENERAL DESCRIPTION

The 54/74HC/HCT40105 are high-speed Si-gate CMOS devices and are pin compatible with the "40105" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 54/74HC/HCT40105 are first-in/first-out (FIFO) "elastic" storage registers that can store sixteen 4-bit words. The "40105" is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flop have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (data-in ready output - DIR) indicates if the FIFO is full,

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay SI to DIR, DOR	C_L = 15 pF; V_{CC} = 5 V	14	16	ns
f_{max}	maximum clock frequency		16	15	MHz
C_I	input capacitance		3.5	3.5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40105P: 16-lead DIL; plastic (SOT-38Z).
PC54HC/HCT40105D; PC74HC/HCT40105D: 16-lead DIL; ceramic (cerdip) (SOT-74).
PC74HC/HCT40105T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2	DIR	data-in ready output
3	SI	shift-in input (LOW-to-HIGH, edge-triggered)
4, 5, 6, 7	D_0 to D_3	parallel data inputs
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
13, 12, 11, 10	Q_0 to Q_3	3-state data outputs
14	DOR	data-out ready output
15	$\overline{SO}$	shift-out input (HIGH-to-LOW, edge-triggered)
16	V_{CC}	positive supply voltage

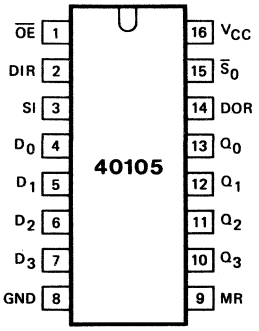


Fig. 1 Pin configuration.

GENERAL DESCRIPTION (Cont'd)

and the status of the last flip-flop (data-out ready output - DOR) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (output end), all data entered later will automatically ripple toward the output.

Loading data

Data can be entered whenever the DIR flag is HIGH, by a LOW-to-HIGH transition on the shift-in input (SI). This input must go LOW momentarily before the next word is accepted by the FIFO. The DIR flag will go LOW momentarily, until the data have been transferred to the second location. The DIR flag remains LOW when all 16 word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes HIGH.

Unloading data

As soon as the first word has rippled to the output, the data-out ready output (DOR) goes HIGH and data of the first word is available on the outputs.

Data of other words can be removed by a negative-going transition on the shift-out input ($\overline{SO}$). This negative-going transition causes the DOR signal to go LOW, while the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go HIGH again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain LOW, and any further commands will be ignored until a "1" marker ripples down to the last control register and DOR goes HIGH.
If during unloading SI is LOW, data on the data input of the FIFO is entered in the first location.

Master reset

A HIGH on the master reset input (MR) sets all the control logic marker bits to "0". DOR goes LOW and DIR goes HIGH. The contents of the data register are not changed but will be superseded when the first word is loaded. Thus MR does not clear data within the register but only the control logic. If the shift-in flag (SI) is HIGH during the master reset pulse, data present at the input (D_0 to D_3) is immediately moved into the first location upon completion of the reset process.

3-state outputs

In order to facilitate data busing, 3-state outputs (Q_0 to Q_3) are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output. A HIGH on the 3-state control flag (output enable input - $\overline{OE}$) forces the outputs into the high-impedance OFF-state mode.

Cascading

The "40105" can be cascaded to form longer register simply by connecting the DIR outputs to the $\overline{SO}$ inputs and the DOR outputs to the SI inputs. In the cascading mode, as master reset pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and DOR outputs must be gated together with AND gates. Their outputs drive the SI and $\overline{SO}$ inputs in parallel, if expanding is done in both directions.

APPLICATIONS

- **Bit-rate smoothing**
- **CPU/terminal buffering**
- **Data communications**
- **Peripheral buffering**
- **Line printer input buffers**
- **Auto-diallers**
- **CRT buffer memories**
- **Radar data acquisition**

IEC SYMBOLOGY

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SUMMARY OF IEC SYMBOLOGY

INTRODUCTION

The logic symbology used in this handbook follows the system developed by the International Electrotechnical Commission (IEC). The representation is very effective in that it shows the exact relationship between every input and output of digital circuits without having to detail internal logic. Basic logic functions are represented by symbols; in the symbols for more complex functions, use is made of 'dependency notation' that specifies inter- relationships of the digital inputs/outputs.

This summary describes the various elements used in symbol construction and the rules and definitions that apply.

SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying-symbols (Fig. 1). The purpose of a general qualifying-symbol is to accurately portray the logic function of the element and those used in this handbook are listed in Table 1. The preferred direction of signal flow through symbols and associated circuit is from left to right; inputs are on the left and outputs on the right. Exceptions to this convention are indicated by arrowheads in the signal lines showing the direction of signal flow, as shown in Fig. 12.

All outputs of a single element of a symbol have internal logic states that are determined by the element's function, unless otherwise indicated by an associated qualifying- symbol.

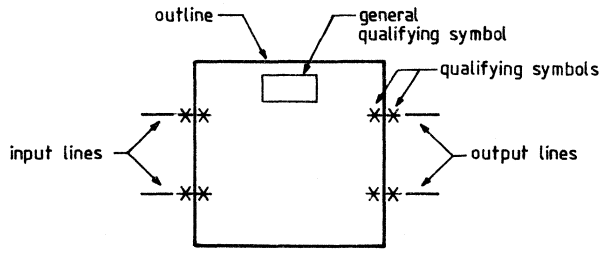


Fig. 1 Symbol composition.

Adjacent elements in a composite symbol may be joined by a common boundary line. When this boundary line is parallel to the direction of signal flow there is no logic connection between the elements, but when the line is perpendicular to the direction of signal flow then there is at least one logic connection between them. The number of logic connections between elements is shown by qualifying- symbols, but if there are no qualifying-symbols on either side of the common line then the elements have just one logic connection.

When a composite symbol contains at least one input common to one or more of the elements, a common-control block can be used. In the example of Fig. 2 the common-control block provides an input to each of the elements below it, this can be otherwise qualified by dependency notation.

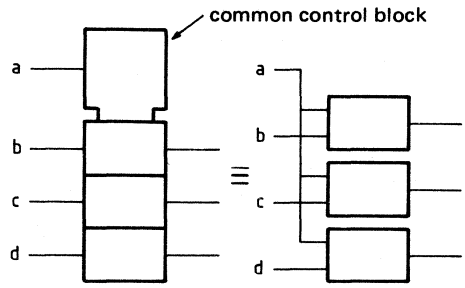


Fig. 2 Common-control block.

An output that depends on all elements of a composite symbol can be shown as an output from a common-output element. This part of the symbol is distinguishable by a double boundary line as shown in Fig. 3. The common-output element may have other inputs. Its function must be indicated by a qualifying-symbol within the outline.

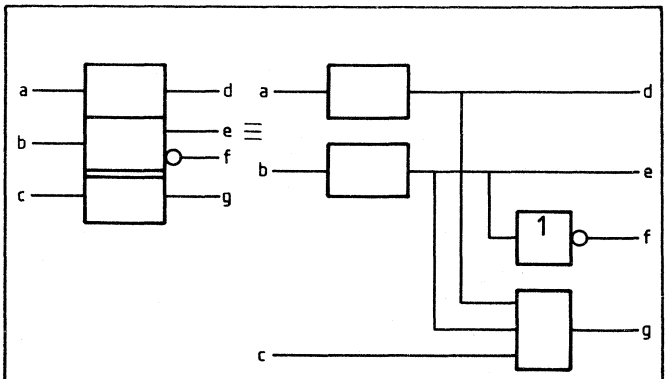
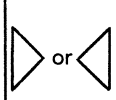


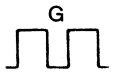
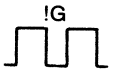
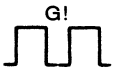
Fig. 3 Common-output element.

GENERAL QUALIFYING-SYMBOLS

Table 1 shows the general qualifying-symbols used in this publication. These characters are usually placed near the top centre of a symbol element and define the logic function that is represented by the symbol or element.

Table 1 Qualifying-symbols - General

qualifying-symbol	definition
&	AND element. If all inputs are at internal logic "1" then the output is at internal logic "1"
≥m	Logic threshold element. If at least m inputs are at internal logic "1" then the output is at internal logic "1"
≥1	OR element. If at least one input is at internal logic "1" then the output is at internal logic "1"
=m	m-out-of-n element. Given that m < n; if m inputs are at internal logic "1" then the output is at internal logic "1"
=1	EXCLUSIVE-OR element. If only one input is at internal logic "1" then the output is at internal logic "1"
=	Logic identity element. If all inputs have the same logic state then the output is at internal logic "1"
>n/2	Majority element. If the majority of inputs are at internal logic "1" then the output is at internal logic "1"
2k	Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1"
2k+1	Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1"
1	Buffer element without amplified output. If the input is at internal logic "1" then the output is at internal logic "1"
	Buffer element with amplified output. The triangle points in the direction of signal flow
	Bi-threshold detector. Schmitt-trigger
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used
MUX	Multiplexer/ data selector
DX	Demultiplexer
MUXDX	Bidirectional selector
Σ	Adder

qualifying-symbol	definition	
P-Q	Subtractor	
CPG	Look-ahead carry generator	
Π	Multiplier	
COMP	Comparator	
ALU	Arithmetic logic unit	
	Retriggerable monostable element	
	Non-retriggerable monostable element	
	Astable element	
	Synchronous-starting astable element	
	Synchronous-stopping astable element	
SGRm	Shift register. "m" = number of bits	
CTRm	Binary counter. "m" = number of bits or is an indication of the cycle length 2^m	
CTRDIVm	Counter with cycle length m	
ROMm1xm2	Read only memory	m1 is the number of words
PROMm1xm2	Programmable read only memory	
RAMm1xm2	Random access memory	
CAMm1xm2	Associative memory	m2 is the number of bits per word
FIFOm1xm2	First-in/first-out memory	
I=0	Initial logic "0" state. When power is switched ON, the element goes to internal logic "0"	

qualifying-symbol	definition
I = 1	Initial logic "1" state. When power is switched ON, the element goes to internal logic "1"
NV	Non-volatile. The internal logic state is maintained regardless of power ON or OFF
Φ	Very complicated element. Depicted by a 'grey box' symbol. Within the 'grey box' outline, the Φ qualifying-symbol is accompanied by a further qualifying expression, e.g. ERR - for error detector

QUALIFYING-SYMBOLS FOR INPUTS AND OUTPUTS

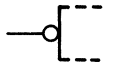
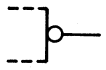
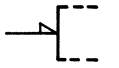
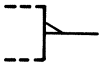
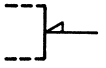
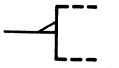
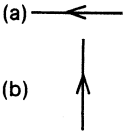
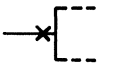
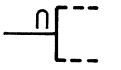
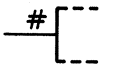
Referring to Table 2, qualifying-symbols for inputs and outputs, the logic negation indicator is used in pure logic diagrams to indicate that an external logic "0" ("1") produces an internal logic "1" ("0") at the input, or that an internal logic "1" ("0") produces an external logic "0" ("1") at the output.

The polarity indicator is used in detailed logic diagrams to indicate which logic level corresponds with the internal logic "1". The following may occur:

- an input or output **with** polarity indicator indicates that the logic level "L" (LOW) corresponds to an internal logic "1".
- an input or output **without** polarity indicator indicates that the logic level "H" (HIGH) corresponds to an internal logic "1".

In an array of elements, if the same general qualifying- symbol and the same qualifying-symbols associated with inputs and outputs should appear inside each element of the array, then they are usually shown only in the first element. Similarly, for large identical elements with subdivisions, the subdivisions may be shown only in the first element. This is done to simplify the array and ease recognition. As an example, omissions of both repeating qualifying-symbols and subdividing lines can be seen in the HC/HCT242 symbol.

Table 2 Qualifying-symbols - Inputs and Outputs

qualifying-symbol	definition of input or output
	Logic negation at an input. An external logic "0" ("1") produces an internal logic "1" ("0")
	Logic negation at an output. An internal logic "1" ("0") produces an external logic "0" ("1")
	Polarity indicator at an input. A logic "L" (LOW) level ("H" (HIGH) level) at an input produces an internal logic "1" at that input
	Polarity indicator at an output. An internal logic "1" ("0") at an output produces a logic "L" (LOW) level ("H" (HIGH) level) at that output
	Polarity indicator at an input where the signal flow is from right to left
	Polarity indicator at an output where the signal flow is from right to left
(a)  (b)	Indicator for direction of signal flow: (a) from right to left; (b) from bottom to top. With no indication of direction, flow is left to right or top to bottom
	Bidirectional information flow (alternate)
	Non-logic connection
	Input for analogue signals
	Input for digital signals (used only to avoid confusion)

Symbols inside the outline

Table 3 shows some of the symbols used within the symbol- outlines. Other symbols used in this handbook but not shown here are self-explanatory. Generally these are associated with arithmetic operations but all are in accordance with the IEC system. When non-standard information is shown inside a symbol-outline, it is enclosed in square brackets.

It can be seen in Table 3 that open-collector, open-emitter and three-state outputs have distinctive symbols. Note that an enable input (EN) affects all of the circuit outputs and has no effect on the inputs. When an enable input affects only certain outputs and/or one or more inputs, a form of dependency notation will indicate this (see 'Dependency Notation, EN-dependancy').

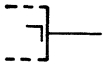
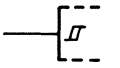
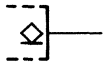
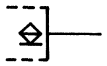
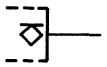
Another important point is that a D-input is always the data input of a storage element. An internal logic "1" at the D-input sets the storage element to its "1" state, and an internal logic "0" at the D-input resets the storage element to its "0" state.

Grouping of inputs or outputs is indicated by the bit- grouping symbol. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. The weights of input and output lines are represented by powers- of-two only when the bit-grouping symbol is used, otherwise decimal equivalents are used. Inputs grouped together by this symbol produce an internal number that is the sum of the individual input weights at logic "1". This number can be a number on which a mathematical function is performed, an identifying number used in dependency notation or a value that becomes the content (CT) of the element (see Fig. 29). A frequent use of the bit-grouping symbol is in memory addressing, see also 'Use of Bit-grouping to Produce Affecting Inputs'. For outputs, usage of the bit-grouping symbol is similar to that of inputs; the number produced by the sum of the output weights is the internal number, or the content (CT) produced by the circuit.

The symbols shown in Table 3 may be used to indicate the internal connections between logic elements abutted together. Each logic connection may be shown by qualifying- symbols at one or both sides of the common line, however, if confusion could arise about the number of connections, one of the internal connection symbols may be used.

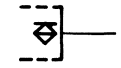
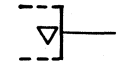
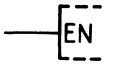
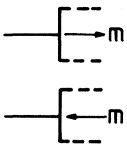
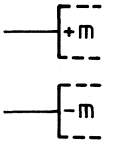
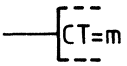
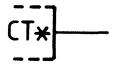
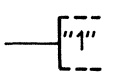
The internal (virtual) input is an input originating somewhere within the circuit and not connected directly to a terminal, and similarly the internal (virtual) output is not connected directly to a terminal.

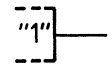
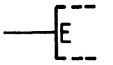
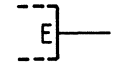
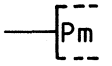
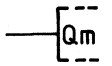
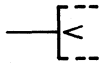
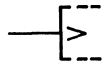
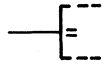
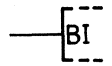
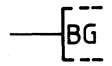
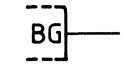
Table 3 Symbols inside the outline

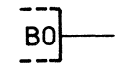
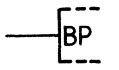
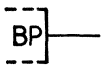
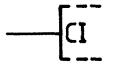
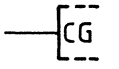
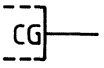
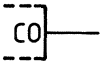
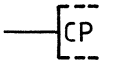
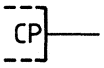
symbol inside outline	explanation
/	Solidus. Separator used in input and output labels. May be interpreted as an OR function
,	Comma. Separator with no logic significance
	Delayed output symbol for pulse and data-lock-out elements. The output change is delayed until the input that initiated the change (e.g. a "C" input) returns to its initial external state or level
	Bi-threshold inputs. Inputs with hysteresis
	Open output with low-impedance "L" (LOW) level
	Passive pull-up output. Similar to open output with low-impedance "L" level but with a built-in passive pull-up
	Open output with low-impedance "H" (HIGH) level

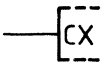
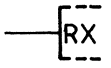
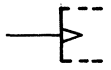
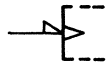
QUALIFYING-SYMBOLS (continued)

Table 3 Symbols inside the outline (continued)

symbol inside outline	explanation
	Passive pull-down output. Similar to open output with low-impedance "H" level but with a built-in passive pull-up
	Three-state output
	Enable input. When at internal logic "1", all outputs are enabled. When at internal logic "0": open outputs are OFF; three-state outputs retain their normal, defined internal logic state but give anexternal high-impedance state; all otheroutputs are at internal logic "0"
R, S, C, T	Control inputs of bistable elements
J, K, R, S, D	Information inputs of bistable elements
	Shift input. The direction of shift is to the right or down when the arrow points to the right, or to the left or up when the arrow points to the left. The number may be ommitted when "m" = 1
	Counting input. Count-up and count-down are indicated by + and - respectively. The number "m" is the count per command and may be ommitted when "m" = 1
	Bit-grouping symbol. "m" is the highest power of 2 in the group
	Content input. The internal logic "1" sets the element to the value "m"
	Content output. "*" is the value of the element that sets the output to an internal logic "1" (e.g. CT = 0, CT > 5, CT ≠ 4...9)
	Line-grouping symbol. The inputs or outputs enclosed by this symbol form a single logic input or output
	Fixed-mode input. This input is permanently at internal logic "1"

symbol inside outline	explanation
	Fixed-state output. This output is permanently at internal logic "1"
a...g	Seven segments of a display element
	Extension input. Input intended for connection to an extender output
	Extender output. Output to an extension input
	Operand input. This input represents one bit of an operand on which one or more mathematical functions are performed; "m" is the decimal equivalent of the **weight** of the bit. If the **weights** of all Pm inputs of the element are powers of 2 then "m" is the exponent of the power of 2
	Operand input. See Pm
	'Smaller-than' input to a magnitude comparator
	'Greater-than' input to a magnitude comparator
	'Equal' input to a magnitude comparator
	'Borrow-in' input to an arithmetic element
	'Borrow-generate' input to an arithmetic element
	'Borrow-generate' output from an arithmetic element

symbol inside outline	explanation
	'Borrow-out' output from an arithmetic element
	'Borrow-propagate' input to an arithmetic element
	'Borrow-propagate' output from an arithmetic element
	'Carry-in' input to an arithmetic element
	'Carry-generate' input to an arithmetic element
	'Carry-generate' output from an arithmetic element
	'Carry-out' output from an arithmetic
	'Carry-propagate' input to an arithmetic element
	'Carry-propagate' output from an arithmetic element
Π	Result of a multiplication
Σ	Result of an addition
P-Q	Result of a subtraction
[...]	Added information

symbol inside outline	explanation
φm	Clock phase. "m" is the clock phase number
	Connection for external capacitor(s)
	Connection for external resistor(s)
	Dynamic input. A transition from logic "L" level to "H" level produces a transitory internal logic "1"
	Dynamic input. A transition from logic "H" level to "L" level produces a transitory internal logic "1"
	Internal connection. A logic "1" at the left-hand side produces a logic "1" at the right-hand side
	Negated internal connection. A logic "1" at the left-hand side produces a logic "0" at the right-hand side
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left-hand side produces a transitory logic "1" at the right-hand side
	Negated dynamic internal connection. A transition from internal logic "1" to internal logic "0" at the left-hand side produces a transitory internal logic "1" at the right-hand side
	Internal (virtual) input. This input is always at internal logic "1" state unless this is overridden or modified
	Internal (virtual) output. The effect on the internal input connected to this output must be indicated by dependency notation

DEPENDENCY NOTATION

General conventions of dependency notation

Dependency notation is the powerful tool that makes IEC symbols compact and yet meaningful. With IEC symbols, the relationships between inputs and other inputs, between outputs and other outputs, and between inputs and outputs are clearly illustrated without the necessity to show all elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying-symbols for an element's function.

In dependency notation, the terms "affecting" and "affected" are used. In cases where it is not evident which inputs must be selected as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the most convenient input has been chosen.

The types of dependency described in this section are "G" (AND); "V" (OR); "N" (negate, or EXCLUSIVE-OR); "Z" (interconnection); "C" (control); "S" and "R" (set and reset); "EN" (enable); "M" (mode); and "A" (address).

The general rules applied to dependency notation are:

- the input (or output) affecting other inputs or outputs is labelled with the letter symbol that indicates the relationship involved (e.g. G for AND) followed by an appropriately-chosen identifying number; and
- each input or output affected by that affecting input (or output) is labelled with that same number.

If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together (see Fig. 4).

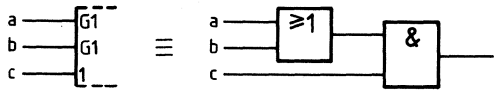


Fig. 4 ORed affecting inputs.

If an input or output is affected by more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal reading order of these numbers is the same as the sequence of the affecting relationships (see Fig. 5).

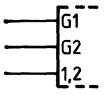


Fig. 5 Input affected by more than one input.

If the labels denoting the function of affected inputs or outputs are numbers, (e.g., outputs of a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, e.g., Greek letters (see Fig. 6).

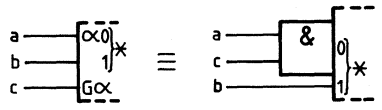


Fig. 6 Substitution for numbers.

If it is the complement of the input's (or output's) internal logic state that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (see Fig. 7).

If the affected input or output has a label to denote its function (e.g. "D"), this label will have the identifying number of the affecting input as a prefix (see Fig. 13).

G-dependency

The traditional method of showing an AND relationship was to use an explicit drawing of an AND gate with the signals connected to the inputs of the gate. With IEC symbology (see Fig. 7), input "b" and input "a" are ANDed together and the complement of "b" is ANDed with "c". The letter G has been chosen to indicate AND relationships and is placed at input "b", within the outline. A number considered appropriate by the designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input "c".

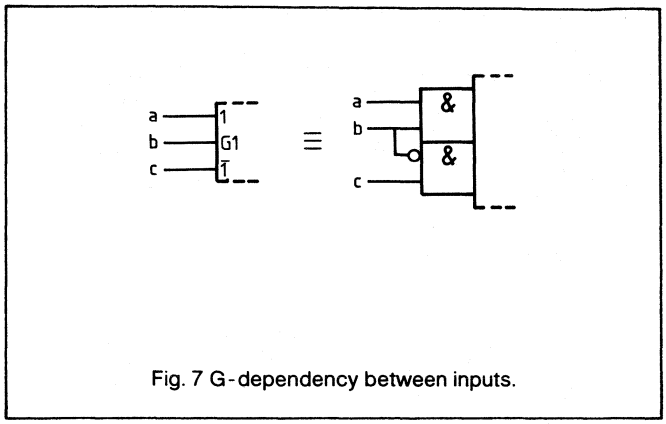


Fig. 7 G-dependency between inputs.

In Fig. 8, output "b" affects input "a" with an AND relationship. The lower example shows it is the internal logic state of "b", unaffected by the negation sign, that is ANDed.

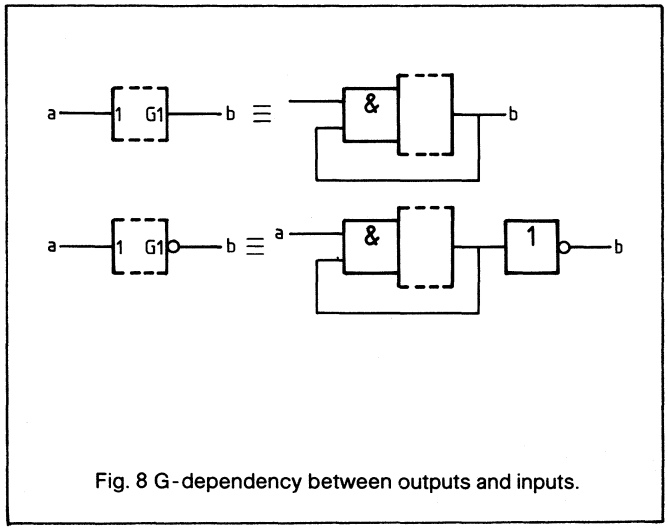


Fig. 8 G-dependency between outputs and inputs.

In Fig. 9, input "a" is ANDed with the dynamic input "b".

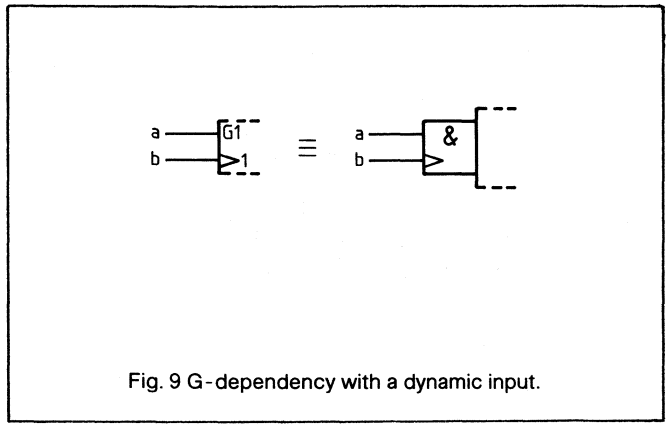


Fig. 9 G-dependency with a dynamic input.

To summarize G-dependancy using input G and allotted number m: when a Gm-input (Gm-output) is at internal logic "1", all inputs and outputs affected by Gm will be at their normally defined internal logic states. When the Gm-input (Gm-output) is at internal logic "0", all inputs and outputs affected will be at internal logic "0".

V-dependency

When a Vm-input (Vm-output) is at internal logic "1", all inputs and outputs affected by Vm will be at internal logic "1". When the Vm-input (Vm-output) is at internal logic "0", all inputs and outputs affected by Vm will be at their normally defined internal logic states (see Fig. 10).

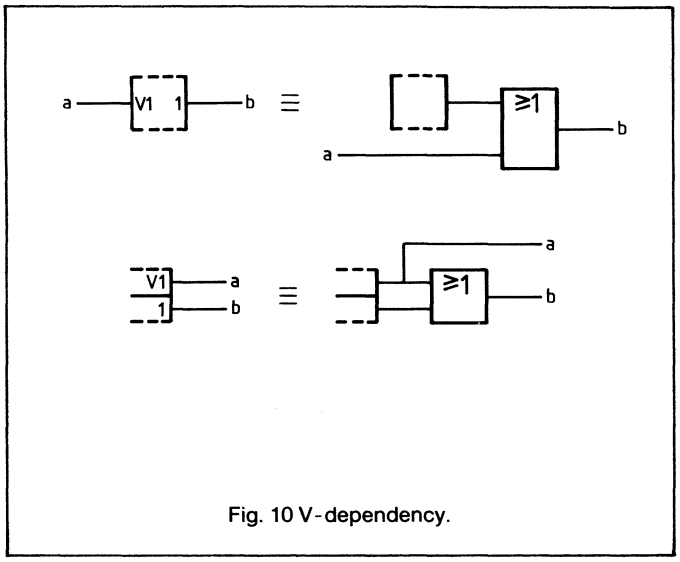


Fig. 10 V-dependency.

N-dependency

Each input or output affected by an Nm-input (or output) is EXCLUSIVE-ORed with the Nm-input (or output) (see Fig. 11).

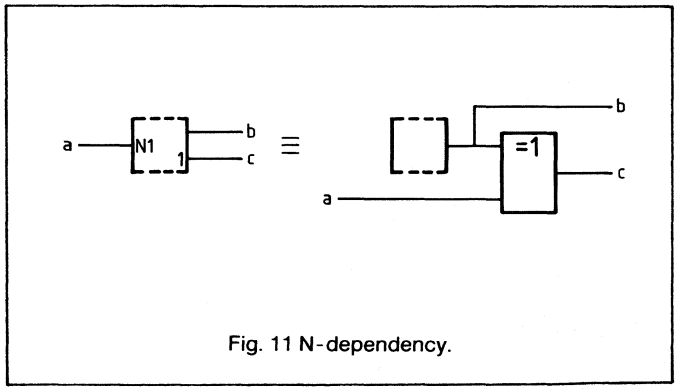


Fig. 11 N-dependency.

When an Nm-input (Nm-output) is at internal logic "1", the internal logic state of each input and each output affected by Nm will be complemented. When an Nm-input (Nm-output) is at internal logic "0", all inputs and outputs affected by Nm will be at their normally defined internal logic states.

DEPENDENCY NOTATION (continued)

Z-dependency

Interconnection dependency is used to indicate internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

All inputs or outputs affected by a Zm-input (or output) will take on the same internal logic state as the Zm-input (or output), unless modified by additional dependency notation (see Fig. 12).

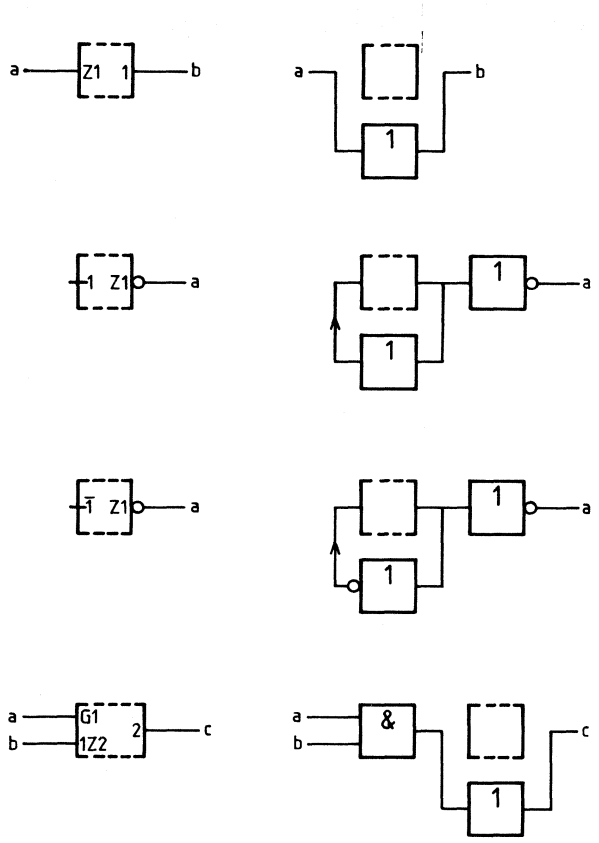


Fig. 12 Z-dependency.

C-dependency

Control inputs enable or disable the data (D, J, K, R or S) inputs of storage elements (see Fig. 13).

When a Cm-input is at internal logic "1", the inputs affected by Cm have their normal effect on the function of the element, i.e. these inputs are enabled. When a Cm-input is at internal logic "0", the inputs affected by Cm are disabled and have no effect on the function of the element.

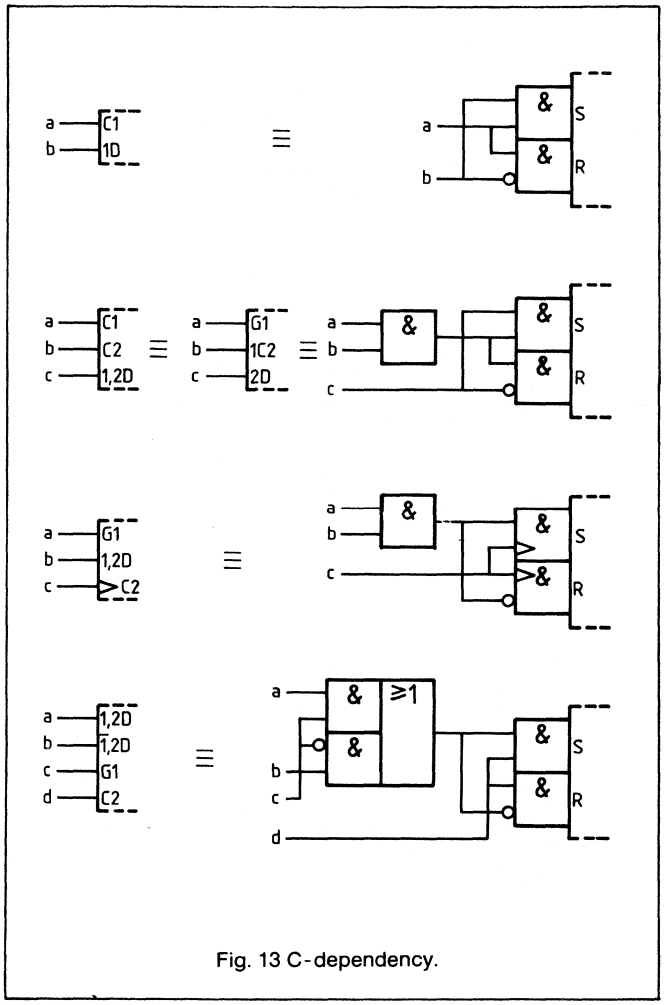


Fig. 13 C-dependency.

EN-dependency

An ENm-input has the same effect on outputs as an EN-input (see Table 1) but it affects both inputs and outputs that have the identifying number "m", whereas an EN-input affects all outputs and no inputs.

The effect of an ENm- input on an affected input is identical to that of a Cm- input (see Fig. 14).

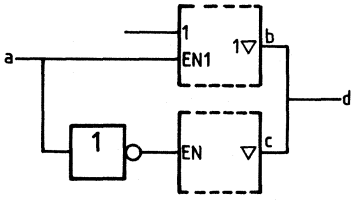


Fig. 14 EN-dependency.

When an ENm-input is at internal logic "1", inputs and outputs affected by ENm are enabled.

When an ENm-input is at internal logic "0": inputs and outputs affected by ENm are disabled; open outputs are turned OFF; passive pull-up outputs will be high-impedance "L" level; passive pull-down outputs will be high-impedance "H" level; 3-state outputs will have their normally defined internal logic states but externally exhibit high-impedance; and all other outputs (e.g., totem-pole outputs) will be at internal logic "0".

S and R-dependencies

Set and reset dependencies are used if the effect of the combination R = S = 1 on a bistable element must be specified. Figure 15a does not use S or R-dependency (? = not specified).

When an Sm-input is at internal logic "1", outputs affected by the Sm-input will react, regardless of the state of an R-input, as they would normally react to the combination S = 1, R = 0 (see Fig. 15b).

When an Rm-input is at internal logic "1", outputs affected by the Rm-input will react, regardless of the state of an S-input, as they would normally react to the combination S = 0, R = 1 (see Fig. 15c).

The non-complementary output patterns in Figs 15d and 15e are only pseudo-stable. The simultaneous return of the inputs to S = R = O produces an unforeseeable stable and complementary output pattern.

When an Sm or Rm input is an internal logic "0", it has no effect.

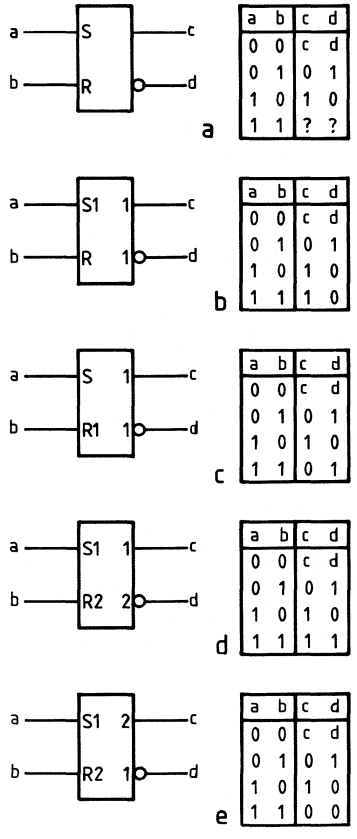


Fig. 15 S and R-dependencies.

M-dependency

Mode dependency indicates that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

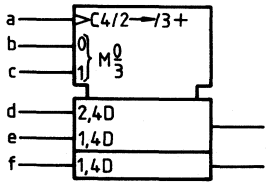
If an input or output has the same affect in different modes of operation, the identifying numbers of the relevant affecting Mm-inputs will appear in parentheses, separated by solidi, in the label of that affecting input or output (see Fig. 20).

M-dependency affecting inputs

When an Mm-input (Mm-output) is at internal logic "1", the inputs affected by this Mm-input (Mm-output) will be enabled.

When an Mm-input (Mm-output) is at internal logic "0", the inputs affected by this Mm-input (Mm-output) will be dis- abled. When an affecting input has several sets of labels separated by solidi (e.g., C4/2►/3+), any set in which the identifying number of the Mm-input (Mm-output) appears has no effect and is to be ignored. This represents the disabling of some of the functions of a multi-function input.

The circuit in Fig. 16 has two inputs, "b" and "c", these control the one of four modes (0, 1, 2 or 3) that will exist at any time. Inputs "d", "e", and "f" are D-inputs subject to dynamic control (clocking) by the "a" input. The numbers 1 and 2 identify the operating modes, and so inputs "e" and "f" are only enabled in mode 1 (for parallel loading) and input "d" is only enabled in mode 2 (for serial loading). Input "a" has three functions: it is the clock for entering data; in mode 2 it causes right-shifting of data (shifts away from the control block); and in mode 3, it causes the contents of the register to be incremented by one.



All operations are synchronous.

Mode 0 (b = 0; c = 0):
The outputs remain at their existing states as the inputs have no effect.

Mode 1 (b = 1, c = 0):
Parallel loading takes place through inputs "e" and "f".

Mode 2 (b = 0, c = 1):
Shifting down and serial loading takes place through input "d".

Mode 3 (b = c = 1):
Counting up takes place in increments of 1 per clock pulse.

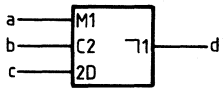
Fig. 16 M-dependency affecting inputs.

DEPENDENCY NOTATION (continued)

M-dependency affecting outputs

When an Mm-input (Mm-output) is at internal logic "1", the affected outputs will be enabled.

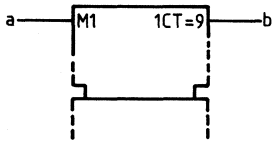
When an Mm-input (Mm-output) is at internal logic "0", the affected outputs will be disabled. When an input or output has several different sets of labels separated by solidi (e.g., 2,4/3,5), any set in which the identifing number of the Mm-input (Mm-output) appears is to be ignored.



Mode 1 (a = 1):
The delayed output symbol is effective only in mode 1 and therefore the device functions as a pulse-triggered D-element.

Mode 2 (a = 0):
The delayed output symbol has no effect and therefore the device functions as a transparent latch.

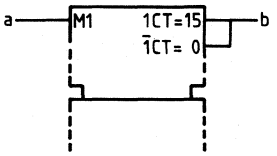
Fig. 17 Flip-flop type determined by mode.



Mode 1 (a = 1):
Output "b" will be an internal logic "1" only when the register content equals 9.

Mode 2 (a = 0):
Since output "b" is located in the common-control block with no defined function outside of mode 1, this output will be an internal logic "0" when input "a" is an internal logic "0", regardless of the register content.

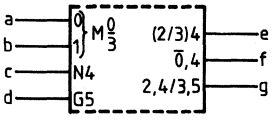
Fig. 18 Disabling an output of the common-control block.



Mode 1 (a = 1):
Output "b" will be an internal logic "1" only when the register content equals 15.

Mode 2 (a = 0):
Input "a" is an internal logic "0", output "b" will be an internal logic "1" only when the register content equals 0.

Fig. 19 Determining an output's function.



Inputs "a" and "b" are binary weighted to generate the numbers 0, 1, 2 or 3 to determine which of the four modes exist.

Mode 0 (a = 0, b = 0):
Since no output label contains a "0", the outputs have their normally defined internal logic states. Output "f" carries a "0-" in its label and this means that output "f" is effected by all modes **except** mode 0.

Mode 1 (a = 1, b = 0):
Only output "f" is affected by mode 1 and is also affected by input "c" (N4).

Mode 2 (a = 0, b = 1):
The outputs "e" and "g" are affected in this mode. They are also affected by input "c" (N4) which means that the internal logic state of the output will be negated at N4 = 1. Output "f" is affected since M0 stands at its internal "0" state. In addition, output "f" is affected by input "c" (N4).

Mode 3 (a = 1, b = 1):
All outputs shown are affected in this mode, with outputs "e" and "f" also affected by input "c" (N4) and input "d" also affecting output "g".

Fig. 20 Dependent relationships affected by mode.

A-dependency

Using address-dependency gives a clear representation of elements, particularly memories, that use address control inputs to select sections of a multi-dimensional array. Such a section of a memory array is usually called a word. Address-dependency allows a symbolic representation of an entire array. An array input at a particular element of a general section is common to the corresponding elements of all selected sections of the array. An array output at a particular element of a general section is the result of ORing the outputs of the corresponding elements of selected sections. If the label of an array output at a particular element of a general section indicates that this output is an open-circuit or a 3-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any input have their normal effect on all sections of the array, whereas inputs affected by an address input only have their normal effect on the section selected by that address input.

An affecting address input has the label "A" followed by an identifying number which corresponds to the address of the particular section of the array selected by this input. Within the general section represented by the symbol, inputs and outputs affected by an "Am" input have the label "A", which stands for the identifying numbers, i.e. the addresses of the particular sections.

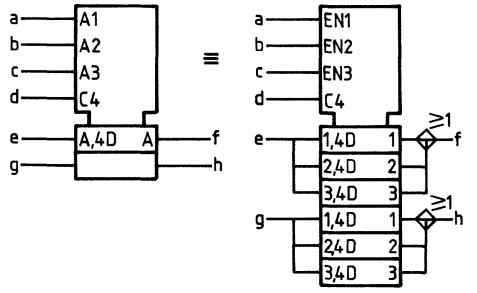


Fig. 21 A-dependency.

Figure 21 shows a 3-word x 2-bit memory having a separate address line for each word; EN-dependency is used to explain the operation. To select word 1, input "a" is forced to logic "1", entering mode 1. Data can now be clocked into the inputs marked "1,4D". Data cannot be clocked into the inputs marked "2,4D" and "3,4D" unless words 2 and 3 are selected. The outputs will be the OR function of the selected outputs, i.e. only those enabled by the active EN functions.

The identifying numbers of affecting inputs correspond to the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, ..), because in the general section represented by the symbol they are replaced by the letter "A".

If there are several sets of affecting "Am" inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter "A" is modified to 1A, 2A, ... These sets of "A" inputs may have the same identifying numbers.

Another illustration of the concept is shown in Fig. 22.

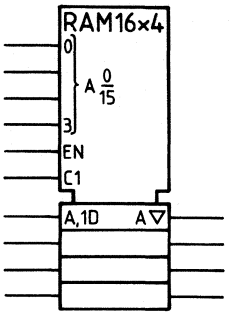


Fig. 22 Array of 15 sections of four transparent latches with 3-state outputs comprising a 16-word x 4-bit random-access memory.

Table 4 Summary of dependency notation

type of dependency	letter-symbol*	affecting input at logic "1"	affecting input at logic "0"
address	A	permits action (address selected)	prevents action (address not selected)
control	C	permits action	prevents action
enable	EN	permits action	prevents action of inputs; open outputs OFF; ▽ outputs at external high impedance, no change in internal logic state; ◈ outputs high impedance "H" level; ◈ outputs high impedance "L" level; other outputs at internal "0" state
AND	G	permits action	imposes "0" state
mode	M	permits action (mode selected)	prevents action (mode not selected)
negate (EXCLUSIVE OR)	N	complements state	no effect
reset	R	affected output reacts as it would to S = "0", R = "1"	no effect
set	S	affected output reacts as it would to S = "1", R = "0"	no effect

DEPENDENCY NOTATION (continued)

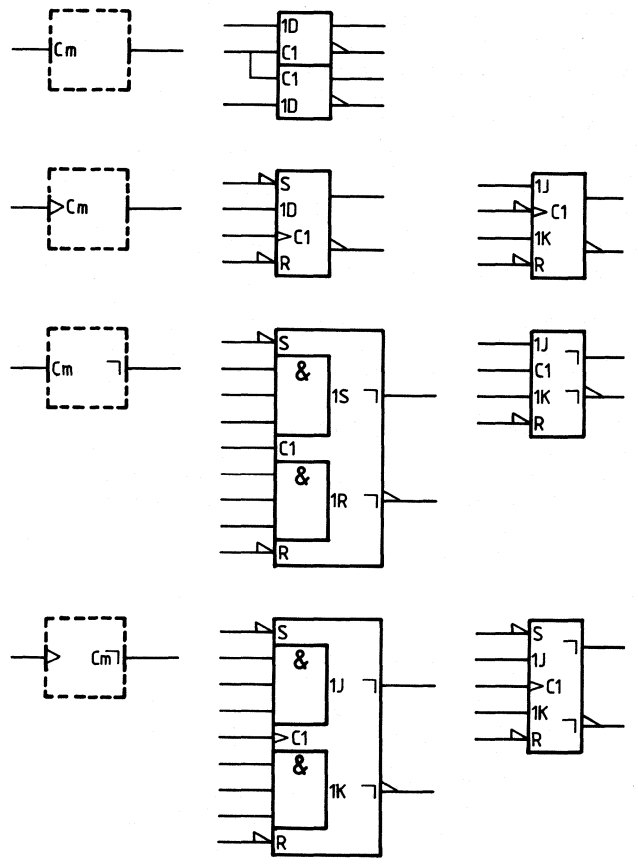
A-dependency (continued)

type of dependency	letter-symbol*	affecting input at logic "1"	affecting input at logic "0"
OR	V	imposes "1" state	permits action
inter-connection	Z	imposes "1" state	permits action

* These letter symbols appear at the **affecting** input (or output) and are followed by a number. Each input (or output) **affected** by that input is labelled with that same number. The descriptions do not apply when the labels "EN", "R" and "S" appear at inputs without numbers following; the action of these inputs is described in 'Symbols inside the outline'.

BISTABLE ELEMENTS

The dynamic input symbol, the delayed output symbol and dependency notation allow the four main types of bistable elements to be shown and make synchronous and asynchronous inputs easily recognizable (see Fig. 23). A fifth type of bistable, the direct acting "SR" element, is mentioned in 'S and R-dependencies'.



The left-hand column of drawings shows essential distinguishing features of the bistables; the other columns show examples.

Fig. 23 Four types of bistable circuits.

Transparent latches have a level-operated control input. The D-input is active as long as the C-input is at internal logic "1". The outputs respond immediately. Edge-triggered elements accept data from "D", "J", "K", "R" or "S" inputs on the active transition of "C". Pulse-triggered elements require the data to be set up before the start of the control pulse; the "C" input is considered static since the data must be maintained as long as "C" is at logic "1". The output is delayed until "C" returns to logic "0". The data- lock-out element is similar to the pulse-triggered version except that the "C" input is considered to be dynamic, in that shortly after "C" goes through its active transition, the data inputs are disabled and data does not have to be maintained. However the output is still delayed until the "C" input returns to its initial external level.

Note that synchronous inputs can be recognized easily because of labels (1D, 1J, 1K, 1S, 2R) unlike the asynchronous inputs "S", "R", which are not dependent on the "C" inputs.

CODERS

The general symbol for a coder or code-converter is shown in Fig. 24. The labels "X" and "Y" may be replaced by appropriate indications of the code that is used to represent the information at the respective inputs and outputs.

Fig. 24 Coder general symbol.

Indication of code conversion is based on the following rule:

Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

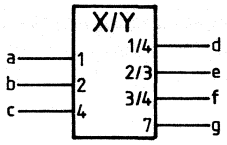
The relationship between the internal logic states of the inputs and the internal value is indicated by:

Labelling the inputs with numbers so that the internal value equals the sum of the weights associated with those inputs that are at internal logic "1"; or by replacing "X" by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationship between the internal value and the internal logic states of the outputs is indicated by:

Labelling each output with a list of numbers representing those internal values that force that output to an internal logic "1". The numbers are separated by solidi (see Fig. 25). This labelling may also be applied when "Y" is replaced by a letter denoting a type of dependency (see 'Use of a coder to produce affecting inputs'). If a continuous range of internal values produces the internal logic "1" at an output, this is indicated by the numbers that begin and end the range, separated by three dots, e.g. "4...9" equals "4/5/6/7/8/9"; or by replacing "Y" with an appropriate indication of the output code and labelling the outputs with characters that refer to this code (see Fig. 26).

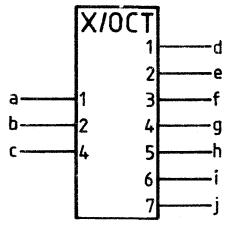
Alternatively the general symbol may be used together with an appropriate reference to a table detailing the relationship between the inputs and outputs. This is a recommended way to symbolize a ROM, or a PROM after it has been programmed.



TRUTH TABLE

inputs			outputs			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Fig. 25 An X/Y code converter.



TRUTH TABLE

inputs			outputs						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Fig. 26 An X/octal code converter.

USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case the symbols for a coder can be used as an embedded symbol (see Fig. 27).

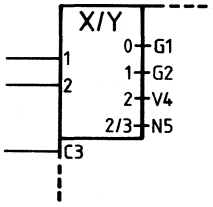


Fig. 27 Producing various types of dependencies.

If all affecting inputs produced by a coder are the same type and their identifying numbers correspond with the numbers shown at the coder outputs, "Y" (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. In this case, affecting input indications should be omitted (see Fig. 28).

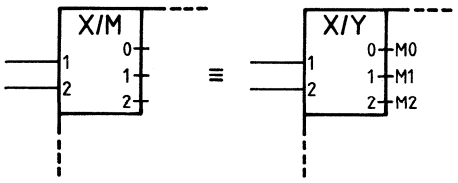


Fig. 28 Producing one type of dependency.

USE OF BIT-GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are the same type and have consecutive identifying numbers (not necessarily corresponding to the numbers that would have been shown at the outputs of the coder) the bit-grouping symbol can be used (see Table 1). Effectively, "k" external lines generate 2^k internal inputs. The bracket precedes the letter denoting the type of dependency which is followed by $^{m1}/_{m2}$. The "m1" is then replaced by the smallest identifying number and "m2" by the largest (see Fig. 29).

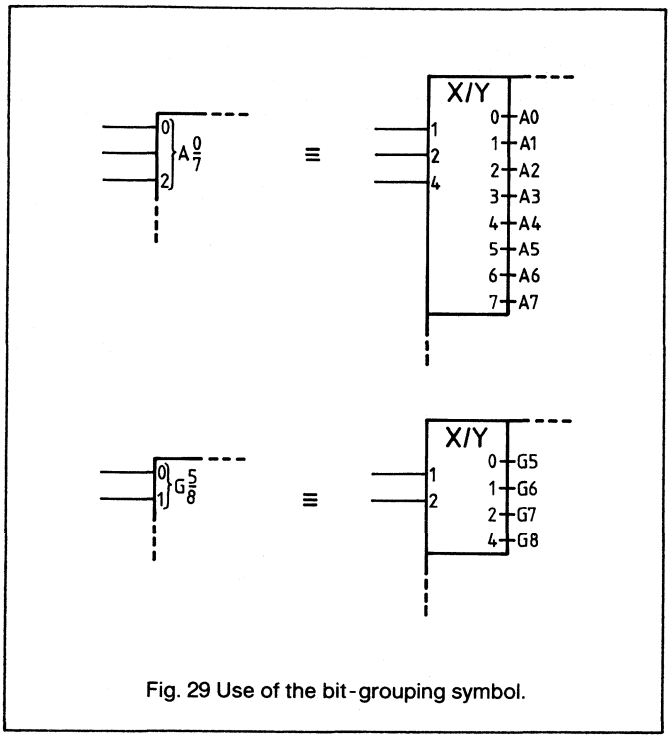


Fig. 29 Use of the bit-grouping symbol.

SEQUENCE OF INPUT LABELS

If an input having a single function is affected by other inputs, the qualifying-symbol (if there is one) for that function is preceded by the labels of the affecting inputs. The left-to-right order of these labels is the sequence in which the effects or modifications must be applied. The affected input has no effect on the element if the logic state of any of the affecting inputs (regardless of the logic states of other affecting inputs) would cause the affected input to have no effect.

If an input has several functions or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of representation is undesirable. In these cases, the input may be shown once with the different sets of labels separated by solidi (see Fig. 30). No meaning is attached to the order of these sets of labels. If one of the functions of an input is as an unlabelled input to an element, a solidus will precede the first set of labels.

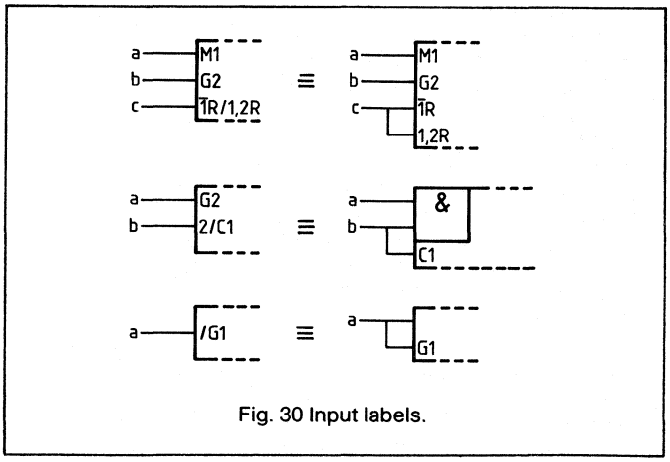


Fig. 30 Input labels.

If all inputs of a combinative element are disabled (have no effect on the function of the element), the internal logic states of the element outputs are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

Labels may be factorized using algebraic techniques (see Fig. 31).

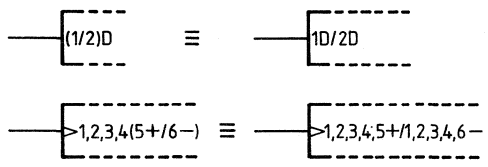


Fig. 31 Factorizing input labels.

When at latched inputs the algebraic factorizing technique is combined with the use of the bit-grouping symbol, the indication "mD" may be placed behind the bit-grouping symbol provided that the proper order of all the other labels is maintained (see Fig. 32).

In "mD", the "m" stands for the identifying numbers of the affecting inputs.

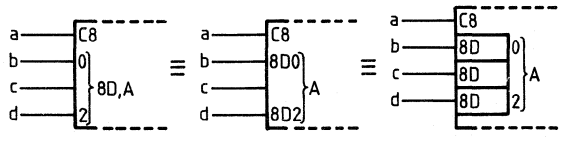


Fig. 32 Algebraic factorizing technique combined with the bit-grouping symbol at "D" inputs.

SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether or not they are identifying numbers of affecting inputs or outputs, these labels are shown in the following order (see Fig. 33):

the delayed output symbol comes first (if to be shown) preceded if necessary by the indications of the inputs to which it must be applied;

followed by the labels indicating modifications to the internal logic state of the output, such that the left-to-right order of these labels is the sequence in which their effects must be applied;

followed by the label indicating the effect of the output on the inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside boundary of the element adjacent to the output line.

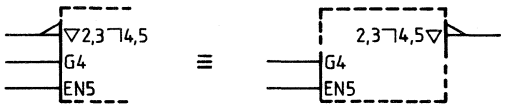


Fig. 33 Placement of 3-state symbols and delayed output symbols.

If an output needs several sets of labels to represent alternative functions, depending on the mode of action, these sets may be shown on different output lines connected together outside the outline. However, there are cases in which this representation is undesirable. In these cases the output may be shown once with the different sets of labels separated by solidi (see Fig. 34).

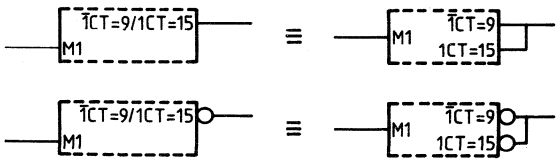


Fig. 34 Output labels.

SEQUENCE OF OUTPUT LABELS (continued)

Adjacent identifying numbers of affecting inputs that are not separated by a non-numeric character are separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting "Mm" input at internal logic "0", this set of labels has no effect on the output.

Labels may be factorized using algebraic techniques (see Fig. 35).

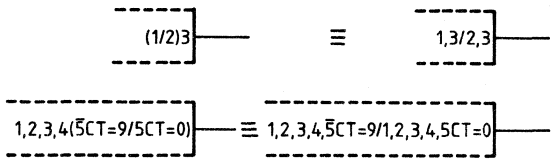


Fig. 35 Factorizing output labels.

If the bit-grouping symbol for outputs is used and the sets of labels of all outputs grouped together differ only in the indications of the weights, the sets of labels may be shown only once between the symbol replacing "*" and the grouping symbol (see Table 3) provided that, except for the grouping symbol and the weights, the proper order of the labels is maintained (see Fig. 36). These sets of labels, therefore, include the symbols for open-circuit, passive pull-down, passive pull-up and 3-state outputs but exclude the indications of weights.

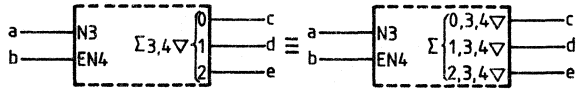


Fig. 36 The bit-grouping symbol at outputs.

RULES FOR SIMPLIFICATION OF SYMBOLS

INTRODUCTION

The IEC symbology can depict a complete integrated circuit but, in many applications, not all available functions are used. For these applications the complete symbol need not be shown and a considerable simplification can be made. To maintain clarity, rules for the simplification of symbols are described in this section.

RULE 1

For an integrated circuit where not all functions are used, the diagram may contain:

a. the complete symbol with indications of which pins are connected to a certain voltage level;

b. a simplified symbol where only the functions used are depicted; the unused pins are detailed in a table including information on whether these pins may remain open (floating) or are to be connected to a certain voltage level.

RULE 2

When two or more pins are shown with a single line, then a comma between the pin numbers means that these pins are connected together; when the pin numbers are separated by a solidus, this means they are separate functions.

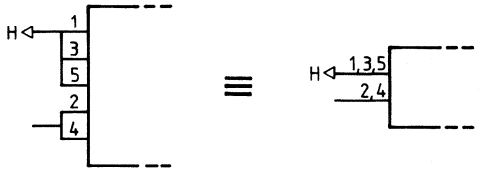
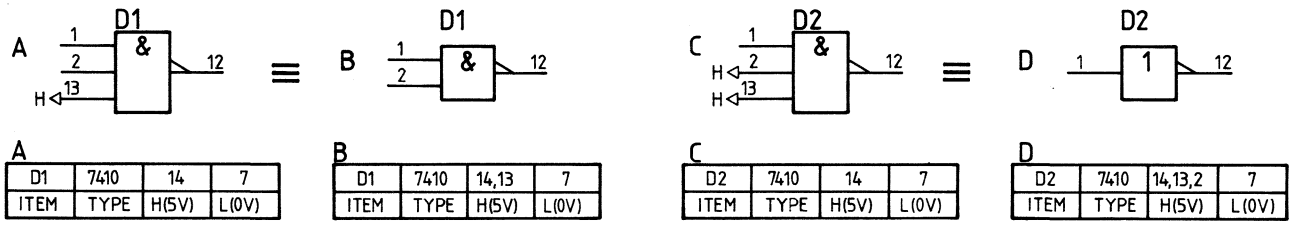


Fig. 38 Example of Rule 2.



A

D1	7410	14	7
ITEM	TYPE	H(5V)	L(0V)

B

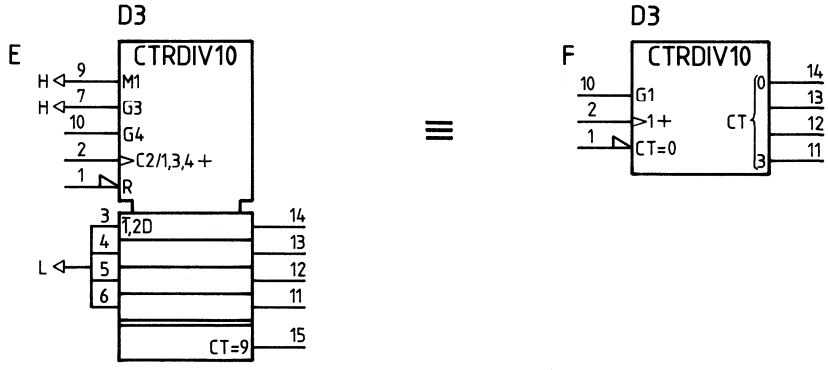
D1	7410	14,13	7
ITEM	TYPE	H(5V)	L(0V)

C

D2	7410	14	7
ITEM	TYPE	H(5V)	L(0V)

D

D2	7410	14,13,2	7
ITEM	TYPE	H(5V)	L(0V)



E

D3	74LS160	16	8
ITEM	TYPE	H (5V)	L(0V)

F

D3	74LS160	16,7,9	8,3,4,5,6	15
ITEM	TYPE	H(5V)	L (0V)	NU

NU=NOT USED

Fig. 37 Examples of Rule 1.

RULE 3

The rules for sets of labels at inputs and outputs using solidi to separate the various parts of a label may be applied when drawing two or more pins with a single line, so the labels must also be joined.

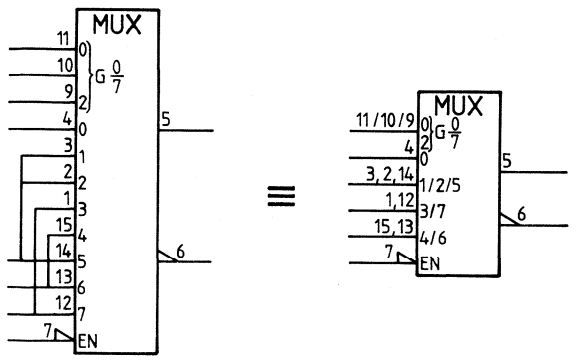


Fig. 39 Example of Rule 3 showing "74151" 8-input multiplexer.

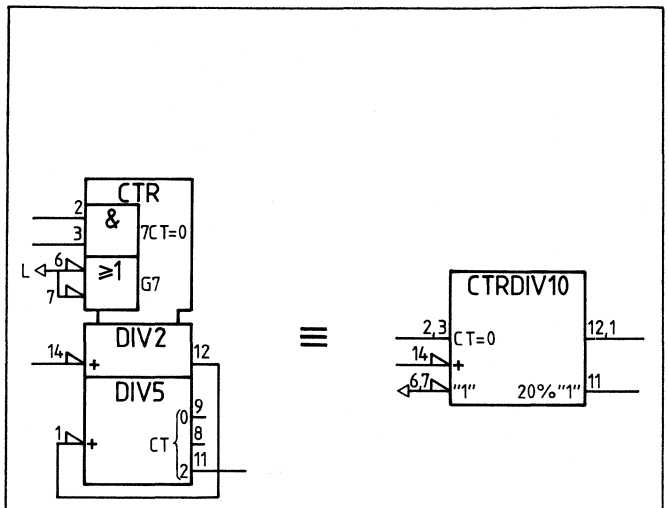


Fig. 41 Example of Rule 4 using TTL "7490".

RULE 4

An output can be connected to an input of equal polarity as shown in Fig. 40C. If the polarity is different this method does not give sufficient information and the methods of Fig.40A or B are then adopted.

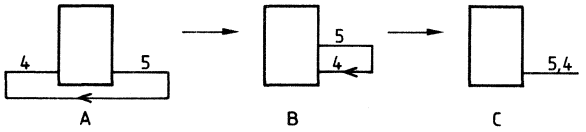


Fig. 40 Examples of Rule 4.

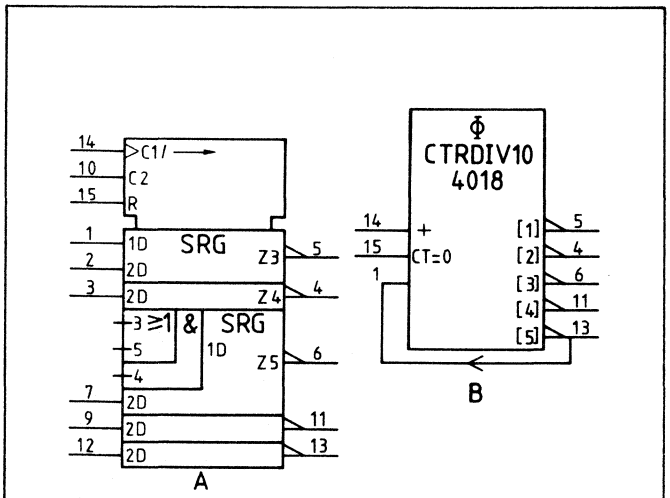


Fig. 42 Example of Rule 4 using CMOS "4018"; the full symbol shown in (A) can be reduced to that of (B) when no parallel loading is applied and the device is used as a divide-by-10 circuit.

RULE 5

Combining elements together to form one element is allowed only if all pin numbers can be shown.

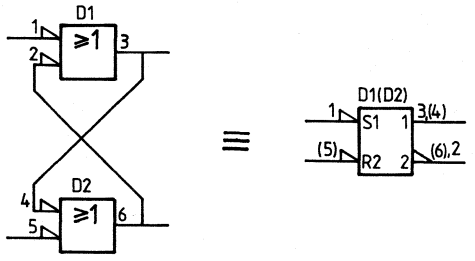


Fig. 43 Example of Rule 5; the pin numbers between parentheses indicate that these belong to another circuit.

RULE 6

A circuit consisting of a combination of two or more elements that appear repeatedly on a diagram, may be replaced by a single symbol. This symbol is used on the diagram, while the complete circuit is shown in an auxiliary diagram elsewhere on the drawing.

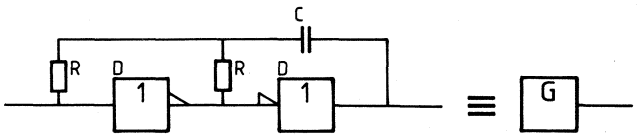


Fig. 44 Example of Rule 6.

RULE 7

A multiple symbol may also be applied for logic symbols.

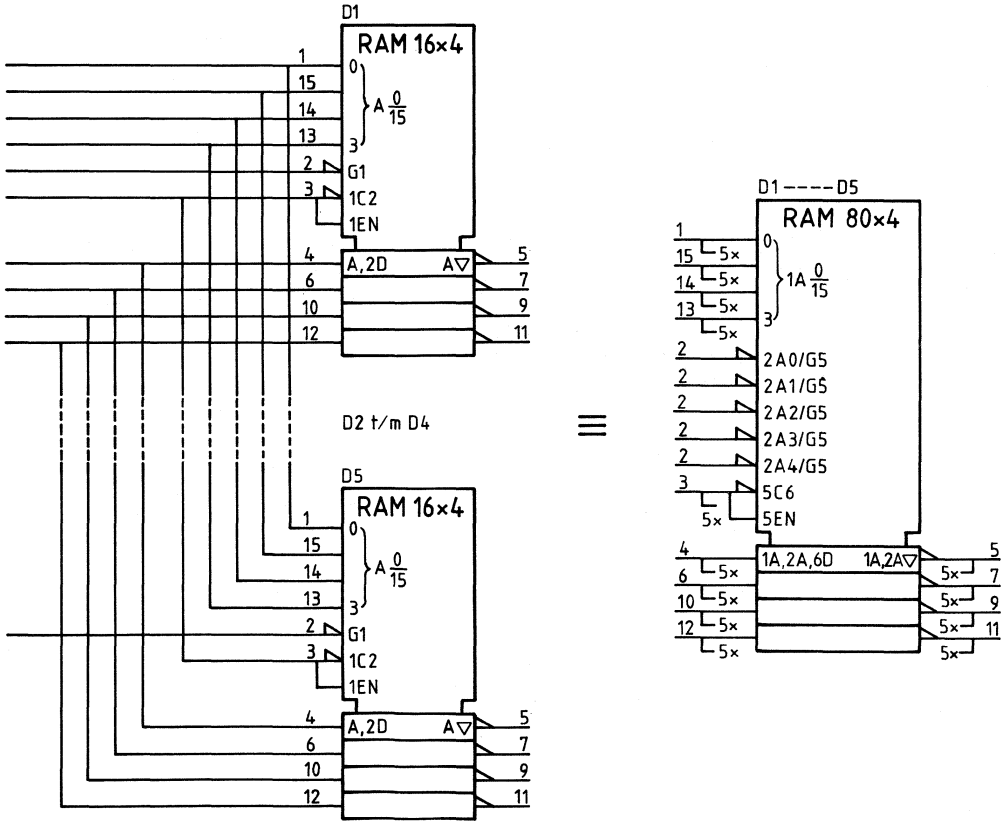


Fig. 45 Example of a multiple symbol showing five TTL "74189" 16x4-bit RAMs connected to enlarge the number of words.

RULE 7 (continued)

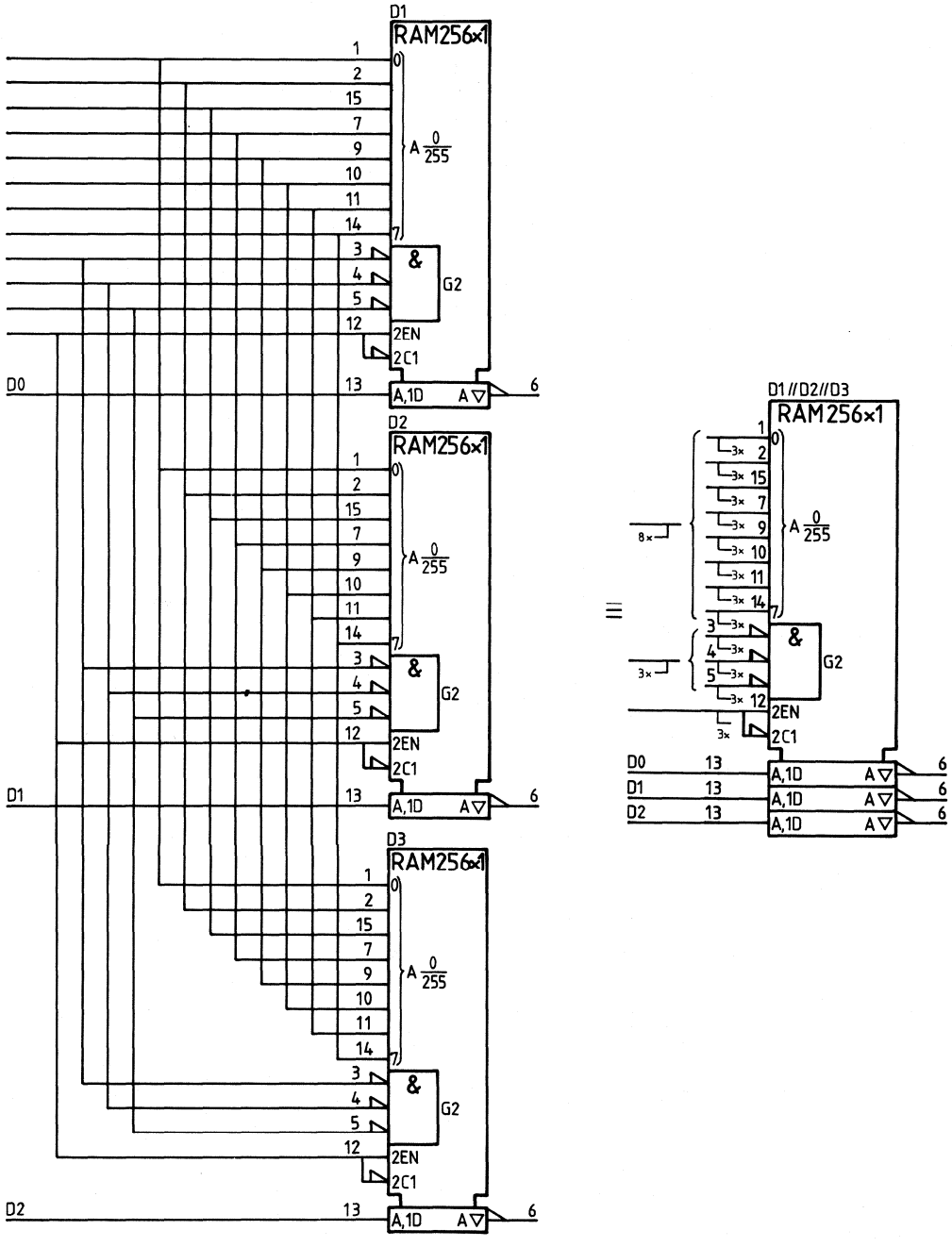


Fig. 46 Example of a multiple symbol showing three TTL "74201" 256x1-bit RAMs connected to lengthen the word.

RULE 8

Every (P)ROM may be regarded as an X/Y-code-converter.

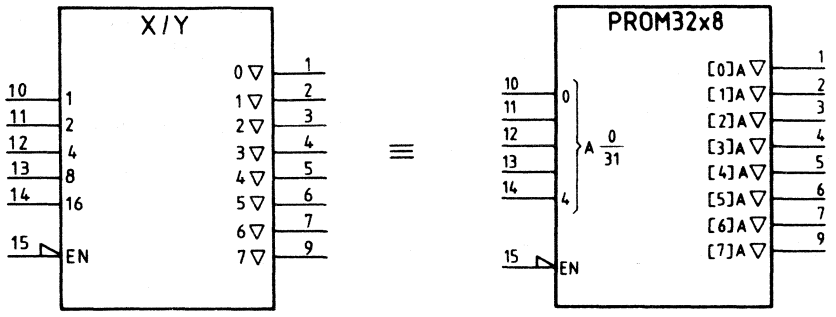
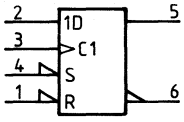


Fig. 47 Example of Rule 8 using Schottky TTL "74S288" PROM.

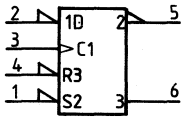
EXAMPLES OF APPLICATION-DEPENDENCY OF SYMBOLS

A symbol depicts the function of an element. In the case of multi-function elements, the functions are depicted separately.

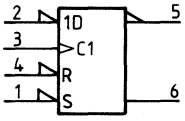
To demonstrate application-dependency of symbols, Fig. 48 shows the basic symbol and eight applications of the "7474" D-element with "S" and "R" inputs.



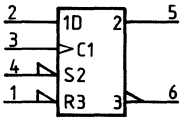
(A) basic symbol



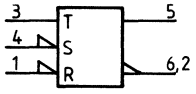
(B) as for (A) but with "R" and "S" dependency



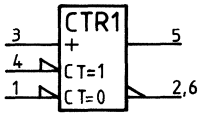
(C) D-input ("L")
(note change of "R" and "S")



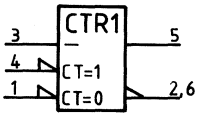
(D) as for (B) but with "S" and "R" dependency



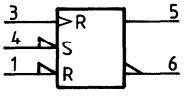
(E) divide-by-2 ("T") element



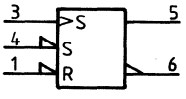
(F) divide-by-2 as a limit case of CTR



(G) as for (F) with down-counter



(H) function at pin 2 = "L", or as indicated in a table



(I) function at pin 2 = "H", or as indicated in a table

Fig. 48 Example of application-dependent symols for edge-triggered D-element with "R" and "S" inputs.

APPLICATION INFORMATION

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Power supply decoupling 811

Interfacing HCMOS 813

Power dissipation 821

Oscillator design 829

User edge protection 835

Handling CMOS devices 837

POWER SUPPLY LINE LAYOUT AND DECOUPLING RECOMMENDATIONS

Peak-current in output stages during switching and the charging and discharging of parasitic capacitance are the two main sources of noise on power lines. And so, to minimize noise generation the power supply should be decoupled. However, where switching speed is high, not only the voltage dips on the power lines must be considered but also the effects of di/dt radiation. In decoupling, a balance between these two phenomena must be achieved.

Before decoupling can provide any noise reduction, there must first be a good power distribution network. Ground (GND) connection is vital and so a good connection pattern is required. But even the commonly used ground pattern as shown in Fig. 1 can cause problems.

In this figure, an output from device 1 drives an input to device 2, and an output from device 3 drives an input to device 4. Since the signal paths 1 to 2 and 3 to 4 are not coupled there should be no crosstalk. However, device 1 and 3 share the hatched part of the GND line, and switching the output of device 1 could produce a spike on the GND of device 3, causing the input to device 4 to switch. It is therefore advisable to reduce the single ground path on a double-sided board by using links as shown in Fig. 2. This is especially true for boards where high currents are switched.

Avoid using jumpers for GND and power line (V_{CC}) connections (Fig. 3). Jumpers are unlikely to be used in production printed-circuit boards, but they should also be avoided on prototype and single boards because the inductance they introduce into the lines permits coupling between outputs. Therefore, printed circuit boards with premanufactured GND connections or copper strips to connect the pins to GND should be used.

However, an even better solution is to use multi-layer printed circuit boards where different layers can be used for the supply rails and the copper interconnections. The capacitive coupling between ground and V_{CC} is essential for high frequency noise pulse reduction. It has the distinct advantage of being free from the inductive effects of the interconnections inherent in discrete decoupling capacitors.

Even with double-sided boards it is advisable to have the V_{CC} and ground lines on opposite side of the board wherever possible. A less expensive alternative to multi- layer PCBs is the multi-wire board, offering the same high frequency noise characteristics.

No matter which type of board is used, it is recommended to have at least 5 ground pins per connector to give good ground current distribution.

The precautions taken with ground lines also apply to the V_{CC} line. Power line stability is a must - even a difference of 0.5 V between V_{CC} lines can produce unwanted effects. It is advisable to have separate power stabilization for each board, to isolate noise sources and avoid the use of a large stabilizer circuit with its heavy gauge (low impedance) wiring to each board. However, care must be taken because a fault on a board's stabilizer circuit may be transmitted via the HC/HCT input structure to other boards, possibly causing damage.

No matter how good the V_{CC} and GND connections, all line inductance effects cannot be avoided. This is where decoupling plays its part.

Ceramic capacitors are the nearest approximation to ideal decoupling capacitors since they have nearly no series inductance. But, the advantage of using inductance-free capacitors is lost if long connections to the capacitor are used. This results in a tuned LC-circuit with a very high Q factor. The oscillations produced would have a worse effect on the circuit than if there were no decoupling at all. If it is not possible to make the decoupling connections shorter than 20 mm, tracks should be placed in parallel, with a separation of at least one track-width (Fig. 4).

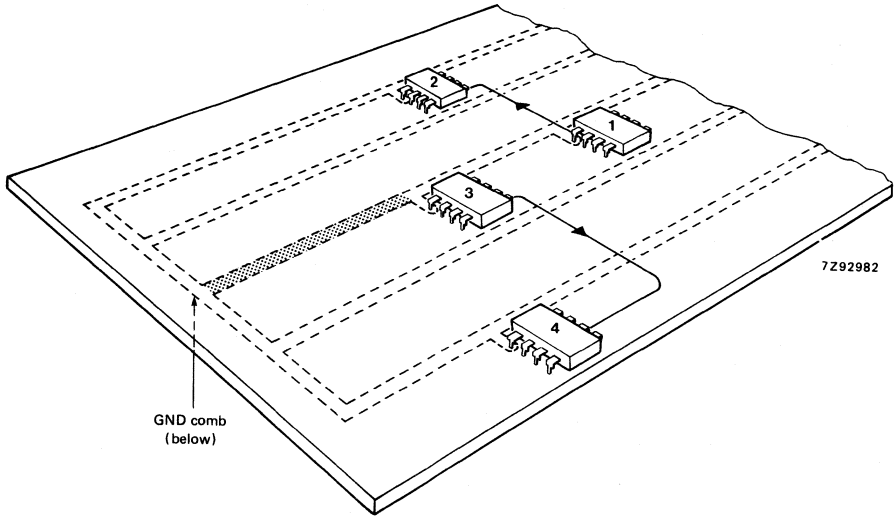


Fig. 1 Common ground path on double-sided board.

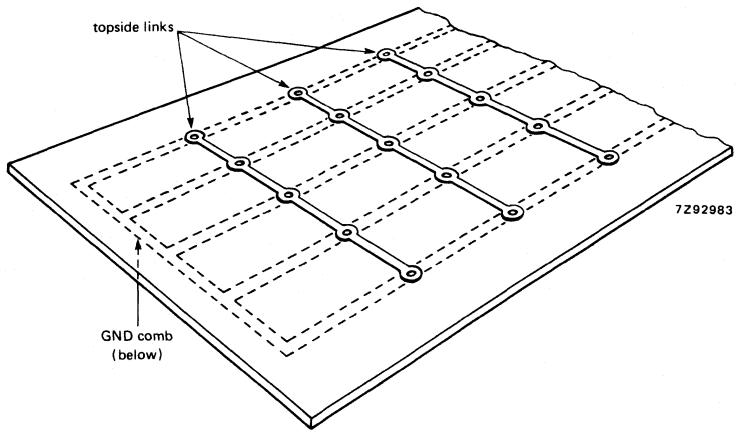


Fig. 2 Reducing ground paths on double-sided board.

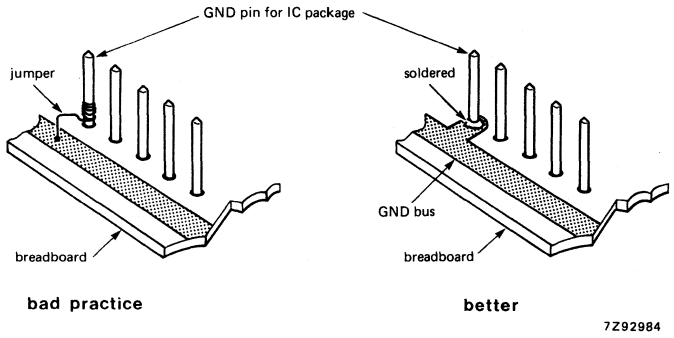


Fig. 3 Ground (GND) connection on a logic board.

Care should be taken when selecting the capacitors to be used. Many capacitors are produced with leads bent as shown in Fig. 5a, but these introduce unwanted inductance. Therefore, it is advisable to use capacitors with leads shaped as shown in Fig. 5b.

In tests a good decoupling was obtained using a minimum of:

- one 47 μF bulk capacitor per Eurocard;
- one 1 μF tantalum capacitor per 10 packages of SSI logic;
- one 22 nF ceramic capacitor for each octal circuit and for each counter/shift register (MSI logic) and;
- one 22 nF ceramic capacitor per 4 packages of SSI logic.

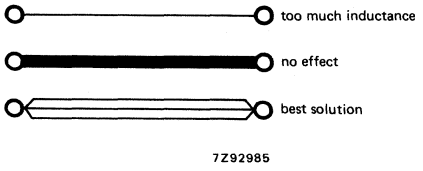


Fig. 4 Decoupling tracks.

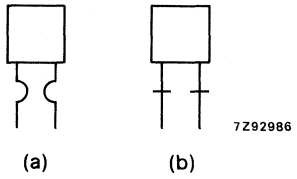


Fig. 5 Decoupling capacitors - capacitors as shown in Fig. 5a should not be used for decoupling, the best results are obtained using the capacitor as shown in Fig. 5b.

INTERFACING HCMOS CIRCUITS WITH OTHER LOGIC FAMILIES

Demands for higher speed, greater complexity and lower power dissipation in logic systems are being met by interfacing different logic technologies in the same system. These mixed technology systems must also be able to communicate with the outside world. As the input voltage requirements of conventional CMOS circuits are incompatible with TTL output levels, it's often necessary to sacrific noise margins, speed and quiescent power dissipation to achieve these interfaces between families. However, with our PC54/74HC/HCT family of high-speed CMOS (HCMOS), this is no longer so.

The HCMOS ICs are available in two versions: circuits with type number suffix HC operating with CMOS input switching levels from a 2 to 6 V supply (intended primarily as faster CMOS ICs in new designs), and devices with suffix HCT, switching at TTL input levels from a supply of 5 V ±10%. All types are fully buffered and pin- and function-compatible with most popular LSTTL ICs.

Additionally, unbuffered inverters (suffix HCU) are available for oscillators, and other feedback circuits operating in linear mode, but it's with the HC and HCT types and their interfacing with other logic families that this article is concerned. Furthermore, it will discuss the quiescent and dynamic noise immunity characteristics of HCMOS devices and compare them with those of LSTTL ICs.

HC/HCT INTERFACING TECHNIQUES

It's necessary to consider two groups of interfaces for the HC/HCT devices: interfacing with other logic families; and interfacing with non-standard peripheral levels and directly driven loads.

Due to the comparable operating speeds of HCMOS and LSTTL logic, it's the interface between these two families that will be most common, so we'll discuss these considerations at greater length. However, interfaces with other families, including the HE4000B series CMOS and ECL 10K, are also simply implemented. Table 1 summarises the solutions for the various types.

HCMOS and TTL output configurations

The typical output structure of an HCMOS IC is shown in Fig.1(a). When the output is HIGH or LOW (V_{OH} or V_{OL}), its level is very close to V_{CC} or GND respectively.

In contrast, the HIGH level output voltage for the standard TTL circuit shown in Fig.1(b) is limited by the V_{BE} of TR_1 plus the voltage drop across D_1, resulting in a maximum V_{OH} of 3,5 V at V_{CC} = 5 V. Further, if a collector current is flowing, R_1 will cause an additional voltage drop and the worst case V_{OHmin} specified for TTL is 2,4 V (at I_{OHmax}), over the full temperature and power supply range.

The LOW level output voltage for TTL is the collector/emitter saturation voltage of TR_2 (excess of base current) and so even when a source current flows from the loaded output, V_{OLmax} will not exceed 0,5 V.

Looking at the output structure for LSTTL devices in Fig.1(c), the V_{OH} is now limited by the V_{BE} of both TR_1 and TR_3 (the diode does not feature in the LSTTL output structure) and is typically 3,4 V. LSTTL specifications quote V_{OHmin} as 2,7 V over the full temperature range with V_{CCmin} = 4,75 V.

TABLE 1
Interfacing HCMOS to other logic families

		TO					
		HC 5 V supply	**HCT** 5 V supply	**HE4000B** 5 V supply	**HE4000B** 6 – 15 V supply	**TTL*** 5 V supply	**ECL 10K**
FROM	**HC** 5 V supply	direct	direct	direct	4104	direct	10124
	HCT 5 V supply	direct	direct	direct	4104	direct	10124
	HE4000B 5 V supply	direct	direct	direct	4104	direct	10124
	HE4000B 6 – 15 V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	transistor
	TTL* 5 V supply	pull-up resistor	direct	pull-up resistor	4104	direct	10124
	ECL 10K	10125	10125	10125	transistor	10124	direct

* Includes LS, S, STD, FAST, ALS and AS.

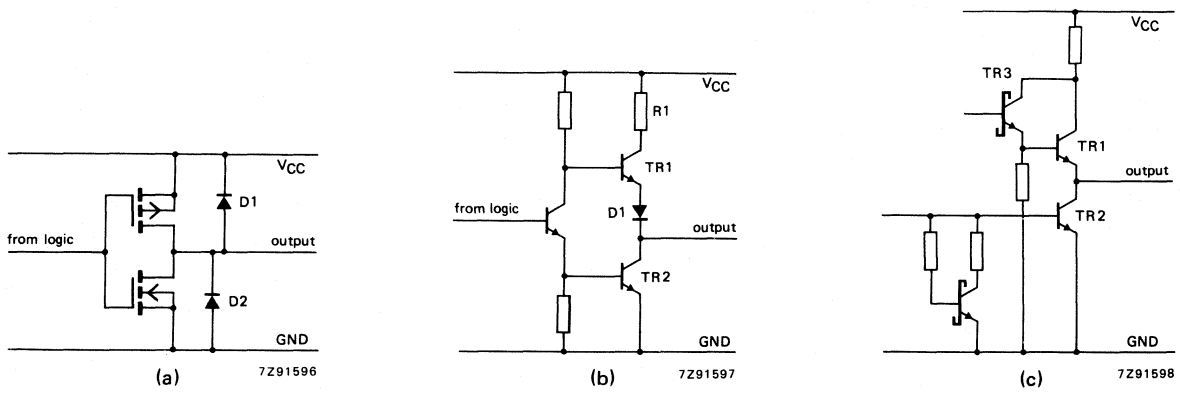


Fig. 1 Typical output configurations of : (a) HC/HCT devices—D1 and D2 are the inherent diodes of the p-drain and the n-drain respectively, (b) standerd TTL, and (c) low-power Schottky TTL (LSTTL)

HCMOS input structures

The input structure for HC devices is given in Fig.2(a). Under normal operating conditions, the input voltage should swing within the supply voltage limits V_{CC} and GND, since exceeding these limits can cause a current to flow through the input protection diodes, D_1 and D_2. The maximum d.c. current permitted through these diodes is 20 mA and if this rating is exceeded, the function of the circuit may be impaired. As the MOS transistors TR_1 and TR_2 are electrically identical, the typical logic switching of the device is $V_{CC}/2$.

The input configuration for HCT devices is basically identical to that for HC circuits but with the addition of a level shifting diode (D_3) between PMOS transistor TR_1 and V_{CC}. This is shown in Fig.2(b). The effect of D_3, combined with NMOS transistor TR_2 having a higher gain than PMOS transistor TR_1, is to reduce the input switching level typically to 1,4 V.

The advantage of diode D_3 is that it reduces power dissipation when a HIGH input from a TTL output is applied. This HIGH level can be as low as 2,4 V, and although it will be recognised as a logic "1", the PMOS transistor TR_1 would not be fully cut-off allowing a flow-through current between V_{CC} and GND. D3, and the influence of the back-gate (substrate) connection of TR_1 to V_{CC}, dramatically reduces the flow-through current, and therefore the power dissipation, in the input stage whilst yielding input switching levels compatible with LSTTL.

Interfacing LSTTL with HC/HCT

When HCT and LSTTL devices operate from the same supply, the quiescent flow-through current I_C at $V_{IH} = 2,4$ V and $V_{CC} = 4,5$ V, is close to zero. This means that the HCT input structure gives true CMOS type power dissipation,

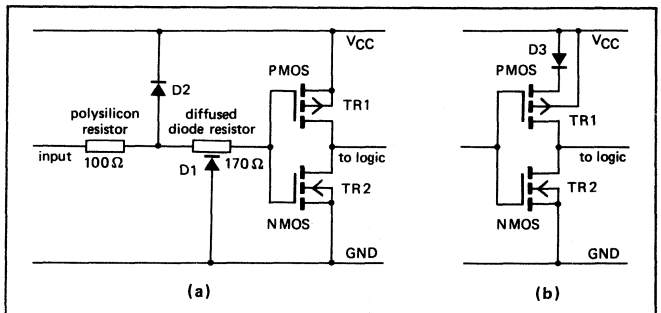


Fig. 2 Typical input structures of: (a) HC devices, and (b) HCT devices

even when driven from TTL. If V_{CC} is increased to 5,5 V, the minimum HIGH level output voltage also rises 1 V to 3,4 V.

For interfacing LSTTL with HC/HCT in a dual supply voltage system, the following worst case conditions supply:

V_{OHmin} for TTL = 2,4 V

V_{OHmin} for LSTTL = 2,7 V

and

V_{IHmin} for HC devices = 3,85 V (70% of V_{CC})

V_{IHmin} for HCT devices = 2 V

(where V_{CC} = 4,75 V for TTL and 5,5 V for HCMOS, over total temperature range).

From the above figures, it's clear that the worst-case TTL HIGH level output voltage is less than the minimum HIGH level input voltage for HC devices and an interface is required. A solution is provided in the circuit in Fig.5(a), where pull-up resistor R_1 will pull the output voltage of the LSTTL against V_{CC}. However, we don't favour this technique because the time-constant formed by the pull-up resistor and the stray capacitance (C_S) plus the load capacitance (C_L) will increase the propagation delay.

Furthermore, with this set-up the propagation time is less predictable because it relies on both active and passive RC time-constants. Although a low value for R_1 will reduce the propagation delay, it consumes extra power and reduces the noise margin LOW (due to an active load) and this conflicts with the purpose of using HCMOS. The pull-up resistor also requires board space and insertion time thus increasing production costs.

Therefore, the pull-up resistor interface should only be used if unavoidable and the practical solution is to use HCT devices (all types in the PC54/74 family are available in both HC and HCT versions). The LSTTL and HCT ICs interface directly as shown in Fig.3(b).

Driving LSTTL from HCMOS

Since the output of HCMOS devices swing between V_{CC} and GND, they are TTL input compatible and the interface is a direct connection (also shown in Fig.3(b)).

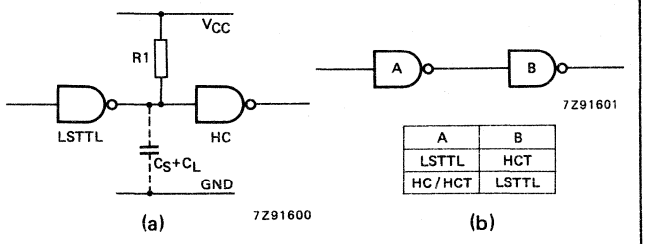


Fig. 3 Techniques for interfacing: (a) LSTTL with HC devices, and (b) LSTTL with HCT devices, and HC/HCT with LSTTL devices

When an HCT device is the driving source, the speed can be accurately predicted because the LSTTL logic switching threshold of 1,4 V is also used for HCT ICs. For HC driving sources, the speed difference introduced by the HC logic switching threshold of $V_{CC}/2$ can be calculated from the specified output transition times (from the data sheets).

Table 2 gives the driving capability (fan-out) of HC/HCT for the various TTL families.

TABLE 2
Maximum fan-out for HC/HCT driving TTL

receiving input	standard output	bus driver output
TTL	2	3
LSTTL	10	15
STTL	2	3
FAST	6	10

Interfacing HC/HCT with HE4000B series CMOS

HC/HCT devices can be coupled directly to standard HE4000B series CMOS ICs if they operate from the same supply voltage. However, if the circuits have different supply voltages, level shifting is necessary. The configuration shown in Fig.4(a) illustrates this for the HC/HCT to HE4000B interfaces using the HEF4104B LOW-to-HIGH level-shifter. Note that this IC is exclusively a LOW-to-HIGH level-shifter and care should be taken to ensure that V_{CC1} never exceeds V_{CC2} by more than one V_{BE}.

Figure 4(b) shows how to interface the HE4000B family with HC/HCT using the HEF4049B/4050B or PC74 HC4049/4050 buffer ICs. These buffers don't have an input clamping diode to V_{CC} and this means that the maximum input level is 15 V. The logic level switching threshold remains referenced to V_{CC2}, so the noise margin LOW will be as for the 5 V specification.

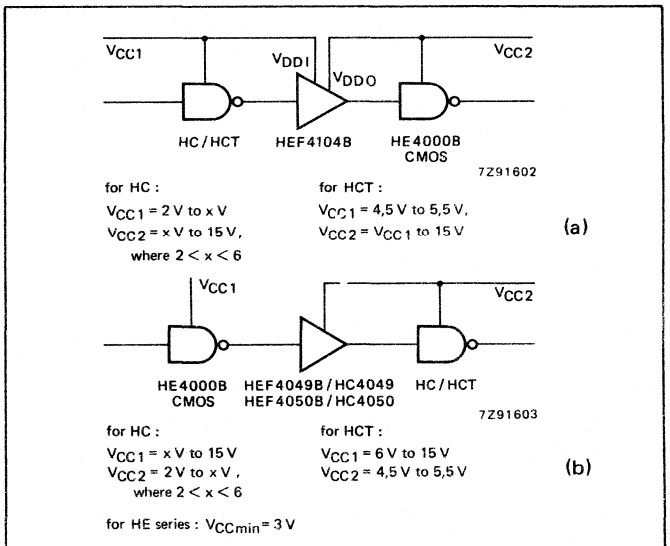


Fig. 4 Techniques for interfacing: (a) HC/HCT devices with HE4000B series CMOS, and (b) HE4000B series CMOS with HC/HCT devices

For interfacing HC/HCT devices with NMOS devices (microprocessors, memories, etc.). the rules for TTL apply since NMOS ICs generally have TTL-compatible inputs and outputs. Exceptions are NMOS ICs with open-drain outputs where a pull-up resistor must be used to load the output.

Interfacing HC/HCT with ECL 10K

To interface with ECL 10K series logic, the 10124 TTL-to-ECL and the 10125 ECL-to-TTL translator ICs (for HC/HCT-to-ECL and ECL-to-HC/HCT interfaces respectively) are used. Note that these devices operate at TTL levels. When using the 10125 for interfacing HC circuits, the pull-up resistor R_1 must be used in accordance with the instructions

for driving HC devices from TTL. The circuit configurations are shown in Figs.5(a) and 5(b).

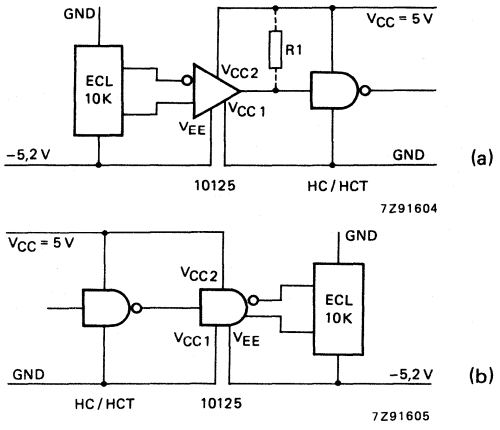


Fig. 5 Techniques for interfacing: (a) ECL 10K logic with HC/HCT circuits — R1 is only required when driving HC types, and (b) HC/HCT devices with ECL 10K logic

Interfaces with terminated buses

Buses are used chiefly in industrial applications and unfortunately, this environment imposes several restraints on microprocessor-based systems, electrical noise and battery back-up requirement being two such examples. CMOS technology provides the ideal solution to these problems, and the HC devices offer superior noise immunity, similar operating speed and lower power dissipation over a wider temperature and supply range than comparable LSTTL ICs. For the HCT range, the noise immunity is the same as for LSTTL.

Therefore, development of a new bus standard for CMOS systems should be based on the performance of the devices available with bus driver outputs, for example, the PC74/54HC245 transceiver. Figs.6(a) and 6(b) show examples of TTL and HC/HCT bus terminations respectively.

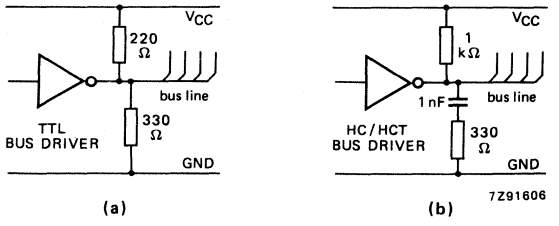


Fig. 6 Examples of bus terminations used in: (a) conventional bipolar (TTL) technologies, and (b) HC/HCT systems

Conventional buses are heavily d.c. loaded so within existing bus standards, HC/HCT bus drivers are unable to drive these loaded buses as they can only deliver an output current of 6 mA. Under these circumstances, the interface should be implemented with a suitable bus driver.

HC/HCT devices do not generally have input hysteresis so Schmitt trigger circuits should be used if slow, noisy bus rise and fall voltages call for hysteresis in the receiver. The PC54/74HC/HCT14 and 132 are two such ICs for noise tolerant systems and five devices in the flip-flop series (PC54/74HC/HCT73, 74, 107, 109 and 112) also have Schmitt triggers in the clock input.

Interfacing with non-standard levels

In many applications, PC54/74 high-speed CMOS ICs will need to interface with non-standard input and output levels, for example, with industrial or automotive systems operating from a 12 to 24 V supply. The circuits in Figs.7(a) and 7(b) show the basic design rules for these interfaces. Figure 7(c) illustrates an example of a user edge input circuit for interfacing with input levels greater than V_{CC}. The configuration for HC/HCT devices driving loads from an external power supply is given in Fig.8(a), and Figs.8(b) and 8(c) show HC/HCT devices driving loads (for example, a relay) on the same supply voltage.

NOISE IMMUNITY IN HC/HCTMOS

The noise immunity characteristics for logic devices can be divided into two categories: static and dynamic noise immunity. If we first examine the static noise immunity, this can also be divided into two further categories as follows:

- static noise immunity LOW — this is the difference between the V_{ILmax} of the receiving circuit and the V_{OLmax} from the driving circuit
- and static noise immunity HIGH — this is the difference between the V_{OHmin} from the driving circuit and the V_{IHmin} of the receiving circuit.

If we compare the guaranteed static noise immunity characteristics for LSTTL, and HC/HCTMOS, the result is as shown in Table 3.

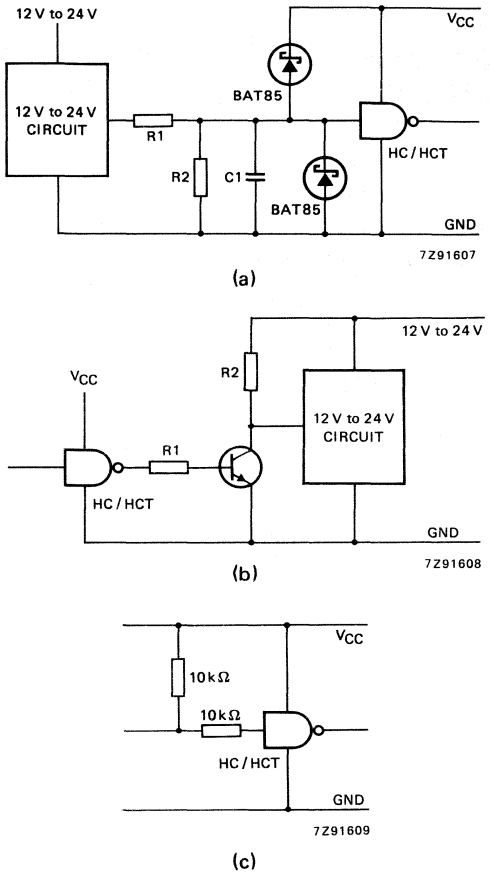


Fig. 7 Techniques for interfacing: (a) non-standard logic levels with HC/HCT circuits — values of R1 and R2 depend on the output voltage of the driving circuit and C1 depends on the noise and speed, and (b) HC/HCT devices with non-standard logic levels — values of R1 and R2 depend on supply voltage and transistor type. (c) shows a user-edge input circuit configuration for interfacing with input voltages greater than V_{CC}

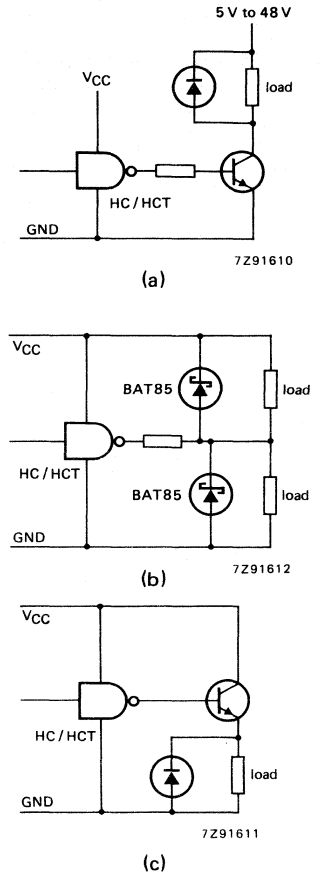


Fig. 8 Interfacing HC/HCT devices with a load on: (a) an extenal power supply via a transistor, and (b) the same power supply via a transistor. (c) shows interfacing HC/HCT directly with loads on the same power supply

TABLE 3
Static noise margins for LSTTL at V_{CC} = 4,75 V and HC/HCT systems at V_{CC} = 4,5 V

	LSTTL	HC	HCT
V_{OHmin}	2,7 V	4,4 V	4,4 V
V_{IHmin}	2,0 V	3,15 V	2,0 V
noise margin HIGH	0,7 V	1,25 V	2,4 V
V_{ILmax}	0,8 V	0,9 V	0,8 V
V_{OLmax}	0,4 V	0,1 V	0,1 V
noise margin LOW	0,4 V	0,8 V	0,7 V

TABLE 4
Ratio of static noise margins, LSTTL to HC/HCT

	LSTTL	HC	HCT
noise margin HIGH	1	1,75	3,4
noise margin LOW	1	2	1,75
ambient temperature range T_{amb}	0 to +70 °C	−40 to +85 °C	−40 to +85 °C
supply voltage V_{CC}	4,75 V	4,5 V	4,5 V

If we now take the static noise margins for LSTTL to be unity, (for both the HIGH and LOW states) a direct comparison can be made by taking the ratio of LSTTL to HC/HCT static noise margins as shown in Table 4. These results are particularly impressive when considering the extended ambient temperature range of the HC/HCT and the lower supply voltage.

The graph in Fig.9(a) compares the static noise margins for HC devices with those for LSTTL. This illustrates that whilst HC circuits can drive LSTTL (as V_{OHmin} for HC > V_{IHmin} for LSTTL), the converse is not true (since V_{OHmin} for LSTTL < V_{OHmin} for HC – there is no overlap on the noise margin HIGH regions). Therefore, the noise margin HIGH for LSTTL driving HC devices is said to be negative which explains the reason for the pull-up resistor interface described in Fig.3(a).

In a mixed technology system with fully loaded HCT outputs driving LSTTL inputs, the static noise margin LOW is equal for both families, and the HCT devices exhibit an excellent static noise margin HIGH that encompasses that displayed by LSTTL. This is illustrated by the graph in Fig.9(b) and shows that HCT and LSTTL devices are fully interchangeable.

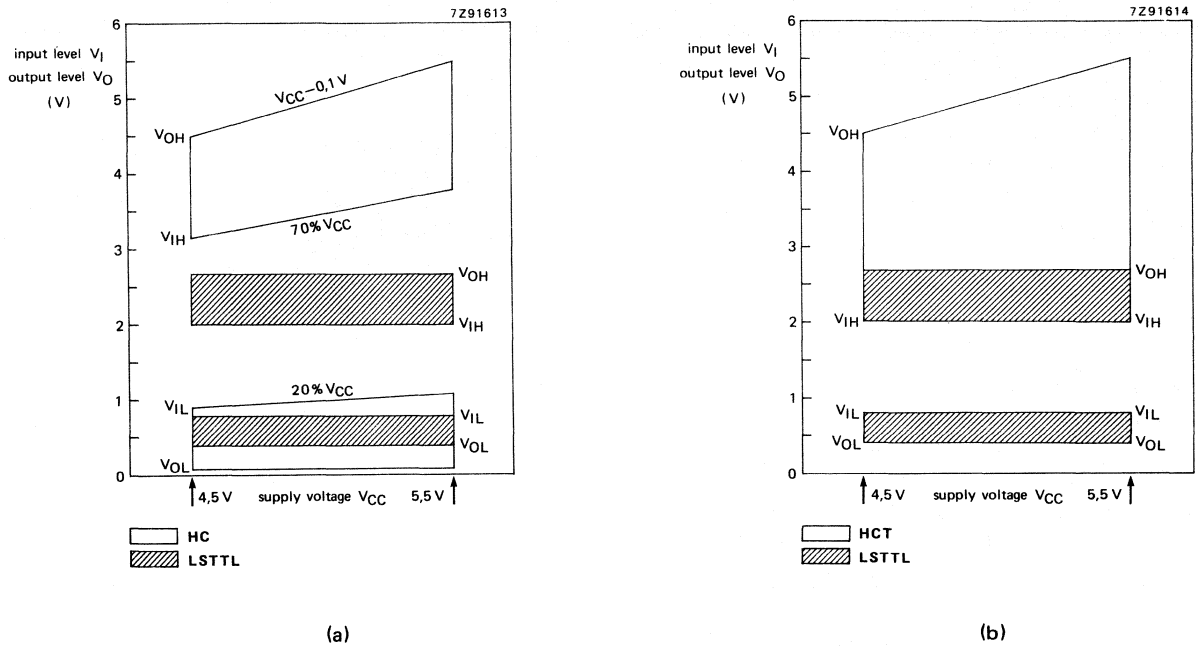


Fig. 9 Static noise margins for: (a) HC devices compared with LSTTL, and (b) HCT devices compared with LSTTL in a mixed technology system

DYNAMIC NOISE IMMUNITY

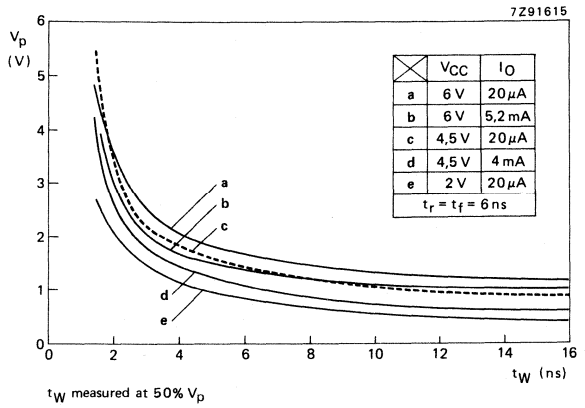
As for static noise immunity, dynamic noise immunity for HC/HCT circuits falls into two catagories, HIGH and LOW. The dynamic noise margin LOW is again the smaller of the two, so it is this parameter that we'll consider here.

To plot the dynamic noise immunity LOW for HC/HCT devices, a pulse of known magnitude V_p is applied to the input of a device and its width (t_W) is increased until the device just begins to switch. The input level on which V_p is based is equal to the switching voltage minus the worst-case static noise margin LOW. Pulse width (t_W) is measured at half pulse height ($V_p/2$) and the rise and fall times (t_r and t_f) are 0,6 ns.

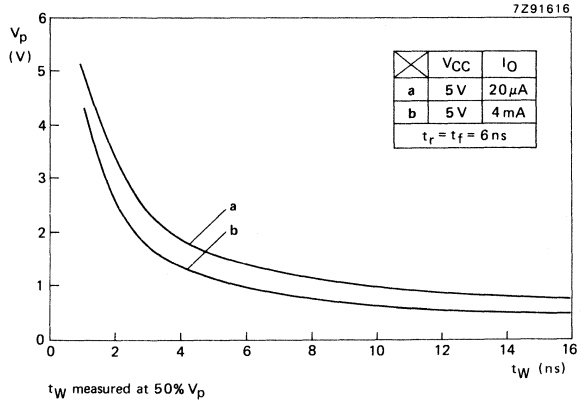
The V_p is then reduced in increments and the t_W for each new value assertained. The test is repeated over a series of varying supply voltages, V_{CC} (between 2 and 6 V for HC and at 5 V for HCT), and output current, I_O.

The resulting graphs in Figs.10(a) and 10(b) illustrate the dynamic noise immunity characteristics of HC and HCT circuits respectively. Note that increasing I_O, lowers the curve and therefore reduces the dynamic noise immunity. As these curves illustrate the worst-case conditions with fully loaded HC/HCT devices, a system of only HC or HCT circuits will demonstrate an increase in dynamic noise immunity, shifting the curves up 0,3 V.

Derived from the typical input switching threshold levels of 1,3 V and 2,5 V for HC and HCT respectively, the noise immunity characteristics will show a typical improvement of 0,8 V in HCT systems and 1,2 V in HC systems.



(a)



(b)

Fig. 10 Dynamic noise immunity characteristics (worst-case, fully loaded driver) for: (a) HC devices and (b) HCT devices

CONSIDERATIONS OF POWER DISSIPATION

Our PC54/74HC/HCT high-speed CMOS (HCMOS) family of logic ICs have the short propagation delays (high speed), formerly only attainable with TTL logic elements, combined with the much lower quiescent power dissipation which is an inherent feature of CMOS circuits. Furthermore, PC54/74 circuits with an HCT suffix also have TTL input switching levels, operate from a 5 V ±10% supply, and are pin-compatible with the most popular LSTTL circuits which they are intended to replace.

For LSTTL circuits operating below about 10 MHz, the most significant part of the total power dissipation is the quiescent power dissipation due to the many bipolar transistors that continuously conduct. With HCMOS circuits however, the converse is true because quiescent power dissipation is only due to leakage currents through reverse-biased junctions and is so low that it's practically negligible compared with the frequency-dependent dynamic power dissipation.

Since the logic functions in most systems only change state during brief periods, the average system frequency is between one or two orders of magnitude lower than the system clock frequency and the ICs therefore only draw quiescent current for most of the time. This means that replacing LSTTL circuits with equivalent HCT circuits, with their much lower quiescent power dissipation, results in a very significant reduction of overall system power dissipation without loss of operating speed.

However, total system power dissipation, is the sum of both the quiescent and the dynamic power dissipation of all the ICs and must be determined and minimised during system design. For LSTTL, where the quiescent power dissipation is the most significant contributor to the total power dissipation, the total power dissipation can be simply derived from the product of V_{CC} and I_{CC} given in the data sheets. For HCMOS circuits however, the dynamic power dissipation which is the most significant part of the total power dissipation is influenced by circuit design. It can't be simply read from the data sheets but must be calculated from the supply voltage, average switching frequency, load capacitance, internal capacitances of the IC, and transient switching currents.

This article explains how our method of specifying HCMOS devices in the data sheets makes it very simple to calculate the quiescent, dynamic and total power dissipation of HCMOS logic circuits.

QUIESCENT POWER DISSIPATION

Quiescent power is dissipated by a device when it is not switching and $V_I = V_{CC}$ or ground. Figure 1(a) will be used to illustrate this power dissipation in HCMOS devices. In the quiescent state, either the PMOS or the NMOS transistor is fully off, and, in theory, no direct MOS transistor channel path exists between V_{CC} and ground. In practice however, thermally generated minority charge-carriers, which are present in all reverse-biased diode junctions, allow a very small leakage current to flow between V_{CC} and ground. This quiescent supply current (I_{CC}) is specified in the published data.

Three factors influence the value of I_{CC}, and therefore the quiescent power dissipation, for a particular device. They are:

Temperature:

increasing temperature causes I_{CC} to increase because the minority charge-carriers in the reverse-biased diode junctions are thermally generated

Device Complexity:

MSI devices dissipate more power than SSI devices because they have a proportionally greater reverse-biased diode junction area.

Supply voltage:

the number of minority charge-carriers is linearly related to reverse junction voltage.

Table 1 shows the JEDEC industry standard for the worst-case I_{CC} in PC54/74HC/HCT high-speed CMOS devices. It shows the effect of temperature and device complexity on I_{CC} at the maximum recommended HC supply voltage $V_{CC} = 6$ V. I_{CC} can be linearly derated for other supply voltages and would be approximately one-third of the value in Table 1 for $V_{CC} = 2$ V. Typical I_{CC} values are well below the maximum specified values.

Another factor which influences quiescent power dissipation is a steady-state input voltage level which may slightly turn-on one of the input transistors shown in Fig.1(a) and yet not fully turn-off the other. This causes a small additional quiescent supply current (I_C) to flow between V_{CC} and ground. The level of I_C depends on the size of the input transistors and is different for each device.

In a system consisting entirely of HC circuits, the additional quiescent supply current I_C is so small that it can be omitted from practical power dissipation calculations. This is because HC I/O levels are fully compatible. The worst-case output levels with $|I_O| = 20\,\mu A$ are $V_O = 0{,}1$ V max. and $V_{OH} = V_{CC} - 0{,}1$ V min., very close to ground and V_{CC} respectively. Figure 2(a) shows that I_C is negligible when these levels are applied to HC inputs because they always turn one of the input transistors fully off.

However, if HC device input levels are held close to the switching threshold (typically $V_{CC}/2$), Fig.2 shows that the additional quiescent supply current I_C becomes much greater than quiescent supply current I_{CC}. This occurs if

the mistake is made of driving an HC input from a TTL output. With a minimum TTL V_{OH} of 2,4 V driving an HC input, not only will a logic "1" probably not be recognized, but several milliamps of I_C will flow. To overcome this problem, an external pull-up resistor could be used as shown in Fig.3 but the resistor would dissipate significant power because its value would have to be low to maintain switching speed. HCT devices have TTL input switching levels and should therefore be used instead of HC devices whenever it is necessary to interface HCMOS with TTL logic.

Unlike HC devices, HCT devices can be substituted for LSTTL devices and/or mixed with LSTTL, ALSTTL, ASTTL or FAST-TTL family ICs in the same system. Under some conditions, they may dissipate somewhat more quiescent power than HC devices. For example, Fig.2(b) shows that a worst-case TTL V_{OL} of 0,5 V max. is close enough to ground to turn the input NMOS transistor fully off so that I_C is close to zero. However, a worst-case TTL V_{OH} of 2,4 V min. causes some I_C to flow. For this reason, HCT data sheets specify I_C at the worst-case input voltage of $V_{CC} - 2{,}1$ V for V_{CC} ranging from 4,5 V to 5,5 V. It is further specified on a per input pin basis to allow more accurate power dissipation calculations if all the functions within an IC are not being used, or are being driven by different input voltage levels.

Our proprietary HCT input structure shown in Fig.1(c) considerably reduces the additional quiescent supply current I_C. The structure is identical to that for HC circuits except for a level-shifting diode between the PMOS transistor and V_{CC}, and the connection of the substrate of the CMOS transistor to V_{CC}. The effect is to reduce the input level switching threshold to 1,4 V instead of $V_{CC}/2$ as is the case with HC circuits. This therefore reduces the additional quiescent current I_{CC} when a TTL minimum HIGH level of 2,4 V is applied to an HCT input by ensuring that the PMOS transistor is fully turned off. Figure 2(b) shows that I_C is negligible when an HCT input is held at a typical TTL HIGH output level (3,4 V) or LOW output level (0,25 V).

Calculating HC quiescent power dissipation

For power-critical applications such as battery-powered equipment, it may be necessary to calculate HC quiescent power dissipation as a standby value of battery drain. It is given by:

$$P_{QHC} = V_{CC} I_{CC} \qquad (1)$$

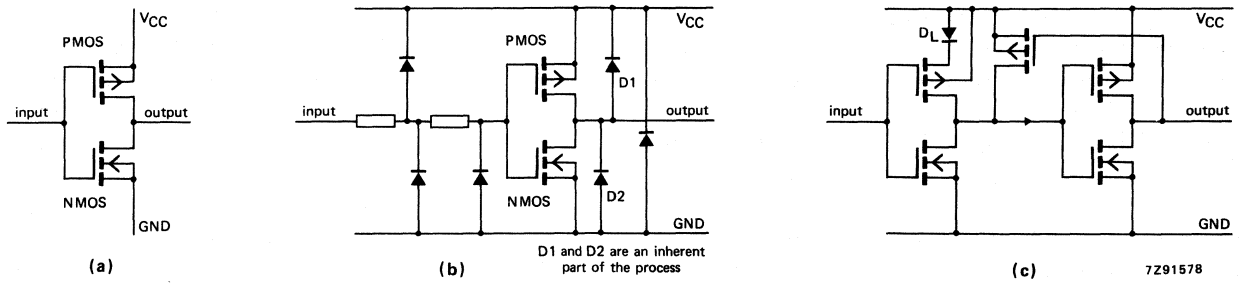


Fig. 1 HC inverter, (a) input structure of HC inverter; (b) HC inverter with protection circuitry; (c) input structure of HCT inverter

TABLE 1

JEDEC industry standard for d.c. characteristics of HCMOS circuits

DC characteristics for 54/74HC/HCT

symbol	parameter	T_{amb} (°C) 54/74HC/HCT +25 min.	typ.	max.	74HC/HCT −40 to +85 min.	max.	54HC/HCT −55 to +125 min.	max.	unit	test conditions V_{CC} V *	V_I	other
	quiescent supply current											
I_{CC}	SSI	–	–	2,0		20,0	–	40,0	μA	5,5	V_{CC}	$I_O = 0$
I_{CC}	flip-flops	–	–	4,0		40,0	–	80,0	μA	5,5	or	$I_O = 0$
I_{CC}	MSI	–	–	8,0		80,0	–	160,0	μA	5,5	GND	$I_O = 0$

* for HC, V_{CC} = 6 V.

V_{CC} is dependent upon the particular application, we recommend that a ±10% variation be allowed. I_{CC} at V_{CC} = 6 V is obtained from the data sheet for the particular device. For critical battery-powered applications, the value of I_{CC} at V_{CC} = 6 V can be linearly derated for any desired V_{CC}; for example, at V_{CC} = 2 V, use one-third of the limits shown in Table 1.

Calculating HCT quiescent power dissipation

Assume that an LSTTL device with an output duty factor of 0,5 is switching one of the inputs to one of the gates in a PC54HCT11 (triple 3-input AND gate) with a 5 V supply and an ambient temperature of 25 °C. Quiescent power dissipation is calculated from:

$$P_{QHCT} = V_{CC}(I_{CC} + \delta I_C) \qquad (2)$$

where δ = switching duty factor.

$I_{C\,max}$ is calculated on a unit-load basis from the part of the data sheet reproduced in Table 2:

$I_{C\,max}$ = 275 μA per pin × 1 pin × 0,5 unit-load = 136 μA

Inserting this current and the values for V_{CC} (5,5 V), I_{CC} = 2 μA from Table 2, and δ (0,5) into equation (2) gives:

$$P_{QHCT} = 5{,}5\ V[2\ \mu A + (0{,}5 \times 136\ \mu A)] = 385\ \mu W.$$

This is only 1,5% of the 25,5 mW maximum quiescent power that would be dissipated by the equivalent LSTTL device. Furthermore, as previously stated, the I_C of 275 μA per input pin quoted in Table 2 for the HCT device is based on a worst-case HIGH input level of V_{CC} − 2,1 V. In a typical application, the TTL HIGH input level driving the device would be much higher than this, resulting in a reduction of I_C by an order of magnitude.

If all the inputs of an HCT device are driven by HC or equivalent CMOS outputs, the input levels are such that the additional quiescent supply current I_C is so small that it can be omitted from HCT power dissipation calculations. HC quiescent power dissipation equation (1) can then be used to calculate HCT quiescent power dissipation.

DYNAMIC POWER DISSIPATION

Unlike quiescent power dissipation, dynamic power dissipation is calculated in the same manner for both HC and HCT devices. All equations presented here for dynamic power dissipation are therefore applicable to both HC and HCT devices.

Three factors influence the dynamic power dissipation of HCMOS devices. They are load capacitance, internal capacitance and switching transient currents (through-currents of transistor pairs when both transistors momentarily conduct during logic level transitions).

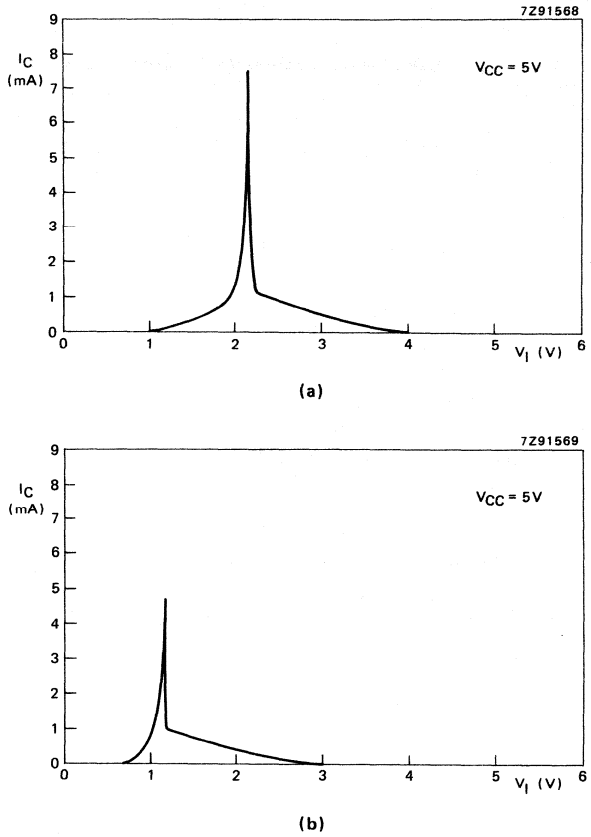


Fig. 2 Supply current as a function of input voltage at V_{CC}=5 V.
(a) PC54/74HC86 quad two-input exclusive-OR gate;
(b) PC54/74HCT86 quad two-input exclusive-OR gate

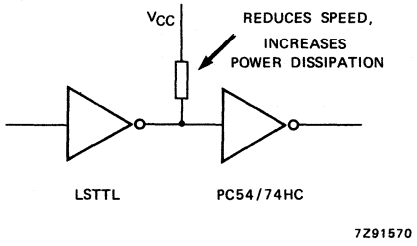


Fig. 3 Using a pull-up resister to interfase HC circuits with LSTTL

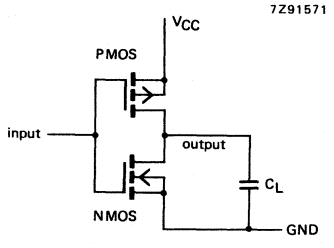


Fig. 4 HC inverter driving a capacitive load

TABLE 2
Specification of I_{CC}, I_C and unit load coefficient for PC54/74HCT11 triple 3-input AND gate

symbol	parameter	T_{amb} (°C) 54/74HCT +25 min.	typ.	max.	74HCT −40 to +85 min.	max.	54HCT −55 to +125 min.	max.	unit	test conditions V_{CC} V	V_I	other
I_{CC}	quiescent supply current			2,0		20,0		40,0	μA	5,5	V_{CC} or GND	$I_O = 0$
I_C	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	275		375		425	μA	4,5 to 5,5	V_{CC} −2,1 V	other inputs ar V_{CC} or GND: $I_O = 0$

Note:

1. The additional quiescent supply current per input is determined by the I_C unit load, which has to be multiplied by the unit load coefficient as given in the table below.

input	unit load coefficient
nA, nB, nC	0,5

Load capacitance

The first contribution to dynamic power dissipation is caused by the charging and discharging of external capacitive loads. Figure 4 illustrates an HCMOS inverter circuit with a capacitive load and, together with the following equations, will help to illustrate how load capacitance consumes power. The energy dissipated (joules) in charging and discharging the capacitive load is:

$$P_{CL}T = C_L V_{CC}^2 \quad (3)$$

where $T = 1/f_o$ and C_L = total external load capacitance due to interconnections, driven inputs and any sockets that are used.

The dynamic power dissipation due to capacitive loads is therefore:

$$P_{CL} = C_L V_{CC}^2 f_o \quad (4)$$

Equation (4) is only applicable if all the outputs are switching the same load. If they are not, the equation becomes:

$$P_{CL} = \Sigma(C_L V_{CC}^2 f_o) \quad (5)$$

For multiple output devices, it is important to calculate with the appropriate output frequency. For example, at either output from a flip-flop, $f_o = f_i/2$; for a 6-stage binary ripple counter (type PC54/74HC/HCT4024), f_o is halved for each successive output stage so that $f_o = f_i/64$ for the final output stage.

Internal capacitance

All ICs have internal parasitic capacitance caused by diode junctions, MOS transistor structures, and the aluminimum and polysilicon interconnections. It has the same effect as external capacitive loads, and its magnitude depends on the complexity of the device.

HCMOS devices are manufactured with a self-aligned polysilicon gate process (3 μm gate length) and local oxidation to reduce internal capacitance by minimising gate-to-source and gate-to-drain capacitances. The junction capacitances, which are proportional to junction area, are smaller than those in HE4000B CMOS devices because the diffusions are shallower. Figure 5 shows the location of the capacitances in an HC inverter.

For power dissipation calculation purposes, the total load caused by internal capacitances and by switching transient currents is defined as a single effective internal no-load power dissipation capacitance C_{PD}. It is defined in the data sheet for each HCMOS device on a 'per function' basis and, where appropriate, it is also separately specified for each different logic function (e.g. gate or flip-flop) within a device. This allows more accurate power dissipation calculations to made if logic functions within the same device are operating at different frequencies.

The published figure for C_{PD} is valid for the worst-case operating mode under typical operating conditions. For example, in the case of a NAND gate, the state of the inputs is assumed to be such that the output is changing state; for a shift register or D-type flip-flop, it is assumed that alternately HIGH/LOW data is being clocked in. The specified value for C_{PD} however is a typical one; nevertheless, some protection will already be built-in to dynamic power dissipation calculations because the assumed worst-case operating modes don't always occur. Although we are not yet prepared to officially publish a maximum value for C_{PD}, a rough guide would be to increase the published figure by 50% for worst-case calculations.

Switching transient currents

The final factor that contributes to the dynamic power dissipation of HCMOS is internal switching transient currents. When the output of a basic HCMOS inverter as shown in Fig.6(a) changes state, either from a logic "1" to a logic "0" or vice-versa, there is a brief period during which both transistors conduct. This creates a temporary low-resistance path between V_{CC} and ground as shown in Fig.6(b). In this transitory state, additional quiescent supply current (I_C) flows and power is dissipated, so input rise and fall times should be kept short. The average value of this transient current increases linearly with increasing switching frequency. In other words, power dissipation due to device switching (like power dissipation due to internal capacitance) increases linearly with increasing switching frequency. However, since it is small compared to the power dissipation due to internal capacitance, its effect is included in the published value of power dissipation capacitance (C_{PD}) which was discussed under the previous heading.

Total dynamic power dissipation

Since C_{PD} represents the load imposed by both internal capacitance and switching transient currents, the total dynamic power dissipation due to these factors is:

$$P_{CS} = C_{PD}V_{CC}^2 f_i \qquad (6)$$

The total dynamic power dissipation of HCMOS devices is obtained by adding equation (6) to the power dissipation due to the total external capacitive load (equation 5) and is given by:

$$P_D = C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) \qquad (7)$$

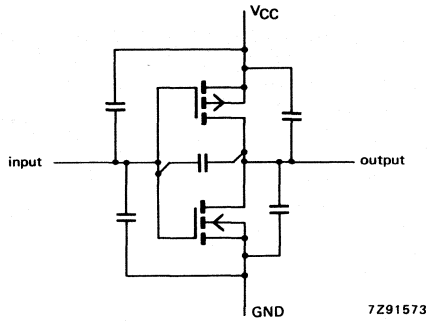


Fig. 5 Location of capacitances in an HC inverter

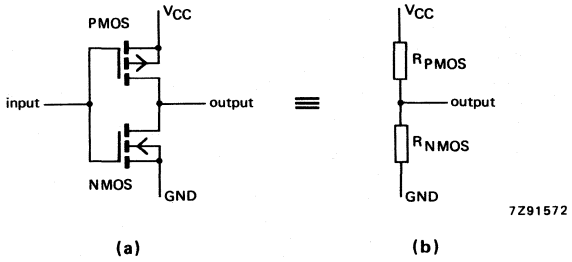


Fig. 6 When an HCMOS inverter changes state, both input transistors momentarily conduct.
(a) inverter input structure
(b) equivalent circuit when the input level is between logic levels

CALCULATING TOTAL POWER DISSIPATION FOR HC AND HCT CIRCUITS

Total HCMOS power dissipation is a summation of the appropriate quiescent and dynamic power dissipation formulae previously described.

For HC devices and HCT devices driven by CMOS levels:

$$P_{tot} = V_{CC}I_{CC} + C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) \qquad (8)$$

For HCT devices driven by TTL:

$$P_{tot} = V_{CC}(I_{CC} + \delta I_C) + C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) \qquad (9)$$

POWER DISSIPATION IN OSCILLATORS AND ONE-SHOTS

The information presented so far is only valid for devices switching rapidly between logic levels. Additional quiescent supply current I_C is greater for one-shots, oscillators and gates arranged as oscillators because, in these applications, the input slowly passes through the switching level (typically $V_{CC}/2$) causing flow-through current as shown in Fig.2. Refer to the individual data sheets for the power dissipation of these applications.

POWER DISSIPATION COMPARISON BETWEEN HCMOS, LSTTL AND ALSTTL

In any integrated circuit, there is a balance between speed and power dissipation. LSTTL logic is relatively fast but the quiescent power dissipated by its bipolar circuitry is considerable. ALSTTL improves upon LSTTL by using advanced wafer fabrication techniques and smaller geometries. These improvements increase speed and approximately halve the quiescent power dissipation.

CMOS devices dissipate negligible quiescent power compared with all bipolar TTL logic devices but, until the development of the HCMOS family, CMOS devices were relatively slow. Use of advanced wafer fabrication techniques and smaller geometries has now made it possible for HCMOS to match the speed of LSTTL and yet retain the substantial power savings afforded by CMOS. Figure 7 shows the speed-power products for today's most popular logic IC technologies.

Figures 8 and 9 compare the typical dynamic power dissipation of SSI and MSI for HC, and LSTTL devices. These graphs show that HC devices maintain their power dissipation advantages for switching frequencies up to several MHz. This is because power is only dissipated during switching. The constant, frequency-independent power dissipation exhibited by LSTTL devices is caused by the many bipolar transistors that continuously conduct.

Figures 8 and 9 also show that, as device complexity increases, the frequency at which HCMOS devices dissipate the same amoubt of power as LSTTL devices also increases. This is because, as LSTTL device complexity increases, there are more resistive paths between V_{CC} and ground which carry more quiescent bias current and thus cause more quiescent power dissipation. HCMOS devices also dissipate more quiescent power as device complexity increases, but the leakage currents which cause it are so small that it can be ignored.

The power dissipation of the different logic IC technologies is translated into total system power as a function of frequency in Fig.10 which is for a small system consisting of one gate and two flip-flops. The graph shows that HCMOS also dissipates substantially less power than LSTTL at the system level.

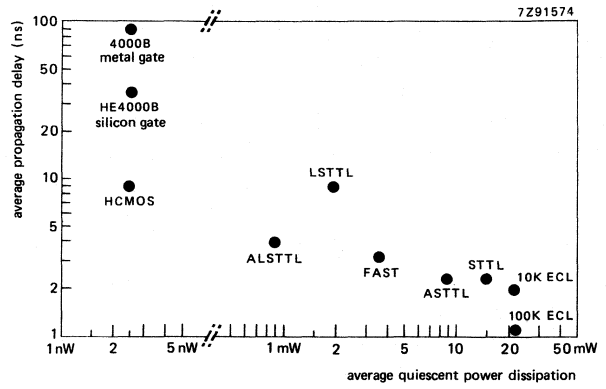


Fig. 7 Speed/power products for the most popular logic IC technologies

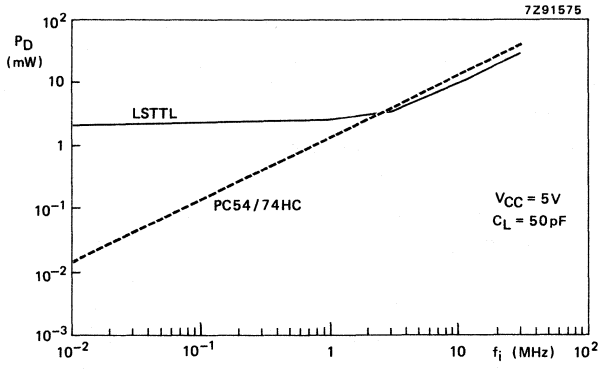


Fig. 8 Typical dynamic power dissipation as a function of switching frequency for gates

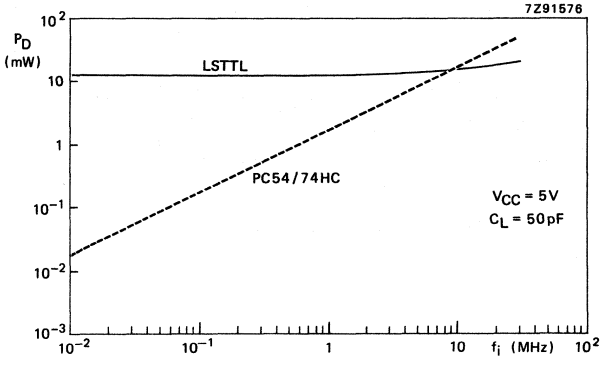


Fig. 9 Typical dynamic power dissipation as a function of switching frequency for a dual flip-flop with one of the flip-flops toggling

INFLUENCE OF HCMOS ICs ON APPLICATIONS

The significantly lower power dissipation in an HCMOS logic system, compared with its LSTTL or ALSTTL equivalent, is *the* primary reason why HCMOS devices should be used for new system designs and to replace LSTTL or ALSTTL ICs in many existing designs where power consumption and/or dissipation is a problem.

For new designs, HCMOS is the only suitable family of logic ICs for battery-powered portable personal computers. The use of HCMOS is *the* major trend in personal computers using all CMOS microprocessors, RAMS, ROMS, and peripherals. All CMOS designs can be powered-down to 2 V standby to extend battery life.

For non-portable equipment, the use of HCMOS logic and CMOS LSI is also preferred because it not only reduces power dissipation, but also significantly reduces, in order of priority, cost, size, and weight. Cost reductions stem from major reductions of power supply current and regulation, cooling fans, heatsinks, and copper buses.

An equally powerful motivating force for using HCMOS logic ICs with their lower power dissipation is the inherent and proven increase of component and equipment reliability. Equipment life is considerably extended because IC junction temperatures are much reduced and other components are exposed to lower ambient temperatures.

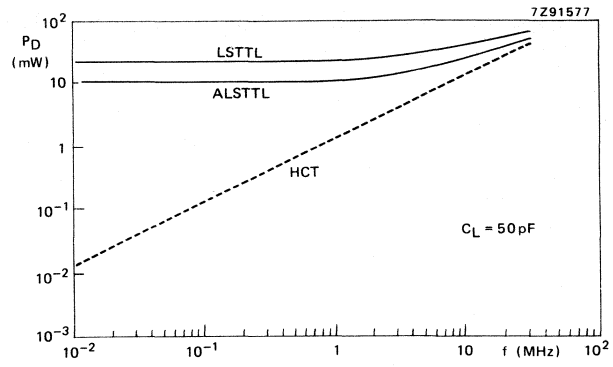


Fig. 10 Total system power dissipation as a function of frequency for a small system comprising one gate and two flip-flops

OSCILLATOR DESIGN USING THE HC/HCT LOGIC FAMILY

Many applications require a clock signal, and depending on the desired accuracy and stability, several oscillator designs can be used. In principle, an oscillator consists of an active network and a feedback network (see Fig. 1). The active network is generally a form of amplifier and the frequency dependent feedback network is made up of resistances and reactances. Figure 2 illustrates some of the more common oscillator feedback circuits. For sinusoidal oscillation, at least one of the reactances must be positive and another negative at the desired frequency.

Mainly RC circuitry or quartz crystals, combined with digital ICs, are used in oscillator designs. Due to their high gain, causing spurious oscillations, buffered HC/HCT circuits are not recommended for analog or semi-analog applications and for this reason the unbuffered 74HCU04 is provided. This unbuffered hex inverter is the only circuit in the HC/HCT family recommended for sinusoidal oscillator design. However, Schmitt-trigger input devices can be used for relaxation oscillators.

Oscillators used in digital systems in general fall into two categories:

A) RC oscillators - for applications where accuracy and stability are not critical

B) Quartz crystal oscillators

Both types of oscillators and their realization using the 74HCU04 will be described in the following sections.

A) RC oscillators

Figure 3 shows an RC oscillator with a frequency that is almost independent of the variation in IC parameter spreads. The related waveforms are shown in Fig. 4 as, depending on the output state, C_t is charged or discharged through R_t. When the input voltage of the first inverter reaches the switching level ($V_{CC}/2$ nominal), outputs A and D will change state and the current to the capacitor will change direction. Since the capacitor is both charged and discharged, to V_{CC} and GND respectively, if the switching levels of the first inverter is off-centre the a duty factor which is not 0.5 will result. However, this will have very little influence on the total repetition time. Taking this duty factor into account, the two cycle times are:

$$T_1 = R_t \times C_t \times \ln\{(V_{CC} + V_{ST})/V_{ST}\}$$

$$T_2 = R_t \times C_t \times \ln\{(2V_{CC} - V_{ST})/(V_{CC} - V_{ST})\}$$

where V_{ST} = the switching level of the first inverter.

The extremes of the switching levels can be found in the data sheets under V_{IH} and V_{IL}. Typically, V_{ST} equals $V_{CC}/2$ resulting in:

$$T_1 = T_2 = 1.09 \times R_t \times C_t$$

The oscillator frequency is:

$$f_{osc} = \frac{1}{T_1 + T_2}$$

But due to a small signal lag at node C the actual value is:

$$f_{osc} = \frac{1}{2.3 \times R_t \times C_t}$$

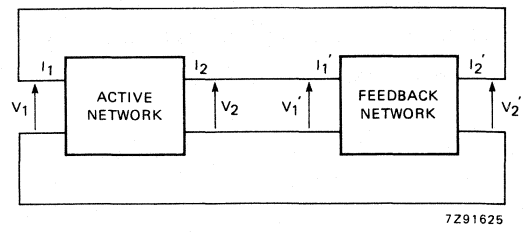


Fig. 1 Oscillator principle.

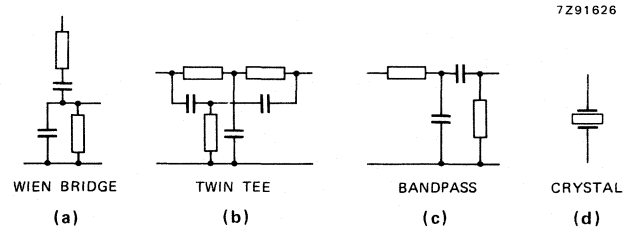


Fig. 2 Some common feedback circuits.

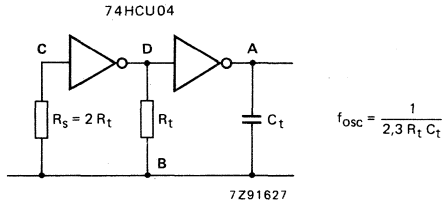


Fig. 3 Standard RC oscillator using PC54/74HCU04.

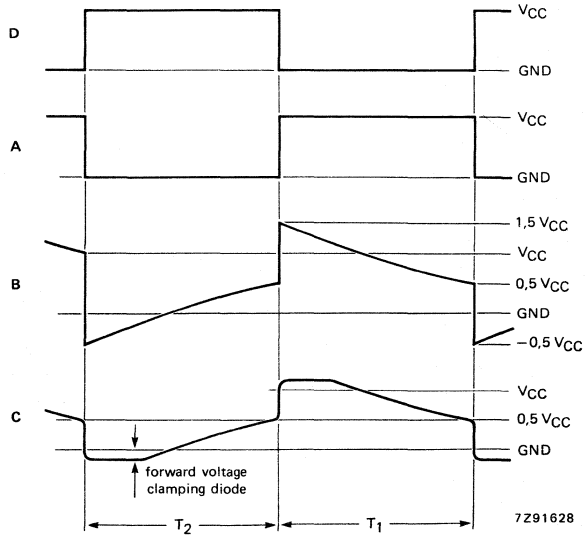


Fig. 4 Waveforms (related to Fig. 3).

From the above formulae it can be concluded that although the switching levels and the supply voltage can effect the duty cycle, they have minimal effect on the frequency.

Guidelines for 3-node RC oscillators design include:

- keep the stray capacitance at to a minimum to avoid the parasitic RC delay of R_s. R_s is provided to aprevent excessive diode input current due to node B being $V_{CC} + 0.5V_{CC}$ (nominal)
- have $R_s = 2 \times R_t$ to minimize the effect on the frequency of input clamping
- at high frequency the inverter's propagation delay affects the cycle time
- if electrolytic capacitors are used then C_t should be bipolar
- $R_{t\,min}$ must be much greater than the output on resistance (typically 30 to 40 Ω at 4,5 V) in series with it
- the recommended component values to agree with the nominal oscillation formula are:

$$C_t > 100\ pF$$
$$1\ k\Omega < R_t < 1\ M\Omega$$

- the power dissipation is determined by the sum of the specified C_{PD} value, the external component value and the additional through-current in the first stage. The through-current can be relatively high (for details see Additional power dissipation due to slow input rise and fall times in the User guide).

The RC oscillator shown in Fig. 5 is a relaxation oscillator and since the absolute input trigger levels and hysteresis determine the frequency, the oscillator is highly dependent on these factors.

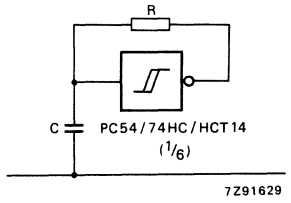


Fig. 5 Basic relaxation oscillator.

B) Quartz crystal oscillators

A quartz crystal behaves like the L, C and R circuit shown in Fig. 6. Reactance and resistance characteristics of the crystal, and the crystal with parallel and serial load capacitance are shown in Fig. 7. The terms and definitions used with crystal oscillators are given in Table 1 (in accordance with IEC 122-1).

At a certain load capacitance, specified for each crystal, the serial and parallel resonant frequencies are equal and in crystal oscillator design it is very important to maintain this value of load capacitance. However, because the board and integrated circuit pins are sources of stray capacitance, the preferred value load capacitance should be made adjustable so that the true load capacitance will be the value specified for the crystal. Preferred values of load capacitance for fundamental mode operation are:

20, 30, 50 and 100 pF

Note

In certain countries 32 pF is still used, but this is not a preferred value and its use is not recommended.

For a crystal operating in the overtone mode, the preferred values are:

8, 12, 15, 20, and 30 pF

Drive level

The power dissipated in a crystal unit is called the "drive level" and is usually expressed in mW. Beyond the range 1 pW to 1 mW, the crystal characteristics become highly dependent upon the drive level and hence crystal characteristics are usually specified at 0.5 mW. At very low drive levels, as can occur during oscillator start-up, the characteristics can vary slightly, in particular, the resonant resistance R_r may increase. To overcome this starting problem, the oscillator circuit should provide sufficient amplification but not enough to overdrive the crystal.

Today, the most widely used oscillator in digital systems is the Pierce type which is basically a Colpitts oscillator with the inductance replaced by a crystal. Figure 8 illustrates a basic Pierce oscillator (note this is a parallel oscillator). It features:

- good suppression of the third overtone (9x)
- lower dissipation in crystal than in series oscillators due to the high ohmic loading.
- amplifier requires a full 180° phase shift, so a simple inverter can be used.

Because the 74HCU04 has a high input impedance, it is ideal for Pierce oscillators. However, good power supply decoupling is necessary (see "Power supply decoupling" in this chapter) since the crystal oscillator is sensitive to parasitic capacitance that in CMOS circuits depends partially upon the power supply. In general, the output impedance of the 74HCU04 is too low to drive the crystal directly. Unfortunately, the simple solution of adding a resistor at the output, also leads to increased phase shift, so that the loop gain increases with the square of the frequency while the drive level decreases with the square of the frequency. Therefore, for higher frequencies a capacitor must be used to increase the output impedance instead of a resistor.

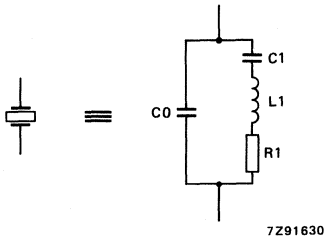


Fig. 6 Equivalent circuit of a crystal unit.

Crystal oscillators using the PC74HCU04

Figure 8 shows a basic Pierce configuration as a parallel oscillator. C_I and C_O in series, together with the stray capacitance, form the load capacitance. The total series capacitance must also be adjusted to match the crystal specification. Furthermore, the ratio of C_O to C_I will affect the total loop gain, and so:

$$V_1/V_2 = C_O/C_I$$

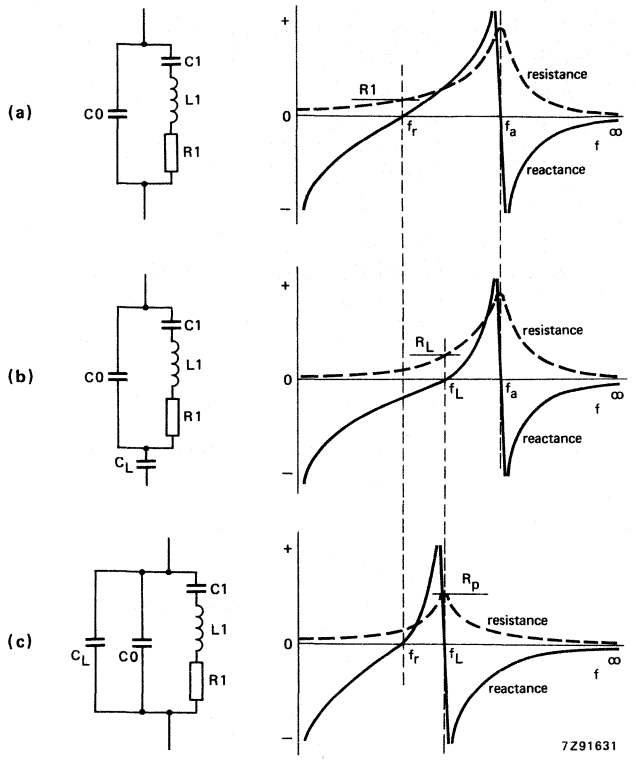


Fig. 7 Reactance and resistance characteristics; (a) resonance, (b) anti-resonance, (c) load resonance.

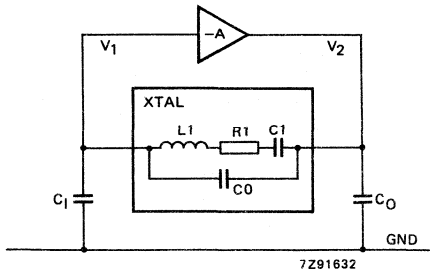


Fig. 8 Basic Pierce oscillator.

For a parallel oscillator, the total impedance of the crystal network at f_{osc} can be simplified to:

$$Z_L = X_c^2/R_L$$

where $X_c = -j/\omega C0$ and R_L is the specified series resistance of the crystal unit.

A Pierce oscillator using PC74HCU04 that operates in the fundamental mode is illustrated in Fig. 9. If we use our 4 MHz crystal (economy range), then:

$$C_L = 30\ pF$$
$$R_r = 75\ \Omega$$

At 4 MHz, a gain factor, C1/C2 of approximately 1 is adequate, and so if there is no stray capacitance:

$$C1 = C2 = 60\ pF$$

But, there will always be some stray capacitance and so 56 pF capacitors should be used, and if very accurate and stable frequencies are required, C_1 should be variable.

For optimal operation of a Pierce oscillator, the output impedance of the driving circuit should be equal to the load impedance. Since:

$$Z_L = (1/2\pi C0 f_{osc})^2/75 = 6.7\ k\Omega$$

and the output impedance of the PC74HCU04 with a 5 V supply is approximately 40 Ω, R1 would need to be 6.6 kΩ. However, this value would result in too high a phase shift and so a compromise of R1 = 2.2 kΩ is chosen. Any value between 1 and 10 MΩ (R2) is suitable for the d.c. bias of the inverter.

High frequency crystal oscillators

In addition to the phase shift introduced by R1, at high frequencies the inverter's propagation delay (t_{Pd}) contributes to the phase shift:

$$\text{Phase shift} = f_{osc} \times t_{Pd} \times 360^o$$

With a maximum t_{Pd} of 14 ns at 4.5 V, f_{osc} equal to 6 MHz would result in a further 30° phase shift. And so, taking t_{Pd} into account, it is evident that the Pierce oscillator circuit shown in Fig. 9 should not be used for high frequency applications. Modifying this circuit by replacing R1 with a capacitor (C3) approximately equal to C_L (equal to 1/2 C1) allows the design to be used for such applications (Fig. 10).

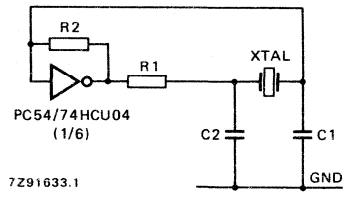


Fig. 9 Pierce oscillator using PC54/74HCU04.

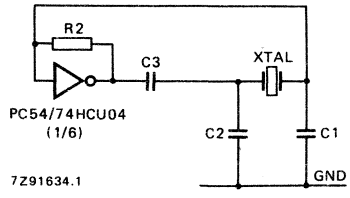


Fig. 10 Pierce oscillator using PC54/74HCU04 for higher frequencies.

Overtone crystal oscillators

Most crystal manufacturers supply fundamental mode crystals of frequencies up to 25 MHz, third overtone crystals in the range 10 to 75 MHz, and fifth overtone crystals in the range 50 to 125 MHz.

Due to the maximum permitted clock frequencies in HC/HCT systems, it may be necessary to use a third overtone oscillator as shown in Fig. 11. A critical part of an overtone oscillator is the supression of the fundamental frequency, because given the chance the crystal would always oscillate at its fundamental frequency. Here, two methods of supression are used:

- capacitor C3, which should have a value close to C_L, presents a higher impedance to the fundamental than to the overtone.
- tuning the C3/L circuit to slightly below the overtone efficiently traps the fundamental.

Tuning L for maximum output voltage may affect the oscillator frequency slightly and, in general, adjusting C2 cannot compensate for this.

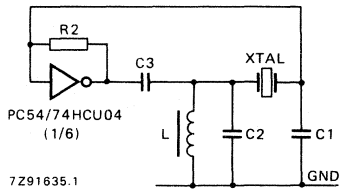


Fig. 11 Oscillator using PC54/74HCU04 in the parallel overtone mode.

Checkpoints

1. Test oscillator design under worst-case conditions (low power supply, worst-case crystal, high temperature). A worst-case crystal can be produced by adding series and parallel resistors.
2. Ensure that there is no oscillation without the crystal.
3. Check frequency stability over a V_{CC} range greater than would occur during normal operation. This gives a idea of the quality of the oscillator design.

Table 1

Terms and definitions used with crystal oscillators (in accordance with IEC 122-1).

Resonance frequency f_r	The lower of the two frequencies of the crystal unit alone, under specified conditions, at which the electrical impedance of the crystal unit is resistive.
Anti-resonance frequency f_s	The higher of the two frequencies of a crystal unit alone, under specified conditions, at which the electrical impedance of the crystal unit is resistive.
Load resonance frequency f_L	One of the two frequencies of a crystal unit in association with a series or with a paralllel load capacitance, under specified conditions, at which the electrical impedance of the combination is resistive. This frequency is the lower of the two frequencies when the load capacitance is in series and the higher when it is in parallel (see Fig. 7). For a given value of load capacitance (C_L), these frequencies are identical for all practical purposes and are given by: $1/f_L = 2\pi\sqrt{L1C1(C0 + C_L)/C1 + C0 + C_L}$
Nominal frequency f_n	The frequency assigned by the specification of the crystal unit.
Working frequency f_w	The operational frequency of the crystal unit together with its associated circuits
Overall tolerance	The maximum permissible deviation of the working frequency from nominal frequency due to a specific cause or a combination of causes.
Adjustment tolerance	The permissible deviation from the nominal frequency at the reference temperature under specified conditions.
Ageing tolerance	The permissible deviation due to time under specified conditions.
Tolerance over temperature range	The permissible deviation over the temperature range with respect to the frequency at the specified reference temperature.
Tolerance due to level of drive variation	The permissible deviation due to the variation of level of drive.
Operating temperature range	The range of temperatures as measured on the enclosure over which the crystal unit must function within the specified tolerances

Operable temperature range	The range of temperatures as measured on the enclosure over which the crystal unit must function though not necessarily within the specified tolerances
Reference temperature	The temperature at which certain crystal measurements are made. For controlled temperature units, the reference temperature is the mid-point of the controlled temperature range. For non-controlled units the reference temperature is normally 25 ± 2 °C.
Resonance resistance R_r	The resonance of the crystal unit alone at the resonance frequency f_r.
Load resonance resistance R_L	The resistance of the crystal unit in series with a stated external capacitance at the load resonance frequency f_L. Note: the value of R_L is related to the value of R_r by the following expression: $R_L = R_r(1 + C0/C_L)^2$
Level of drive	A measure of the condition imposed upon the crystal unit expressed in terms of power dissipated. Note: in special cases, the level of drive may be specified in terms of crystal current or voltage.
Unwanted response	A state of resonance of a crystal vibrator other than that associated with the working frequency.
Load capacitance C_L	The effective external capacitance associated with the crystal unit which determine the load resonance frequency f_L.
Ageing (long-term parameter variation)	The relation which exists between any parameter (e.g. resonance frequency) and time. Note: such parameter variation is due to long-term changes in the crystal unit and is usually expressed in fractional parts per period of time.
Motional capacitance C1	The capacitance of the motional (series) arm of the equivalent circuit.
Motional inductance L1	The inductance of the motional (series) arm of the equivalent circuit.

USER EDGE PROTECTION

Input protection for inputs connected directly to the board connector

Our 54/74HC/HCT circuits have input protection that can withstand all normal Electrical Static Discharge (ESD). However, an input that is connected directly to the world outside the PC-board can be exposed to stress situations during e.g.:

- transport;
- servicing (short-circuit against high external voltage);
- partial power down, resulting in an input diode current;
- operation when parts of the circuit are damaged.

For this reason many manufacturers of professional electronic equipment build in additional input protection to inputs that communicate directly with the world beyond the PC-board. A simple protection circuit is shown in Fig. 1, consisting of:

- a pull-up resistor to ensure that the input is in a defined state - even when the driving board is disconnected; and
- a series resistor to handle over-voltages by limiting the input diode current to 2 mA during operation or to below the maximum rating of 20 mA.

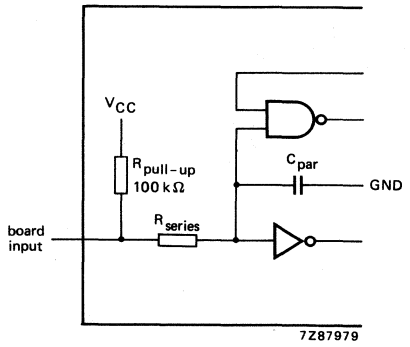


Fig. 1 Additional input protection for board inputs.

Resistor values

- The value for the pull-up resistor is easy to determine because it has only to supply the leakage current when the driving board is disconnected. Here, a good compromise between power consumption and noise sensitivity is 100 kΩ.
- The value of the series resistor is system dependent. Since there is always parasitic capacitance on IC inputs, every series resistance added will result in a further RC delay. These delays are:

For HCT: $t_{PHL} = 1{,}27RC$ s
$t_{PLH} = 0{,}33RC$ s
For HC : $t_{PHL} = 0{,}70RC$ s
$t_{PLH} = 0{,}70RC$ s

If we assume that in Fig. 1 the parasitic capacitance of each IC input is 3,5 pF and the wiring capacitance is 10 pF, then the maximum additional delay permitted is 10 ns. And so, we get:

$$R_{max} = 400\ \Omega \text{ for HCT circuits}$$

and

$$R_{max} = 840\ \Omega \text{ for HC circuits}$$

From this example, it is clear that if higher resistance values are required without having to increase the speed significantly, care must be taken to minimize the wiring capacitance.

Note

- The input capacitance of the circuit itself cannot be reduced but it is possible to reduce the number of inputs - to as low as 1.
- Connect the resistor as close to the input concerned as possible to minimize parasitic capacitance.
- Place the circuit and series resistor as close as possible to the connector to avoid cross-talk.

RECOMMENDATIONS FOR HANDLING CMOS DEVICES

Electrostatic charges

Electrostatic charges are found in many things; commonplace examples are persons wearing man-made fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and human movement. The charge is caused by friction to movement between two surfaces, at least one of which is non-conductive. The magnitude and polarity of electrostatic charge depends on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the air.

Electrostatic discharge is a transfer of electrostatic charges between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. It is the electrostatic discharge that causes damage to sensitive electronic components. All of our CMOS integrated circuits are internally protected against electrostatic discharge, but they can be damaged if proper precautions are not taken.

The following paragraphs give an outline of the precautions that can be taken to avoid damage by electrostatic discharge to sensitive devices.

Work station

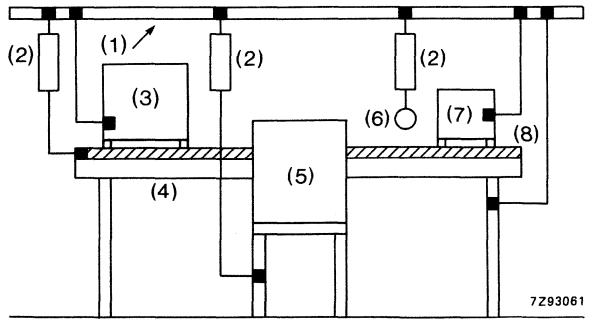
The work station (Fig. 1) is a working area constructed for the safe handling of electrostatic sensitive devices. It has a work bench with a conductive surface or with the surface covered by an antistatic sheet. A typical resistance value for the bench surface is 1 kΩ to 0.5 MΩ per cm^2. The floor covering should also be of antistatic material.

Persons working at the bench should be connected to ground potential via a wrist strap and a resistor.

All electrical equipment should be connected to the mains supply via an earth-leakage switch and the casings connected directly to ground.

Relative humidity should be kept within the range 50 to 65%.

An ionizer should be employed to neutralize objects with immobile static charges.



(1) Grounding rail
(2) Resistor (1 MΩ ± 10%, 0.5 W)
(3) Ionizer
(4) Work bench
(5) Chair
(6) Wrist strap
(7) Electrical equipment
(8) Conductive surface/ antistatic sheet

Fig. 1 Protected work station for handling electrostatic sensitive devices.

Receipt and storage

Our electrostatic sensitive devices are packed for despatch in antistatic/conductive boxes, rails or blister tape. The fact that the devices are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

Sensitive devices should be kept in their original packing whilst in storage. If a bulk container is to be partially unpacked, this work should be performed at the protected work station. The removed devices and devices requiring temporary storage should be packed in conductive or antistatic packing or carriers.

Assembly

Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the electrostatic sensitive devices are the last of the components to be mounted and that this is done at the protected work station (Fig. 1).

Devices are to be removed from their protective packing with a grounded component-pincer or short-circuit clip. Short-circuit clips are to be fitted to all leads of each device and remain there during mounting, soldering and cleansing/drying processes. Do not take more components from the storage packing than are needed at any one time.

All tools used during assembly, including soldering tools and solder baths, are to be grounded. All hand tools should be of conductive or antistatic material and, where possible, not be insulated.

Measuring and testing after assembly should be performed at the protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Carry out measuring and testing making sure that the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled printed circuit boards containing electrostatic sensitive devices are to be handled as for the sensitive devices themselves. They should carry suitable warning labels and be packed in conductive or antistatic packing.

QUALITY INFORMATION

page

Quality high-speed CMOS 841

QUALITY HIGH-SPEED CMOS

Our range of high-speed CMOS (HCMOS) includes devices that are pin-for-pin compatible with many LSTTL and HE4000B CMOS circuits. The HC series are high-speed alternatives to the 4000B series; the HCT series are low power replacements for LSTTL. Both are produced using our proven LOCOS technology, but with tighter layout (3 μm gate structures with thinner gate oxide); propagation delays are of the order of 10 ns.

Our HCMOS shares both the latch-up immunity of our HE4000B CMOS, and the high quality achieved by a zero defect-oriented production organization. All our HCMOS devices incorporate a high degree of protection against electrostatic discharge damage. The 1985 target process-average reject level is 100 ppm. Life-test results indicate a failure rate at 50 °C of 6 FITS (6 x 10^{-9}/h).

The 74/54 HC(T) device range is processed using the silicon-gate LOCOS process that we pioneered nearly 10 years ago for 4000B CMOS (Ref.1). The accumulated experience has already enabled us to achieve very high quality in our High Speed CMOS (HCMOS) production. Our process-average target for 1985 is 100 ppm.

AQLs AND CONFORMITY

All outgoing batches of our HC/HCT devices are sampled according to AQL levels as specified in Table 1. The sampling system is in accordance with MIL-STD-105D, level II, single sampling plan.

Although AQL is available for contractual quality procurement, the main purpose of this testing is the establishment of internal quality thresholds for rogue batch detection. Production quality is better than indicated by the AQL as the results expressed in ppm in Fig.1.

TABLE 1
Our standard AQLs for HCMOS

inspection criterion	ambient temperature	AQL (%) individual SSI, MSI and LSI	inspection level
cumulative electrical	full range	0,10	II
major visual		0,25	II
cumulative visual		0,65	II

Notes:

major visual: incorrect or illegible marking, and such defects as leads bent or damaged so as to prevent insertion of device into socket or wiring board.

minor visual: slight deviation from outline specification.

cumulative electrical: functional, d.c. and a.c.

functional: open or short-circuit, or failure to satisfy function table.

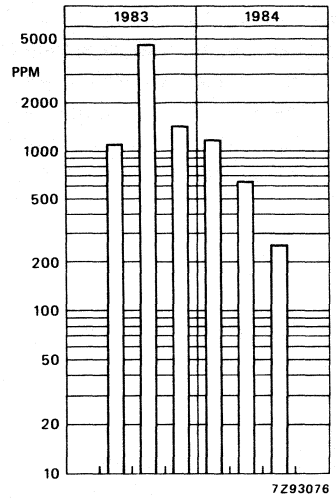


Fig. 1 Cumulative electrical ppm levels for our HCMOS as determined by Quality Control during 1983-1984.

ESD PROTECTION

Each HC/HCT series device has built-in protection against electrostatic-discharge damage (ESD). Our accumulated experience in this area has resulted in a considerably improved resistance to ESD at each device terminal (Ref.2).

Table 2 indicates the ESD resistance of our HC/HCT devices as measured by both positive and negative discharges from a 100 pF capacitor through a 1,5 kΩ resistor.

TABLE 2
ESD resistance of our HCMOS

	polarity	1% fail	50% fail
inputs	positive	2050 V	2700 V
	negative	2300 V	>3000 V
outputs		>3000 V	>3000 V
supply		>3000 V	>3000 V

LATCH-UP PREVENTION

Conventional CMOS circuits are inherent latch-up prone. Latch-up is the thyristor action in four-layer n-p-n-p structures comprising parasitic p-n-p and n-p-n transistors. It is usually destructive.

Biasing conditions

When no circuit junction is forward biased, minority-carrier injection does not take place and, thus, no parasitic transistor is activated. In practice, forward biasing leading to latch-up results from the application of voltages to either

input or output terminals in excess of positive supply voltage V_{CC} or below negative supply voltage GND. These applied voltages are clamped by junctions associated with the device terminals. Over-voltage spikes on the supply lines can also result in forward biasing through avalanche breakdown. Fast-switching and supply-line spikes can enter through junction capacitance to cause forward biasing at circuit nodes.

Parasitic structures

Figure 2(a) shows in outline a CMOS structure in which latch-up can occur. Figure 2(b) shows the equivalent circuit of the parasitic components formed from the n-channel MOST with adjoining n^+ and p^+ regions. The resistors represent the resistance to lateral current flow; their values depend on circuit geometry and doping.

Application of a negative voltage to the output results in a current I which, in turn, gives rise to a current $I \cdot h_{FB}$ in the collector of TR_2. When the voltage across r_c produced by this current is large enough, TR_3 turns on. Since the h_{FE} of TR_2 is fairly high, virtually all the collector current of TR_3 flows through $r_{bb'1}$ and $r_{bb'2}$. Sufficient voltage dropped across $r_{bb'1}$ turns TR_1 on and its collector current further increases the base drive of TR_3. Once the collector current of TR_1 is sufficient to sustain TR_3, current I due to the negative voltage on the output is no longer necessary: the current through TR_1TR_3 being, in principle, limited only by the source resistance of the power-supply.

Latch-up can also be supply-line initiated. Figure 3(a) shows the same circuit structure as Fig.2(a), but now TR_2 is lateral, formed by the source and drain junction of the associated n-channel MOST, which is part of a complementary inverter stage. Its p-channel complement (not shown) connects the n-channel drain and, consequently, the collector of TR_2 to V_{CC}. Figure 3(b) shows the equivalent circuit of this arrangement complete with actual inverter stage.

Excessive supply voltage can break down the collector-base junction of TR_2. Thyristor TR_1TR_2 will trigger if the resulting current flow through $r_{bb'1}$ is sufficient to turn TR_1 on. Although the breakdown current through TR_2 is limited by the on-state resistance of the p-channel MOST

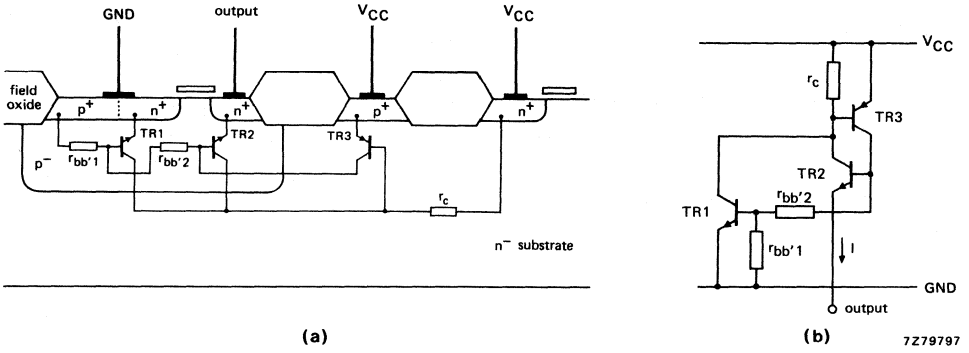


Fig. 2 (a) Section through a CMOS circuit showing how parasitic components are formed.
(b) Equivalent circuit of the parasitic components shown in (a)

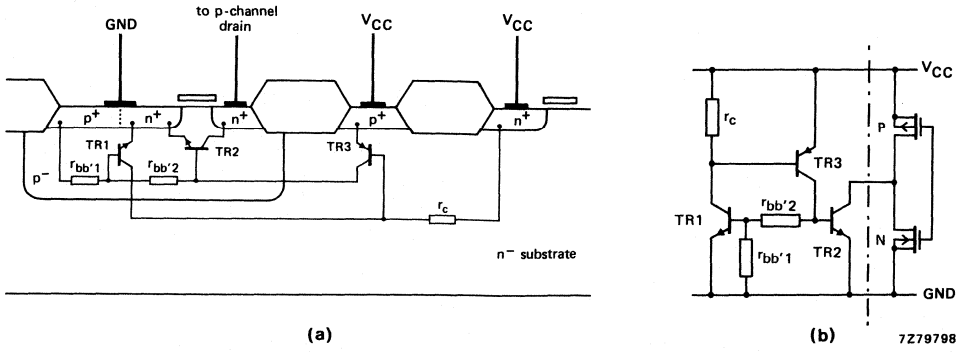


Fig. 3 (a) The structure of Fig. 2, but with TR_2 now formed laterally.
(b) Equivalent circuit incorporating the lateral transistor TR_2

the current through TR_1TR_3 is limited only by power-supply resistance.

It can by seen from Fig.3(b) that a sharp positive-going transient on the supply line can also produce a trigger voltage across $r_{bb'1}$ directly as the result of current through the capacitance of the collector-base junction of TR_2.

Precautions

This outline description of latch-up phenomena serves to illustrate the problem and indicate measures that can be taken to reduce the chance of latch-up occurring.

It is apparent from both Figs.2 and 3 that both the values of $r_{bb'1}$ and r_c, and the topologies of the p^+ and n^+ diffusions to the n-type substrate are important factors in susceptibility to thyristor latch-up. Considerable improvement can be obtained by careful design of the source-to-pocket contact of the n-channel MOST and the interchange of the p^+ and n^+ diffusions to the substrate, as shown in Fig.4. The value of r_c can be reduced by arranging the n^+ diffusion as a guard ring around the n-channel device. This solution, however, increases device area considerably. The best way of coping with the problem is to avoid lateral current flow in the n-type substrate. This can be achieved by growing an epitaxial layer on a very low resistivity substrate, as shown in Fig.5.

The properties of our HCMOS process enable both geometry precautions and an epitaxial substrate to be used. Since the d.c. current required for latch-up initiation is generally in excess of 80 mA at any input and over 100 mA at any output, the HC/HCT range can be considered virtually latch-up proof.

RELIABILITY AND QUALIFICATION

Extensive testing is performed continually in order to determine the mechanical and electrical reliability of our HC/HCT devices.

All tests are performed on plastic (epoxy) products, except 175 °C and 225 °C life tests which are performed on cerdip devices. Table 3 gives the test results for 1983 and 1984.

Endurance testing of our HC/HCT series consists of

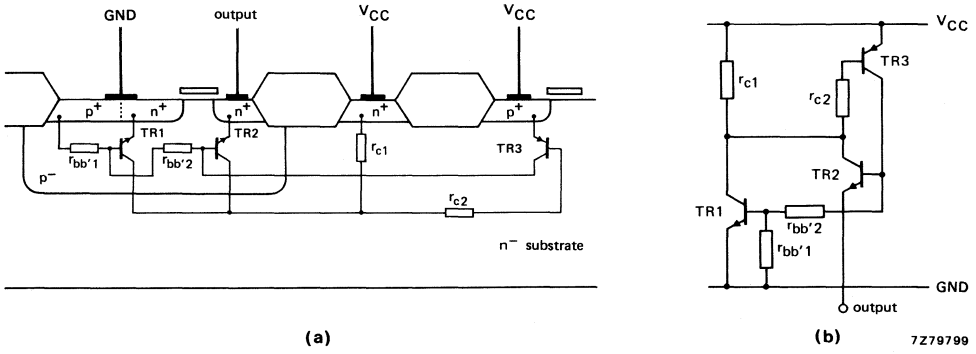


Fig. 4 (a) Rearrangement of the structure of Fig. 3(a) greatly reduces the susceptibility to latch up by incorporating base resistance r_{c2} as shown in the equivalent circuit (b)

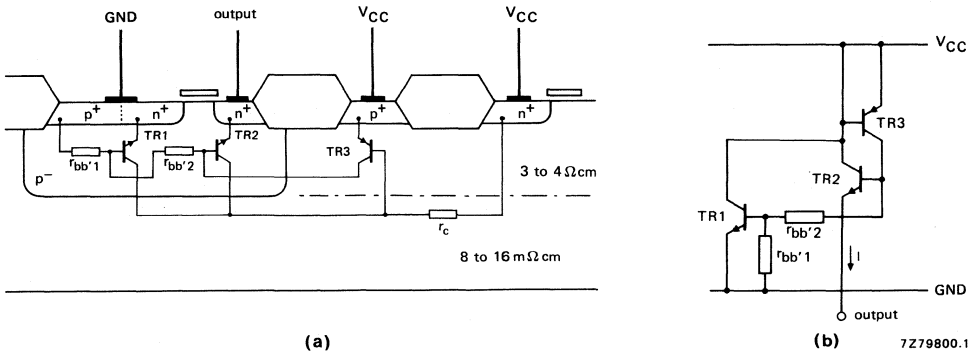


Fig. 5 (a) By growing an epitaxial layer on a very-low resistivity substrate, the lateral current flow responsible for latch-up is very largely eliminated. The resulting circuit is virtually latch-up proof, (b)

static life-tests (V_{CC} = 6 V, inputs 6 V or 0 V, outputs floating) at various temperatures. The test results given in Table 4 are derived from tests on many different device types, both HC and HCT. Note that some failures recorded did not involve lack of function and so are not complete failures.

The results given in Table 4 can be converted to equivalent results at the usual operating temperature of 50 °C, using Arrhenius' Law.
Assuming an activation energy of 0,7 eV (as used in MIL-HDBK-217D) produces the results of Table 5. These indicate a failure rate of 6 FITS (6 x 10^{-9}/h).

TABLE 3
Group B and C Quality Control Acceptance test results for our HCMOS 1983 and 1984 (cumulative)

test	duration	sample	failures	analysis
THB (85 °C, 85% RH, 6 V)	1000 h	540	2	2 x I_{CC}, 1 x corrosion
	2000 h	520	5	4 x I_{CC}, 1 x corrosion
	3000 h	320	7	2 x I_{CC}, 4 x corrosion
	4000 h	159	5	2 x I_{CC}, 3 x corrosion
	6000 h	120	6	3 x I_{CC}, 3 x corrosion
temperature cycling (–65 °C to +150 °C)	1600 h	260	0	
ESD (>2000 V)	3 pulses	54	0	
storage (–65 °C)	1000 h	40	0	
storage (+150 °C)	1000 h	40	0	

TABLE 4
Results of static life testing of our HCMOS (cumulative)

temp. (°C)	48 h	168 h	1000 h	2000 h	4000 h	8000 h
150			0/200	2/200[1]	2/200	2/200
			3/408[2]	3/408		
	0/1216		1/1216[3]			
	1/1462[4]					
175			3/320[5]	4/320[6]		
225		0/48	0/48			

[1]) 2 x I_{CC}
[2]) 1 x gate oxide; 1 x I_{CC}; 1 x I_{CC}
[3]) 1 x gate oxide
[4]) I_{CC}
[5]) 1 x I_{CC}; 1 x I_{CC}; 1 x V_{OH}
[6]) 2 x I_{CC}; 1 x I_{CC}; 1 x V_{OH}.

TABLE 5
Static lift test results derated to the normal operating die temperature of 50 °C

test temperature (°C)	equivalent 50 °C device hours (x 10^6)	observed failures
150	1414	7
175	714	4
225	331	0
totals	2459	11
failure rate (at 60% UCL): 6 x 10^{-9}/h (FITS)		

Specification Highlights

HC DEVICES

- full parametric DC and AC specification at a power supply of 2 V, 4,5 V and 6 V over the ambient temperature range
- 20% and 70% input switching levels

HCT DEVICES

- full parametric DC and AC specification at a power supply of 5 V ±10% over the ambient temperature range
- 0,8 V and 2 V input switching levels

FAMILY

- operating ambient temperature range
  75HC/HCT: −40 to +85 °C
  54HC/HCT: −55 to +125 °C
- output drive capability
  standard: 10 LSTTL
  bus driver: 15 LSTTL
- propagation delays at V_{CC} = 4,5 V and C_L = 50 pF
  gates: 10 ns
  latches: 15 ns
  flip-flops: 20 ns
- operating frequency at V_{CC} = 4,5 V and T_{amb} = 25 °C
  f_{max}: 30 MHz (60 MHz typical)
- symmetrical output transition times at C_L = 50 pF
  standard outputs: $t_{TLH} = t_{THL}$ = 7,5 ns
  bus driver outputs: $t_{TLH} = t_{THL}$ = 6,0 ns

NOTES

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